

Measuring and Modeling the Effects of Substrate Noise on the LNA for a CMOS GPS Receiver

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ABSTRACT

The influence of substrate noise generated in digital circuit on the low-noise amplifier (LNA) of a CMOS GPS receiver has been experimentally characterized and theoretically analyzed. A frequency domain approach is used to model noise injection into the substrate from the digital circuitry and the mechanisms by which that noise can affect analog circuit behavior. The results reveal that substrate noise can modulate the LNA input signals as well as directly couple to the LNA output.

I. INTRODUCTION

Crosstalk from digital circuitry into sensitive analog circuits via the common substrate may preclude the practical integration of a complete broadband communications receiver on a single CMOS chip [1]. A number of techniques have been proposed for studying the propagation of substrate noise by estimating the equivalent substrate impedance [2], [3]. This paper focuses on the experimental and analytical study of how the characteristics of substrate noise are related to the specific nature of the digital circuitry and how the substrate noise might impact the performance of analog RF circuits. The low noise amplifier (LNA) for a CMOS GPS receiver [4], integrated on the same chip as a digital circuit emulator and a substrate noise sensor, is used as a test vehicle for this study. Models for the substrate coupling are developed based on the initial analytical and experimental results, and predictions obtained with the model are then verified by the further experiments.

II. EXPERIMENTAL SETUP

A test chip was fabricated in a 0.5- μm , single-poly, triple-metal epitaxial CMOS technology, operating from a 2.5V power supply. The chip contains the front-end circuits of a CMOS GPS receiver, including the LNA, mixer, IF amplifier, IF filter and PLL. Figure 1 shows the simplified schematic of the fully differential LNA[4]. Figure 2 is a chip micrograph. To study the crosstalk between digital and analog circuits, a digital circuit emulator and a substrate noise sensor were included on the chip. The chip was packaged in a 52-pin J-lead chip carrier, and surface-mounted on a two layer copper board. Special care was taken to minimize package and board-level noise coupling. For example, analog bondwires are positioned perpendicular to the digital bondwires, analog and digital components are physically separated on the board, and separate power supplies are used for various functional blocks on the test chip.

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The digital circuit emulator comprises nine tri-state buffers driving capacitive loads that are formed by integer multiples of a unit junction capacitor, $C_0=0.34\text{pF}$. The tri-state buffers are controlled by a shift register so as to vary the total coupling capacitance (C_{couple}) to the substrate from C_0 to $183C_0$ with a step size of C_0 . All of the buffers are sized so that rise and fall time of their output $t_{\text{rise/fall}}$ equals 0.9ns, with one exception. The buffer driving the load of $56C_0$ capacitor actually consists of 3 tri-state buffers in parallel, with their binary weighted sizing. This allows the $t_{\text{rise/fall}}$ of this buffer to vary among 0.9, 1.0, 1.2, 1.4, 1.8, 2.7, 5.4ns. The digital clock that drives the inputs of the tri-state buffers can be generated on-chip by a 7.1-MHz ring oscillator or provided from off chip as a small swing signal with variable frequency (f_{clock}) and duty cycle.

The substrate noise sensor consists of a single NMOS transistor that senses the substrate noise through the body effect and capacitive coupling to the gate, drain, and source nodes. The source and the gate terminals of the NMOS are biased with dedicated power supplies, and its drain is connected through an off-chip 1-k Ω resistor to the 2.5-V supply. The drain is ac coupled to the 50- Ω input of an oscilloscope or spectrum analyzer. To reduce the capacitive coupling this ac output, the bonding pad connected to the drain is ground shielded. The sensor has a gain of -29dB.

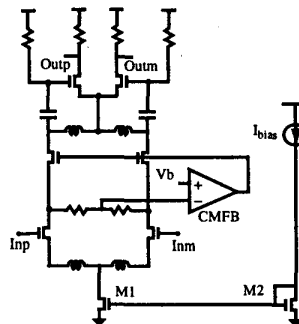


Figure 1: Low-noise amplifier for a GPS receiver [4].

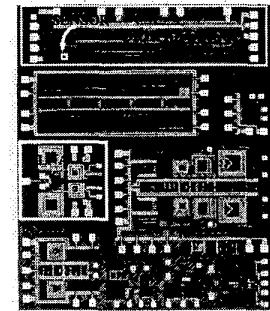


Figure 2: Chip micrograph

III. SUBSTRATE NOISE CHARACTERIZATION

Figure 3 shows an example waveform measured at the substrate noise sensor output with $C_{\text{couple}} = 43.5 \text{ pF}$, $t_{\text{rise/fall}} = 0.9 \text{ ns}$, and $f_{\text{clock}} = 7.1 \text{ MHz}$. In the time domain, substrate noise sensor output is characterized in terms of its negative peak voltage (V_{np}), positive peak voltage (V_{pp}) and settling time (t_{settle}).

For the same $t_{\text{rise/fall}} = 0.9 \text{ ns}$, but different values of C_{couple} the substrate noise sensor output waveforms are all similar to

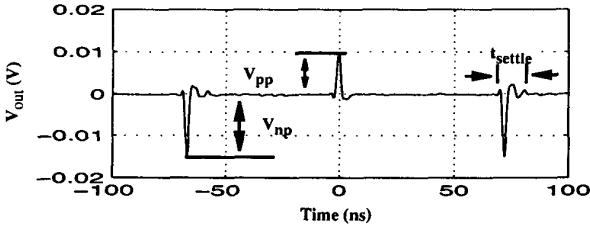


Figure 3: Measured substrate noise sensor output waveform when $C_{\text{couple}}=43.52\text{pF}$, $f_{\text{clock}}=7.1\text{MHz}$, $t_{\text{rise/fall}}=0.9\text{nsec}$.

Figure 3. However, $|V_{\text{pp}}|$ and $|V_{\text{np}}|$ increase linearly with C_{couple} as shown in Figure 4, while t_{settle} does not change. These experimental results suggest that the substrate noise is a linear function of the coupling capacitance if $t_{\text{rise/fall}}$ is constant.

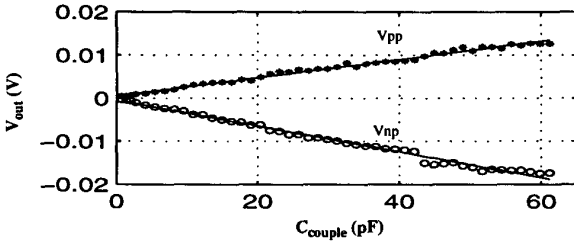


Figure 4: Measured V_{np} , V_{pp} as a function of C_{couple}

For a fixed $C_{\text{couple}} = 56C_0$, but different values of $t_{\text{rise/fall}}$, time domain waveforms and their spectra were both measured. Figure 5(a) and (c) show that in the time domain when $t_{\text{rise/fall}}$ is reduced from 5.4 ns to 0.9 ns, the substrate noise magnitude increases by almost three times, while t_{settle} decreases slightly. Figure 5(b) and (d) show that in the frequency domain, substrate noise locates at integer multiples of the digital clock frequency (f_{clock}). When $t_{\text{rise/fall}}$ decreases from 5.4 ns to 0.9 ns, the low frequency components of the substrate noise remain almost unchanged while the magnitude of its high frequency components increase from under the noise floor to about 10 dB above the noise floor.

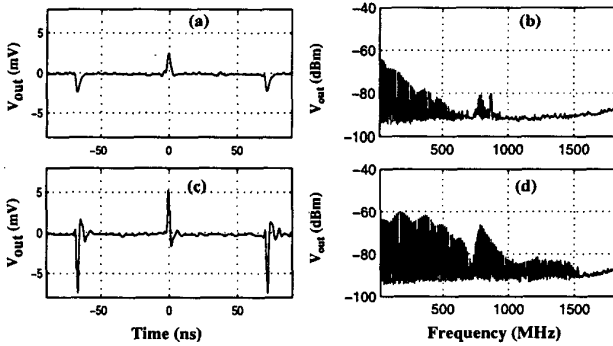


Figure 5: Measured substrate noise sensor output waveforms and spectra (a) (b) $t_{\text{rise/fall}}=5.4\text{nsec}$, (c) (d) $t_{\text{rise/fall}}=0.9\text{nsec}$.

Experiments were also conducted to examine the effectiveness of staggering digital switching transitions to reduce the substrate noise. To emulate the case of digital switching without

such staggering, buffers driving a load of $96C_0$ was switched at a frequency of 20 MHz. To simulate the staggering of the digital transitions, the digital switching was then modified as follows: $48C_0$ was switched during the first half of the 20-MHz clock cycle, and the other $48C_0$ was switched during the latter half of the cycle, which is equivalent to switching $48C_0$ at a frequency of 40 MHz. The measured results shown in Figure 8 indicate that staggering does not reduce the substrate noise in all frequency ranges, although the total noise power and the magnitude of the noise peaks in the time domain are reduced by a factor of 2.

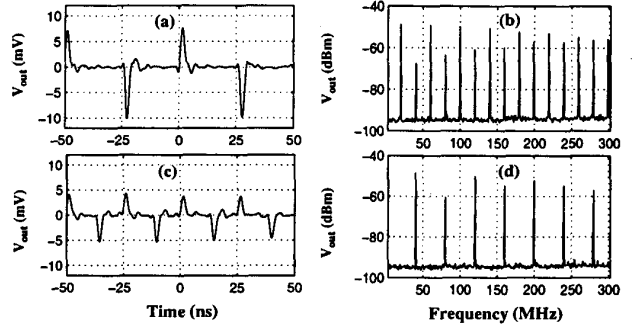


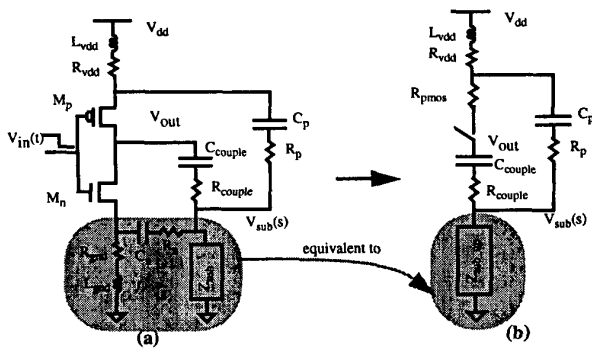
Figure 6: Measured waveforms and spectra at the substrate noise sensor output (a), (b) without staggering the digital switching, (c), (d) staggering the digital switching.

Figure 7(a) shows a simplified circuit used to model substrate noise injection, with the P^+ bulk represented by a single node. Suppose at $t = 0$, $V_{\text{in}}(t)$ transitions from high to low, so that M_p is on and M_n is off. Using R_{pmos} to represent the equivalent resistance of M_p , Figure 7(a) can be further simplified as shown in Figure 7(b). Generally since $C_{\text{couple}} \ll C_p$ and $R_p \ll R_{\text{pmos}}$, the resulting substrate noise is

$$V_{\text{sub}}(s) = \frac{C_{\text{couple}}}{(1 + \tau_{\text{up}}s)} \times \frac{V_{\text{dd}}Z_{\text{sub-up}}}{1 + (Z_{\text{sub-up}} + L_{\text{vdd}}s + R_{\text{vdd}}) \frac{C_p s}{1 + R_p C_p s}} \quad (1)$$

where τ_{up} is the rise time of the buffer output. The time domain substrate noise $V_{\text{sub}}(t)$ is the inverse Laplace transform of $V_{\text{sub}}(s)$. Similar equations can be derived for the low-to-high transition of V_{in} . In the time domain, the total substrate noise is the summation of substrate noise caused by each digital transition. For a digital circuit switching at a period of T , the corresponding substrate noise spectrum can be derived by the Fourier transform of the time domain noise. Thus in the frequency domain, substrate noise locates at k/T , with a magnitude determined by $V_{\text{sub}}(2\pi jk/T)/T$, where k is an integer.

Eq. 1 shows that the substrate noise is indeed proportional to C_{couple} while its settling time (t_{settle}) is independent of C_{couple} . It further indicates that $V_{\text{sub}}(s)$ is inverse proportional to $1 + \tau_{\text{up}}s$. Thus, it predicts that at high frequencies substrate noise power decreases quadratically with an increase of $t_{\text{rise/fall}}$, but the low frequency noise components are not influenced significantly by changes in $t_{\text{rise/fall}}$.



C_{couple}, R_{couple}	junction capacitance and epi resistance under C_{couple}
$L_{vdd}, R_{vdd}, L_{gnd}, R_{gnd}$	power supply inductance and resistance result from package and wiring
C_n, R_n	equivalent capacitance and resistance from chip ground to the heavily doped substrate. C_n includes wiring capacitance and junction capacitance from NMOS
C_p, R_p	equivalent capacitance and resistance from chip power supply to the heavily doped substrate. C_p includes wiring capacitance and the well capacitance
Z_{sub}	equivalent substrate impedance from the P+ substrate through substrate contact to the board ground
Z_{sub-up}	the equivalent impedance for the network formed by $R_{gnd}, L_{gnd}, C_n, R_n, Z_{sub}$
M_p, M_n	driver transistors
R_{pmos}	the equivalent resistance of M_p

Figure 7: Simplified model for the substrate noise injection circuit with single node representation of the heavily doped substrate.

IV. MEASURED SUBSTRATE NOISE EFFECTS ON LNA

The LNA output spectrum was examined experimentally with a sinusoidal input of -60 dBm at 1.575 GHz. When the digital circuit emulator is off, the LNA output spectrum has a single -44 dBm tone at 1.575 GHz, as shown in Figure 8 (a).

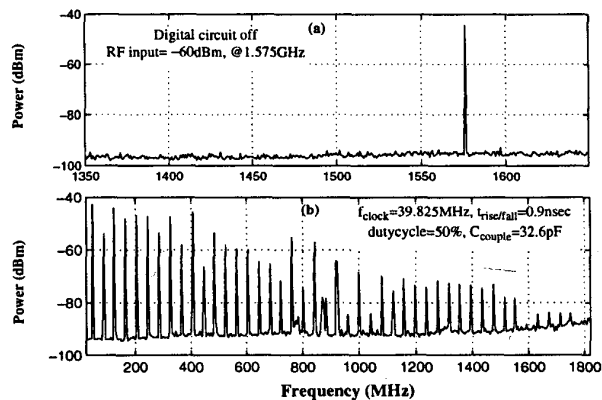


Figure 8: Measured (a) LNA output spectrum when digital circuits are inactive; (b) spectrum at the substrate noise sensor output, when the digital circuits are on.

Figure 8(b) shows the measured substrate-noise-sensor output spectrum when the digital circuit emulator is on, with

$C_{couple}=32.6$ pF, $t_{rise/fall}=0.9$ ns and $f_{clock}=39.825$ MHz. Under the influence of this substrate noise, the LNA output includes not only the -44 dBm, 1.575 GHz RF signal but also noise tones as shown in Figure 9(a). Further study indicates that noise tones at $1.354, 1.394, 1.434, 1.474, 1.513, 1.553, 1.593, 1.633$ GHz are the result of digital switching noise at the 34th to 41st harmonics of f_{clock} , while the noise tones at $1.615, 1.535, 1.456, 1.416, 1.376$ GHz are caused by intermodulation (IM) between the 1.575 -GHz RF signal and the substrate noise at the 1st, 1st, 3rd, 4th, and 5th harmonics of f_{clock} . To confirm this, the RF input frequency was decreased by 5 MHz to 1.570 GHz with the result, shown in Figure 9 (b), that the noise tones at the harmonics of f_{clock} remain unchanged, while the noise tones due to intermodulation are shifted down 5 MHz.

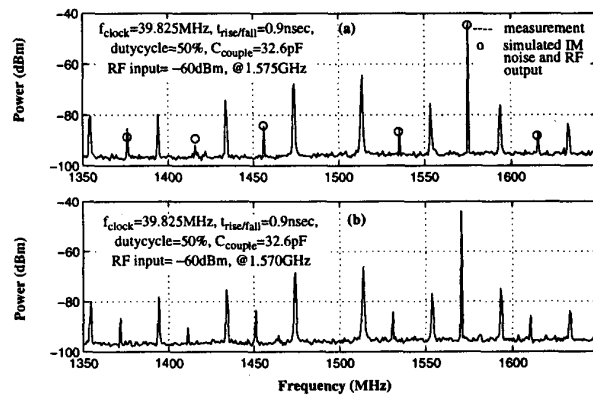


Figure 9: (a), (b) Measured LNA output spectrum in the presence of substrate noise, and the IM tones shift down 5MHz when the RF frequency is decreased by 5MHz.

V. NOISE COUPLING MECHANISM AND MODELING

Theoretically, the output, Y , of a fully differential analog circuit can be modeled as the difference between two identical system functions, $F(X \pm x_d/2, B)$, where X , x_d , and B are the common-mode dc input, the differential ac input, and the bias. Substrate noise coupled to this circuit can be modeled as perturbations of the bias (δ_b) and inputs ($\delta_{xc} \pm \delta_{xd}/2$), so that F can be rewritten as $F(X \pm x_d/2 + \delta_{xc} \pm \delta_{xd}/2, B + \delta_b)$. δ_b and δ_{xc} are referred to herein as common-mode noise, while δ_{xd} is differential-mode noise.

The output response Y can be approximated by retaining the first and second order terms of the Taylor's series expansion of F , as shown in Figure 10. From this approximation it is apparent that common-mode noise influences the output through intermodulation with the differential inputs, while differential mode noise appears at the output directly, scaled by some gain factor. In this example, the GPS received signal is band-limited to the range 1.57442 GHz to 1.57642 GHz [4]. Therefore, only high-frequency differential-mode noise and low-frequency common-mode noise mixed with the RF signal can fall into the RF signal band and degrade the LNA's performance.

The effect of common-mode noise on the LNA response can

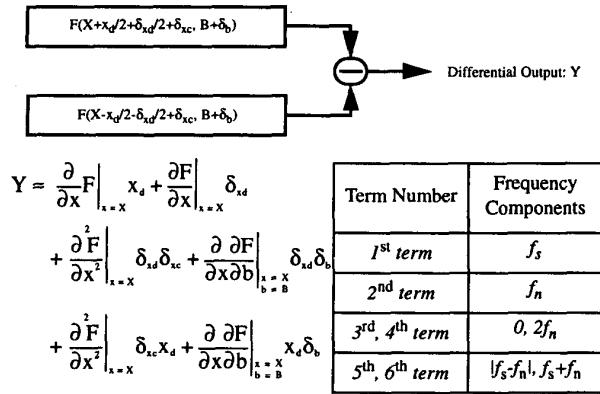


Figure 10: Model of substrate noise in a fully differential circuit.

be modeled with a single-node approximation of the heavily doped substrate, and simulations match the experimental measurements with a maximum difference of 3.4dB, as shown in Figure 9 (a). Common-mode noise perturbs the bias of the LNA, and thereby modulates the RF input. Referring to Figure 1, substrate noise coupled to M2 causes its (and M1's) gate voltage to vary (δ_{v_g}). The same noise could also cause M1's drain current to vary, but this will be canceled by δ_{v_g} if M2 matches M1. HSPICE simulations show that changing the width ratio between M1 and M2 from 18:1 to 1:1 reduces the IM power by 10 dB. Experiments combined with simulations, also suggest that placing the substrate contact close to the source of the NMOS transistors reduces the IM power.

The differential-mode noise is more difficult to model because a single-node representation of the substrate is no longer valid. As a result of asymmetry between the two differential branches in the circuit, digital switching noise can cause differential-mode perturbations through either electrical or magnetic coupling. The asymmetry can result from process variations, bonding or packaging mismatch, or location asymmetry with respect to the digital circuit. For the test chip, as shown in Figure 2, the digital circuitry is located parallel to the symmetric axis of the LNA and is most likely the source of the high-frequency differential-mode noise observed in the LNA output.

The equation in Figure 10 suggests that the impact of substrate crosstalk on analog circuit performance can be reduced by lowering substrate noise power in those frequency ranges that can result in output noise in the analog signal band. As predicted by Eq. 1, high-frequency substrate noise power decreases quadratically with the transition times ($t_{rise/fall}$) of transients in the digital circuits. Substrate noise power decreases quadratically with a decrease in the coupling capacitance to the substrate, as does the power of the IM components in LNA output. Figure 11(a) indicates that the measured power (in dBm) of the 1.513 GHz noise tone decreases linearly with the log of $t_{rise/fall}$. Figure 11(b) plots the measured power of the largest IM tone (at 1.456 GHz) in the LNA output as a function of the coupling capacitance, as well as the power of the substrate noise tone at 119 MHz that causes this noise.

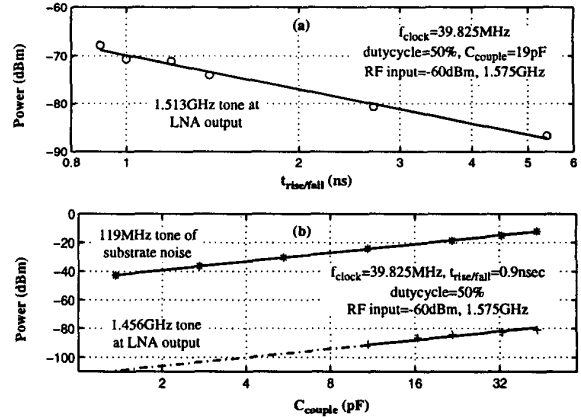


Figure 11: In the measured LNA output: (a) the power of the largest harmonic noise tone decreases with $t_{rise/fall}$; (b) the power of the largest IM tone, and the power of the 119-MHz substrate-noise tone that causes this IM tone, increase with increasing coupling capacitance.

VI. CONCLUSION

This paper presented experiments and theoretical analysis related to two issues: (1) the relationship between substrate noise and the characteristics of the digital circuitry, (2) the mechanisms by which substrate noise affects the low-noise amplifier in a communications receiver. It was shown that the spectral distribution of substrate noise greatly affects its impact in such a system. With the LNA as an example, both analysis and measurements indicate that although the substrate noise power may be several orders of magnitude higher than the received GPS signal power, only those noise components located in a specific frequency range actually degrade the LNA performance. The frequency domain analysis and models presented in this paper provide insight into substrate noise mitigation. It is shown that some time domain techniques for reducing substrate noise, such as increasing the digital transition time, are not always effective in reducing low-frequency substrate noise.

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