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Phase Noise in Multi-Gigahertz CMOS Ring Oscillators

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Abstract

An analysis of the phase noise in differential and single-ended ring oscillators using a time-variant model is presented. An expression for the RMS value of the impulse sensitivity function (ISF) is derived. A closed-form equation for phase noise of ring oscillators is calculated and a lower limit on the phase noise of ring oscillators is shown. Phase noise measurements of oscillators running up to 5.5GHz are shown to be in good agreement with the theory.

Introduction

Due to their integrated nature, ring oscillators have recently become an important building block in many digital and communication systems [1]. They can also be used for some low-tier RF products.

Recently, there has been some work on modeling the phase noise in ring oscillators. [2] and [3] develop models for clock jitter based on time domain treatments of MOS and bipolar differential ring oscillators, respectively. Reference [4] proposes a frequency domain approach to find the phase noise based on an LTI model for differential ring oscillators with a small number of stages.

In this work we present a general framework to calculate the phase noise of ring oscillators by applying a time-variant phase noise model [5] to ring oscillators.

Based on this derivation we obtain a lower limit on the phase noise of ring oscillators in long and short channel regimes. Good agreement is observed between the predictions and measurement results of the phase noise of ring oscillators running up to 5.5GHz.

Brief Review of the Time-Variant Model

In any practical oscillator, there are fluctuations in amplitude and phase due to internal and external noise. The amplitude fluctuations are significantly attenuated by the amplitude limiting mechanism which is present in any practical stable oscillator and is very strong in ring oscillators. Therefore, we will focus on phase variation, which is not quenched by such a restoring mechanism.

The output of an oscillator can be written as

$$V_{out}(t) = A(t) \cdot f[\omega_0 t + \phi(t)] \quad \textbf{(1)}$$

Being interested in its phase, $\phi(t)$, we can treat an oscillator as a system that converts voltages and currents to phase. As will be seen shortly, for small perturbations this is a linear system. It is also a time-variant system no matter how small we make the perturbations. As an example, consider the arbitrary single-ended ring oscillator with a single current source on one of the nodes, as shown in Fig. 1. Suppose that the current source consists of an impulse of current with area Δq (in coulombs), occurring at time $t=\tau$. This will cause an instantaneous change in the voltage of that node which is given by

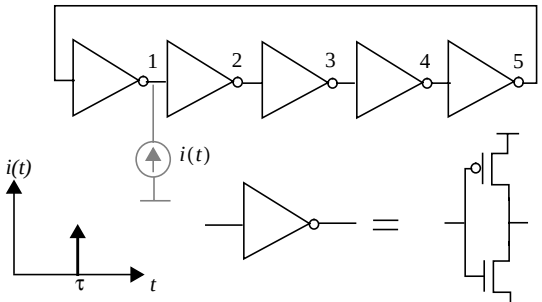

Fig. 1. CMOS inverter chain ring oscillator.

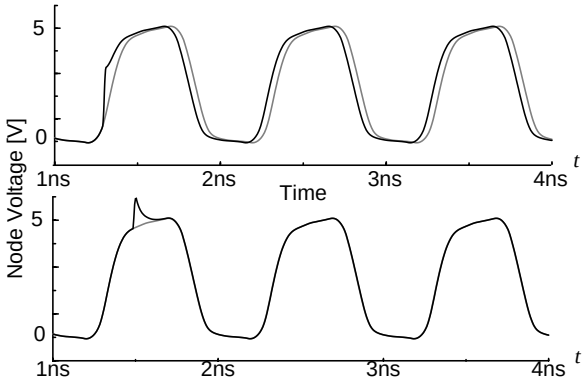

Fig. 2. Time variance of the phase response.

$$\Delta V = \frac{\Delta q}{C_{node}} \quad \textbf{(2)}$$

where C_{node} is the effective capacitance on that node at the time of charge injection. This corresponds to an equivalent shift in the transition time for small changes in voltage. Therefore the change in the phase, $\phi(t)$, is given by

$$\Delta\phi \propto \frac{\Delta V}{V_{swing}} = \frac{\Delta q}{q_{max}} \quad \textbf{(3)}$$

where $q_{max} = C_{node}V_{swing}$ and V_{swing} is the voltage swing across the capacitor. However, the proportionality constant is time-dependent. This can be visualized by considering two extreme cases. One case is when the impulse is injected during an output transition. This will result in a large phase shift. As the other extreme case, consider injecting an impulse while the output is saturated either to supply or ground. This impulse will have a minimal effect on the phase of the oscillator, as shown in Fig. 2.

Unlike the amplitude response, once the phase shift is introduced into the oscillator its effect persists indefinitely, since subsequent transitions are shifted by the same amount. Thus, the phase response of an oscillator to an impulse is a time varying step. Also note that as long as the introduced change in the voltage due to the current impulse is small, the resultant phase shift is linearly proportional to the injected charge, and hence the transfer function from current to phase is linear. However, the time variant nature of the system does not disappear even for small perturbations.

We define the unit impulse response of the system as the amount of phase shift per unit current impulse. Based on the foregoing argument, we obtains the following time dependent impulse response

$$h_\phi(t,\tau) = \frac{\Gamma(\omega_0\tau)}{q_{max}}u(t-\tau) \quad \textbf{(4)}$$

where $u(t)$ is the unit step and $\Gamma(x)$ is a periodic unitless function with period 2π, which gives the time varying proportionality constant for (3). It is large when a given perturbation causes a large phase shift and small where it has a small effect [5]. Since $\Gamma(x)$ represents the sensitivity of every point of the waveform to a perturbation, $\Gamma(x)$ is called the *impulse sensitivity function* (ISF).

Knowing the impulse response, we can calculate $\phi(t)$ using the superposition integral

$$\phi(t) = \int_{-\infty}^{\infty} h_\phi(t,\tau)i(\tau)d\tau = \int_{-\infty}^{t} \frac{\Gamma(\omega_0\tau)}{q_{max}}i(\tau)d\tau \quad \textbf{(5)}$$

where $i(t)$ represents the input noise current injected into the node of interest. Note that the integration arises from the closed loop nature of the oscillator. For a white noise current source, the argument of the second integral of (5),

$$\psi(t) = \frac{\Gamma(\omega_0 t)}{q_{max}}i(t) \quad \textbf{(6)}$$

has the following power spectrum

$$S_\psi(f) = \Gamma_{rms}^2 \cdot \frac{\overline{i_n^2}/\Delta f}{2q_{max}^2} \quad \textbf{(7)}$$

where $\overline{i_n^2}/\Delta f$ represents the single-sideband power spectrum of the noise current source and Γ_{rms} is the root mean square (RMS) value of the ISF. $\phi(t)$ is related to $\psi(t)$ through an ideal integration; therefore, the single sideband phase noise spectrum for a ring oscillator with N identical stages is

$$L\{f\} = N\frac{\Gamma_{rms}^2}{8\pi^2 f^2} \cdot \frac{\overline{i_n^2}/\Delta f}{q_{max}^2} \quad \textbf{(8)}$$

where f represents the frequency offset from the carrier. In the case of multiple noise sources, $i_n^2/\Delta f$ represents the total current noise on each node and is given by the power sum of individual sources [5].

In the presence of device $1/f$ noise, the device noise power spectrum, $i_n^2/\Delta f$, has a $1/f$ region in addition to the white noise region, where $f_{1/f}$ is the corner frequency between the two regions.

From (5), it follows that the upconversion of low frequency noise, such as $1/f$ noise, is governed by the DC value of the ISF. The corner frequency between $1/f^2$ and $1/f^3$ regions in the spectrum of the phase noise is called f_{1/f^3} and is related to $f_{1/f}$ through the following equation [5]

$$f_{1/f^3} = f_{1/f} \cdot \frac{\Gamma_{dc}^2}{\Gamma_{rms}^2} \quad \textbf{(9)}$$

where Γ_{dc} is the dc value of the ISF. Since the height of the positive and negative lobes of the ISF are determined by the slope of the rising and falling edges of the output waveform, symmetry of the rising and falling edges can reduce Γ_{dc} and hence the upconversion of $1/f$ noise.

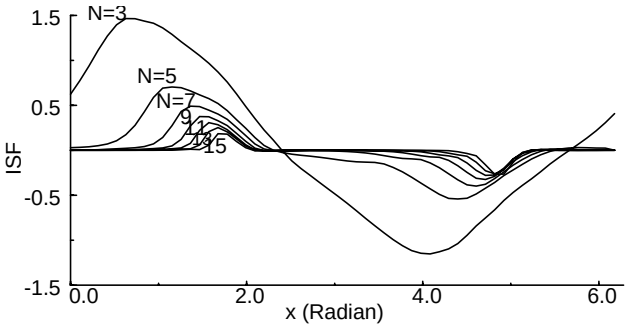

Fig. 3. ISF for CMOS inverter chain ring oscillators with different N.

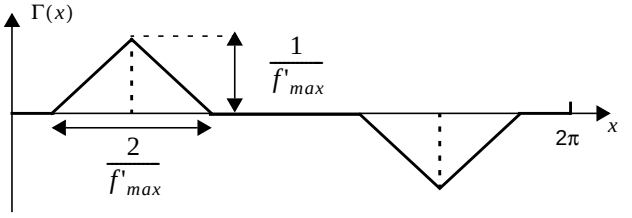

Fig. 4. Approximate ISF for ring oscillators.

Calculation of the ISF for Ring Oscillators

To calculate the phase noise using (5) and (9), one needs to know the RMS value of the ISF. This can always be done by finding the ISF through simulation. However in this section, we obtain a closed-form equation for the RMS value of the ISF of ring oscillators which makes such simulations unnecessary.

To gain insight into the shape of the ISF for ring oscillators, we calculate the ISF for a group of single-ended CMOS ring oscillators in which the frequency of oscillation is kept constant (through adjustment of channel length), while the number of stages is varied from 3 to 15 (odd numbers). To calculate the ISF, a narrow current pulse is injected into one of the nodes of the oscillator and the resulting phase shift is measured a few cycles later. The resulting ISFs are shown in Fig. 3. As can be seen, increasing the number of stages reduces the peak value of the ISF. This is because the normalized waveform has a period of 2π, and therefore the transitions of the normalized waveform become faster for larger N. Since the sensitivity is inversely proportional to the slope, the peak of the ISF drops. Also the widths of the lobes of the ISF decrease as N becomes larger since each transition will occupy a smaller fraction of the period.

To estimate Γ_{rms}, we assume that the ISF is triangular in shape and that its rising and falling edges are symmetric as shown in Fig. 4. The ISF has a maximum of $1/f'_{max}$, where f'_{max} is the maximum slope of the normalized waveform f in (1). Also the width of the triangles is $2/f'_{max}$ and hence the slope of the sides of the triangles is ± 1. Therefore Γ_{rms} is given by

$$\Gamma_{rms}^2 = \frac{1}{2\pi}\int_0^{2\pi}\Gamma^2(x)dx = \frac{4}{2\pi}\int_0^{1/f'_{max}} x^2 dx = \frac{2}{3\pi}\left(\frac{1}{f'_{max}}\right)^3 \quad \textbf{(10)}$$

Stage delay is proportional to the rise time, *i.e.*

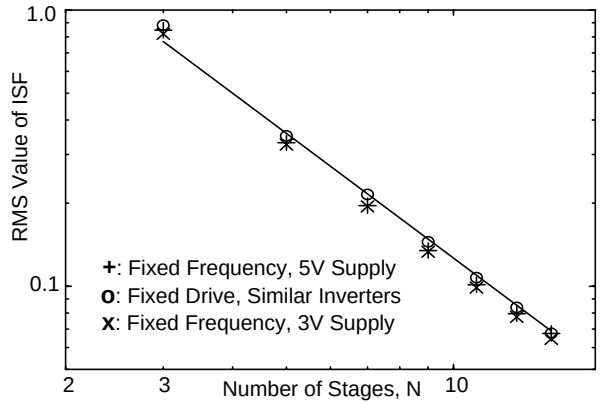

Fig. 5. $\Gamma_{\rm rms}$ vs. number of stages for CMOS inverter chain oscillators.

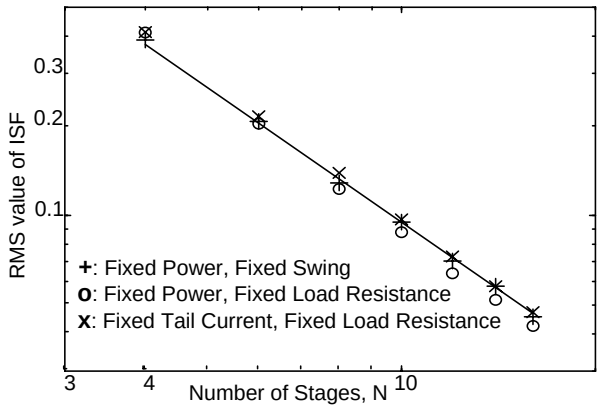

Fig. 6. $\Gamma_{\rm rms}$ vs. number of stages for differential ring oscillators.

$$t_D = \frac{\eta}{f'_{max}} \tag{11}$$

where t_D is the stage delay and η is the proportionality constant, which is typically close to 1. The period is $2N$ times longer than a single stage delay, *i.e.*

$$2\pi = 2Nt_D = \frac{2N\eta}{f'_{max}} \tag{12}$$

Combining (10) and (12), we have

$$\Gamma_{rms} = \sqrt{\frac{2\pi^2}{3\eta^3}} \cdot \frac{1}{N^{1.5}} \tag{13}$$

Note that the $1/N^{1.5}$ dependence of Γ_{rms} is independent of the value of η and is general. Fig. 5 illustrates Γ_{rms} for the ISF shown in Fig. 4 with plus signs on log-log axes. The solid line shows the line of $\Gamma_{rms} \approx 4/N^{1.5}$, which is obtained from (13) for $\eta = 0.75$. To further verify the dependence of this result on other parameters, we maintain a fixed channel length for all the devices in the inverters while the number of stages is varied, and therefore allow different frequencies of oscillation. Again, Γ_{rms} is calculated and shown in Fig. 5 with circles. We also repeat the first experiment with a different power supply (3volts as opposed to 5volts) and the result is shown with crosses. As can be seen, the values of Γ_{rms} are almost identical for these three cases. This confirms that Γ_{rms} is primarily a function of N. This should not be surprising because as discussed earlier, ISF is a unitless, frequency and amplitude independent function.

Equation (13) is valid for differential ring oscillators as well. Figure 6 shows the Γ_{rms} for three sets of differential ring oscillators, with varying number of stages (4, 6, 8, 10, 12, 14 and 16). The first set, shown with plus signs, corresponds to oscillators, in which the total power dissipation and the drain voltage swing are kept constant by scaling the tail current sources and load resistors as N changes. Members of the second set of oscillators have a fixed total power dissipation and fixed load resistors, which results in different swings and is depicted using circles. The third case is that of a fixed tail current for each stage and constant load resistors, which is illustrated using crosses. Again, in spite of the diverse variations of the frequency and other circuit parameters, the $1/N^{1.5}$ dependency of Γ_{rms} and its independence from other circuit parameters still hold. In the case of a differential ring oscillator, $\Gamma_{rms} \approx 3/N^{1.5}$, which corresponds to $\eta = 0.9$, results in a better approximation for Γ_{rms}. This is shown with the solid line in Fig. 6. A similar result can be obtained for bipolar differential ring oscillators.

Although Γ_{rms} decreases as the number of stages increases, one should not prematurely conclude that the phase noise can be reduced using a larger number of stages, because the number of noise sources, as well as their magnitudes, will also increase, for a given total power dissipation and frequency of oscillation.

Limits on the Phase Noise of Differential Ring Oscillators

For CMOS transistors, the channel noise current density is given by

$$\frac{\overline{i_n^2}}{\Delta f} = 4kT\gamma\mu C_{ox}\frac{W}{L}(V_{GS}-V_T) \tag{14}$$

where μ is the mobility, C_{ox} is the gate oxide capacitance per unit area, W and L are the channel width and length of the device,and V_{GS}-V_T is the gate voltage overdrive. The coefficient γ is 2/3 for long channel devices in the saturation region and about 2.5 for short-channel devices.

For a differential MOS ring oscillator, the total power dissipation is

$$P = NI_{tail}V_{dd} \tag{15}$$

where N is the number of stages, I_{tail} is the tail bias current of the differential pair, and V_{dd} is the supply voltage. The frequency of oscillation can be approximated by

$$f_0 \approx \frac{1}{2Nt_r} \approx \frac{I_{tail}}{2Nq_{max}} \tag{16}$$

Only the noise of the transistors forming the differential pair and the load is taken into account. As long as the output resistance of the transistors in the differential pair is large compared to the load, the total current noise on each single-ended node is given by

$$\frac{\overline{i_n^2}}{\Delta f} = \left(\frac{\overline{i_n^2}}{\Delta f}\right)_N + \left(\frac{\overline{i_n^2}}{\Delta f}\right)_{Load} = 4kTI_{tail}\left(\frac{1}{V_{char}} + \frac{1}{\Delta V}\right) \tag{17}$$

where ΔV is the voltage swing across a half circuit and $V_{char} = (V_{GS}-V_T)/\gamma$ for a balanced stage in the long channel regime and $V_{char} = E_cL/\gamma$ in the short channel case, where E_c is the critical field in silicon. The phase noise

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Table 1: Measurement results for differential MOS ring oscillators in a 0.25µm process technology.

N	W/L [µm/µm]	R_L [Ω]	I_{tail} [mA]	P_{tot} [mW]	f_{max} [GHz]	Tuning Range	Limit PN @ 1MHz [dBc/Hz]	Predicted PN @ 1MHz [dBc/Hz]	Measured PN @ 1MHz [dBc/Hz]
4	4.2/0.25	2k	1	10	2.81	34%	-97.5	-94.9	-95.2
4	8.4/0.25	1k	2	20	4.47	42%	-96.0	-94.0	-94.3
4	16.8/0.25	500	4	40	3.89	44%	-100.7	-97.0	-97.4
4	33.6/0.25	250	8	80	5.43	25%	-100.8	-99.2	-98.5
4	8.4/0.25	2k	1	10	2.87	37%	-97.3	-95.9	-93.8
4	16.8/0.25	1k	2	20	3.39	45%	-98.8	-97.2	-96.8
4	33.6/0.25	500	4	40	5.33	32%	-97.9	-96.5	-95.3
4	16.8/0.25	2k	1	10	1.75	73%	-101.6	-97.0	-95.2
4	33.6/0.25	1k	2	20	2.24	58%	-102.5	-100.3	-99.0
4	33.6/0.25	2k	1	10	1.27	67%	-104.4	-101.6	-100.2
4	67.2/0.25	1k	2	20	1.19	76%	-107.9	-102.0	-100.0
4	33.6/0.25	2k	1	10	1.53	N/A	-102.7	-98.1	-97.3
6	13.4/0.25	3k	0.67	10	859	58%	-106.0	-104.6	-104.3
8	6.7/0.25	4k	0.5	10	731	74%	-106.2	-105.7	-106.0
12	4.2/0.25	6k	0.33	10	458	52%	-108.5	-108.4	-108.0

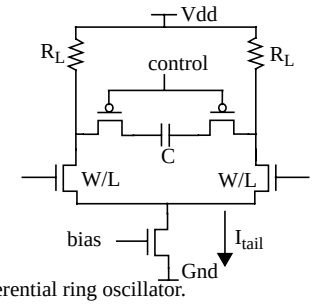

Fig. 7. A differential ring oscillator.

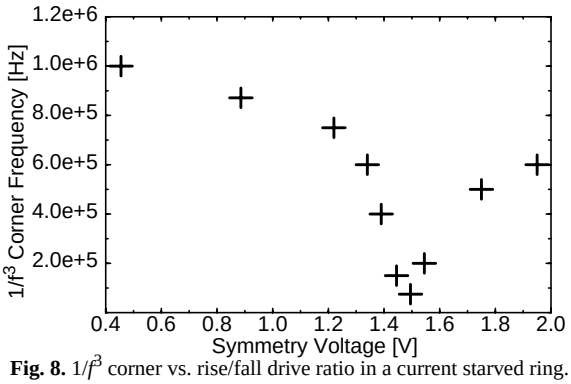

Fig. 8. $1/f^3$ corner vs. rise/fall drive ratio in a current starved ring.

due to all $2N$ noise sources is 2 times the value given by (8). Using $\Gamma_{rms} \approx 3/N^{1.5}$, the lower bound for the phase noise of a differential MOS ring oscillator is

$$L\{\Delta f\} \geq \frac{18}{\pi^2} \cdot \frac{kT}{P} \cdot \left(\frac{V_{dd}}{V_{char}} + \frac{V_{dd}}{\Delta V}\right) \cdot \frac{f_0^2}{\Delta f^2} \cdot N \qquad \textbf{(18)}$$

A similar analysis can be performed for the inverter-chain ring oscillators, and it turns out that unlike the differential case, the phase noise at a given power dissipation and frequency is not a strong function of the number of stages. This result may be understood as a consequence of the necessary reduction in the charge swing that is required to accommodate a constant frequency of oscillation at a fixed power level as N increases. At the same time increasing the number of stages at a given total power dissipation demands a proportional reduction of tail current sources, which will reduce the swing, and hence q_{max}, by a factor of $1/N^2$.

Measurement Results and Conclusion

Fifteen differential ring oscillators were built in a 0.25µ process technology, covering a large span of frequencies up to 5.5GHz. The basic topology of all the ring oscillators in Table 1. is shown in Fig. 7. All the oscillators, except the one marked with N/A, have the tuning circuit shown. The resistors are implemented using an undoped polysilicon layer. The main reason to use poly resistors has been to reduce $1/f$ noise upconversion by making the waveform on each node closer to an ideal RC limited step and hence more symmetrical. The measured phase noise is compared with the predicted value and the lower limit in Table 1. Equations (8) and (13) are used to calculate the predicted phase noise and the limit is obtained from (18). An E_c of $4\text{x}10^6$ V/m and a γ of 2.5 is used in all the above calculations. A very good agreement between the predicted and measured values is observed. It is also noteworthy that the measured and predicted phase noise is always larger than the limit obtained from (18).

In a separate experiment, a current-starved single-stage ring oscillator, which consists of two NMOS and two PMOS devices in series, is implemented in the same process technology. The outer NMOS and PMOS control the pull-down and pull-up currents while the inner devices act as an inverter. The $1/f^3$ corner of the phase noise is measured for different ratios of the pull-up and pull-down currents while keeping the frequency constant. One can observe a sharp reduction in the corner frequency at the point of symmetry in Fig. 8.

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