A 2.125 Gbaud 1.6kΩ Transimpedance Preamplifier in 0.5μm CMOS

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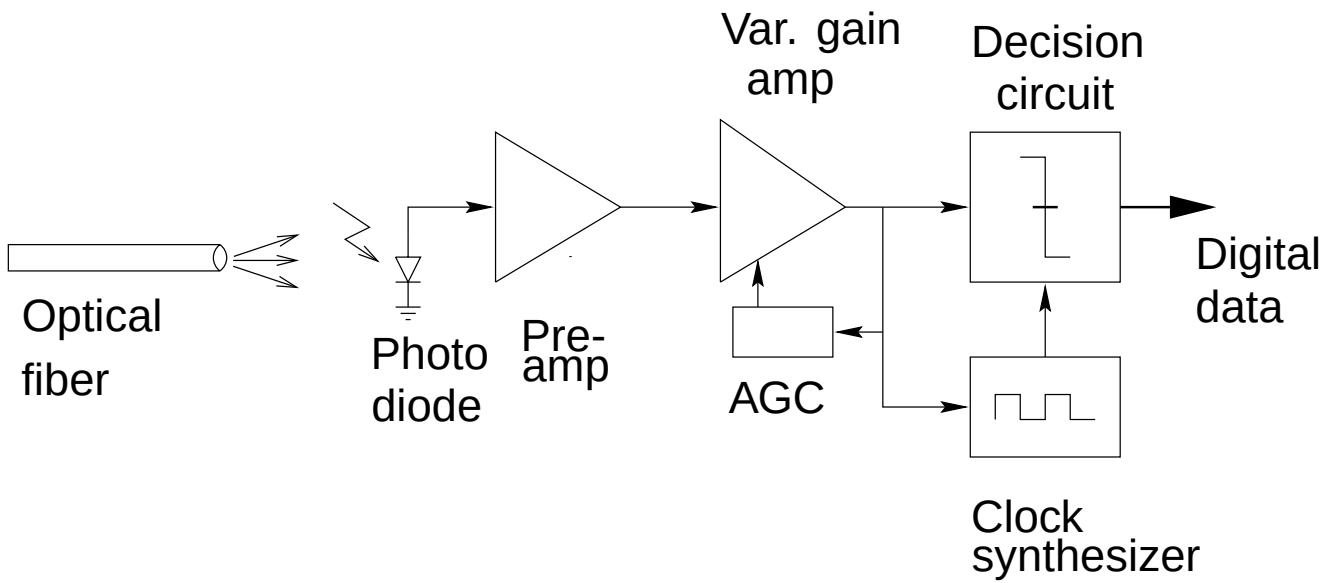
OUTLINE

- Motivation
- Shunt-peaked Amplifier
- Inductor Modeling and Optimization
- Circuit Layout and Measurement
- Summary

SYSTEM OVERVIEW



- Pre-amp design is critical
- Challenge: CMOS implementation

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CMOS vs. GaAs

Factor	GaAs	CMOS
Performance	Excellent	Sufficient for up to low GHz
Integration	Photodiode with Pre-amp	Analog and Digital
Cost	High	Low

- Photodiode in GaAs
- Flip-chip techniques can reduce parasitics at the GaAs to CMOS transition
- Parasitic coupling from digital to analog is a challenge for integration

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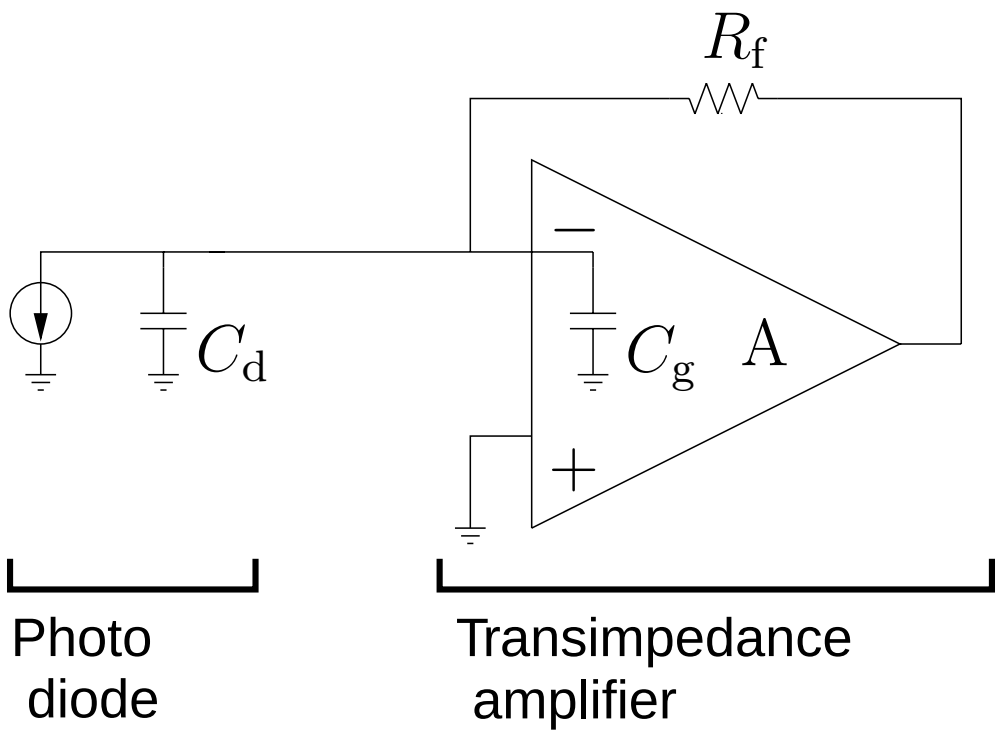
TRANSIMPEDANCE AMPLIFIER



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- $\omega_{3\mathrm{dB}} = \frac{1}{R_{\mathrm{in}}C_{\mathrm{in}}} = \frac{(A+1)}{R_{\mathrm{f}}(C_{\mathrm{d}}+C_{\mathrm{g}})} \approx \frac{A}{R_{\mathrm{f}}(C_{\mathrm{d}}+C_{\mathrm{g}})}$
- $A_{\mathrm{MAX}} = k\frac{\omega_{\mathrm{T}}}{\omega_{3\mathrm{dB}}}$ where ($k \approx 1$)

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TRANSIMPEDANCE LIMIT

- $R_{\mathrm{f,MAX}} \approx \frac{k\omega_{\mathrm{T}}}{\omega_{\mathrm{3dB}}{}^{2}(C_{\mathrm{d}}+C_{\mathrm{g}})}$
- Desire maximum R_{f} for sensitivity, stability and high gain
- Need to circumvent this limit

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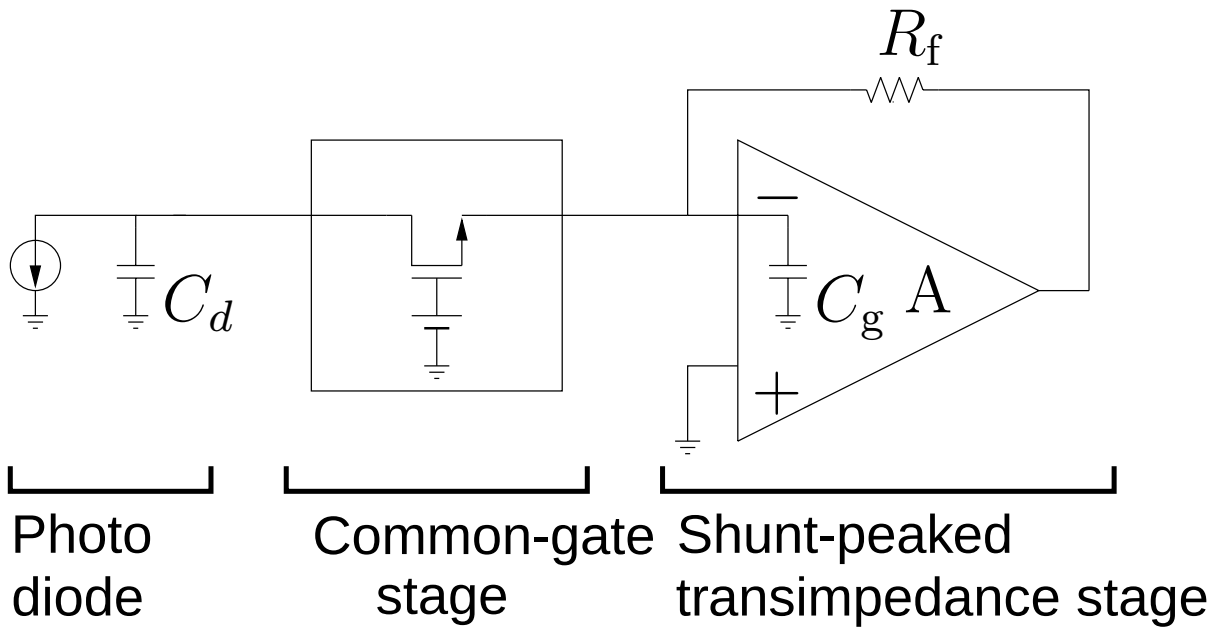
CIRCUMVENTING THE TRANSIMPEDANCE LIMIT



- Decouple photodiode from the transimpedance stage with common-gate stage
- Increase gain-bandwidth product by shunt-peaking

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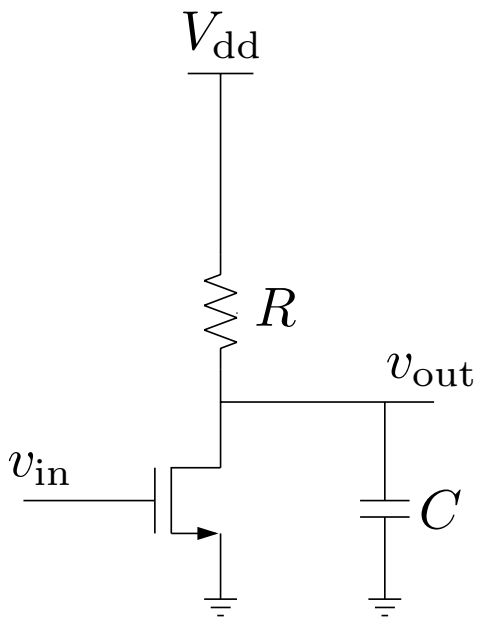
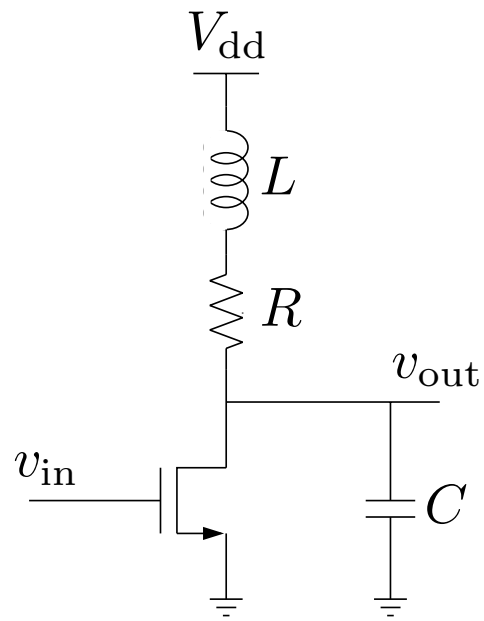
SHUNT-PEAKED AMPLIFIER

Common Source Amplifier



Shunt-peaked Amplifier



- Bandwidth enhancement using zeros
- No additional power dissipation

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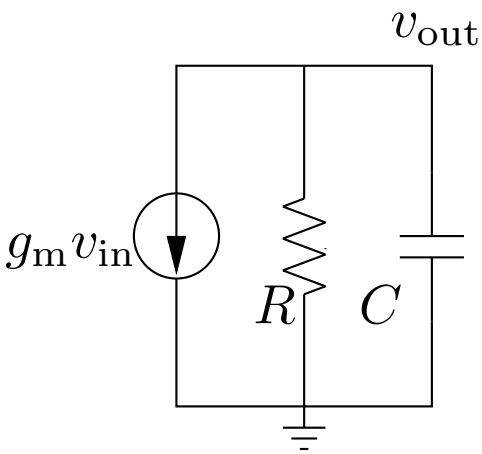
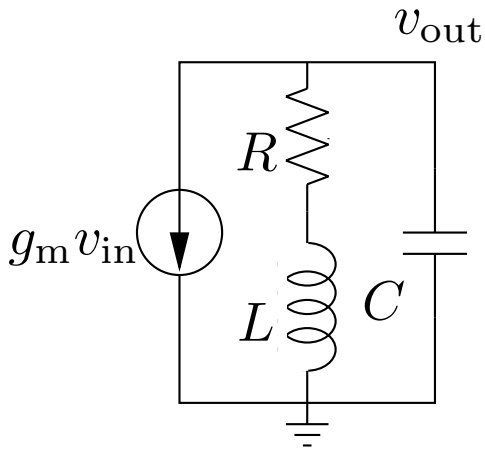
SMALL SIGNAL MODELS

Common Source Amplifier



- One pole
- $\frac{v_{\mathrm{out}}}{v_{\mathrm{in}}}(\omega) = \frac{g_{\mathrm{m}} R}{1+j\omega RC}$

Shunt-peaked Amplifier



- One zero, two poles
- $\frac{v_{\mathrm{out}}}{v_{\mathrm{in}}}(\omega) = \frac{g_{\mathrm{m}}(R+j\omega L)}{1+j\omega RC-\omega^2 LC}$

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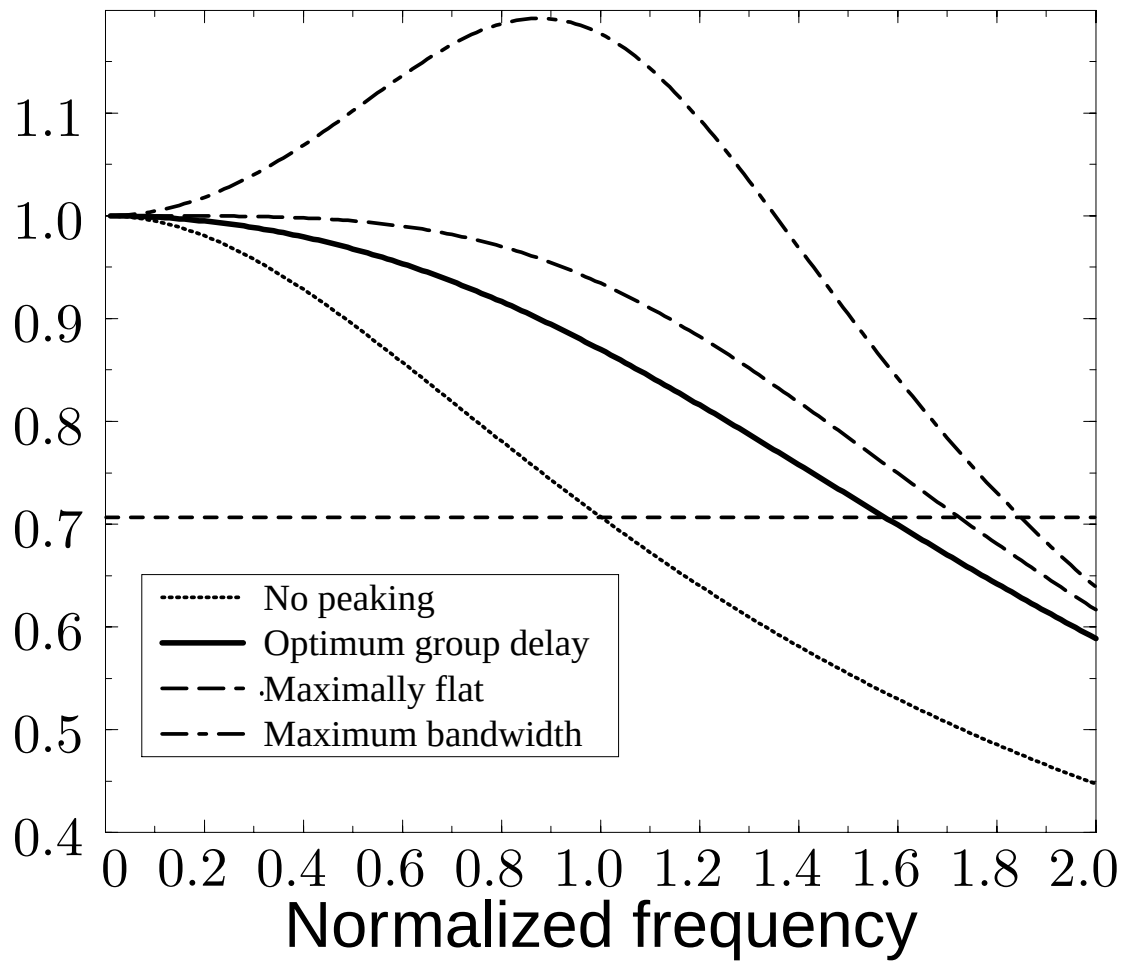
MAGNITUDE RESPONSE



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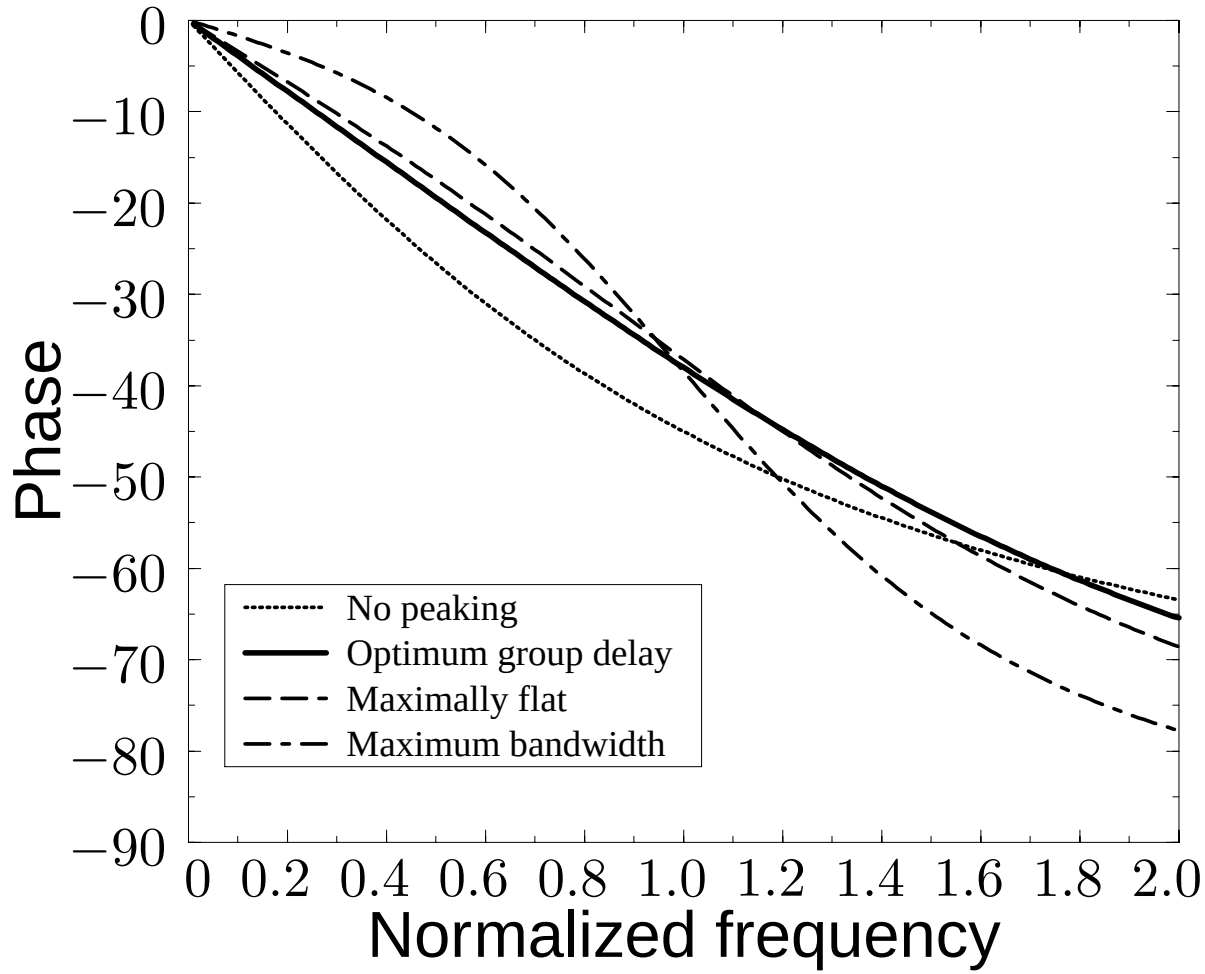
PHASE RESPONSE



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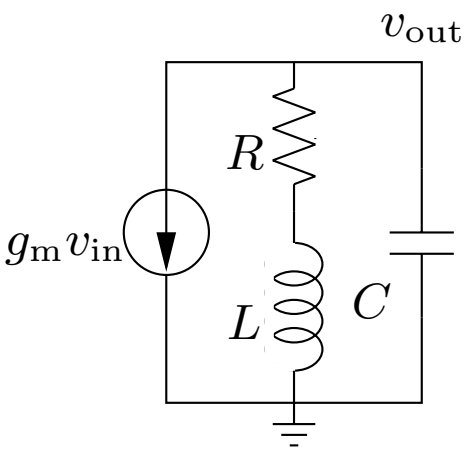
Frequency Response



- Two time constants:
  $\tau_{\mathrm{C}} = RC, \tau_{\mathrm{L}} = L/R$
- Ratio determines performance:
  $m = \frac{\tau_{\mathrm{L}}}{\tau_{\mathrm{C}}} = \frac{L}{R^2 C}$

Factor (m)	**Normalized $\omega_{3\mathrm{dB}}$**	**Response**
0	1.00	No shunt peaking
0.32	1.60	Optimum group delay
0.41	1.72	Maximally flat
0.71	1.85	Maximum bandwidth

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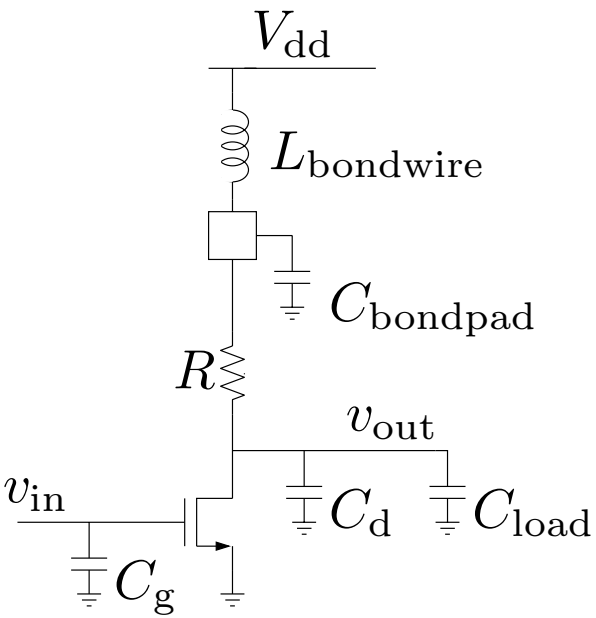
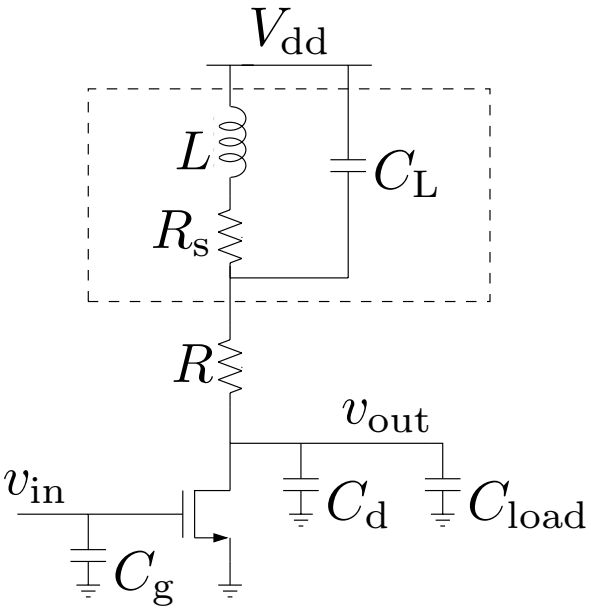
On-chip Shunt Peaking : Previous Work

Bond-wire inductor



- Large C_{bondpad}
- Limited L_{bondwire}
- Coupling issues

Maximum Q on-chip



- Large C_{L}
- Large area
- Limited L

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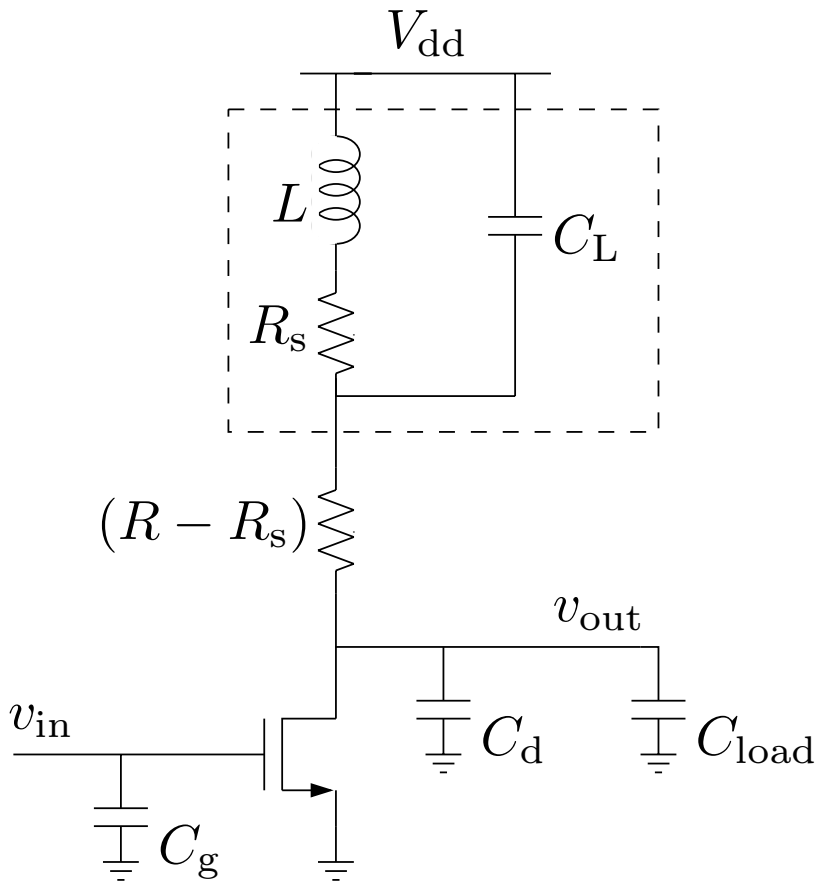
On-chip Shunt Peaking: NEW



- Work with inductor parasitics
- R_{s} is **not** an issue (now part of load resistance)
- Inductor Q is **not** relevant
- Minimize area and C_{L}
- L determined by R, C_{load}, C_{L} and C_{d}

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MODELING CHALLENGE

- **Simultaneous optimization** of active **and** passive components
- 3-D field solvers are **inconvenient**
  - { Numerically expensive and cumbersome
  - { Good for **verification** but not for **design**
- **Scalable, analytical models**
  - { Design **guidelines** and explore **trade-offs**
  - { Circuit **design** and **optimization**

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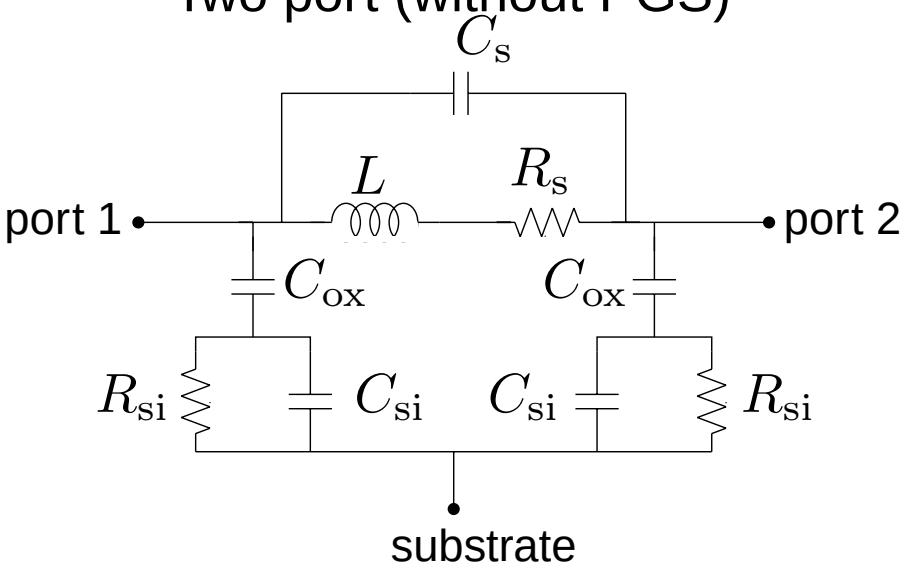
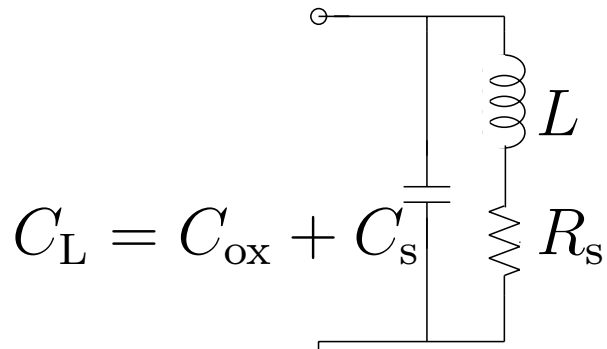
INDUCTOR MODELING

Two port (without PGS)





One port (with PGS)

- Simple expressions for R_s, C_{ox} and C_s
- Patterned ground shield (PGS) eliminates R_{si} and C_{si}
- **NEED** simple, accurate expression for inductance!

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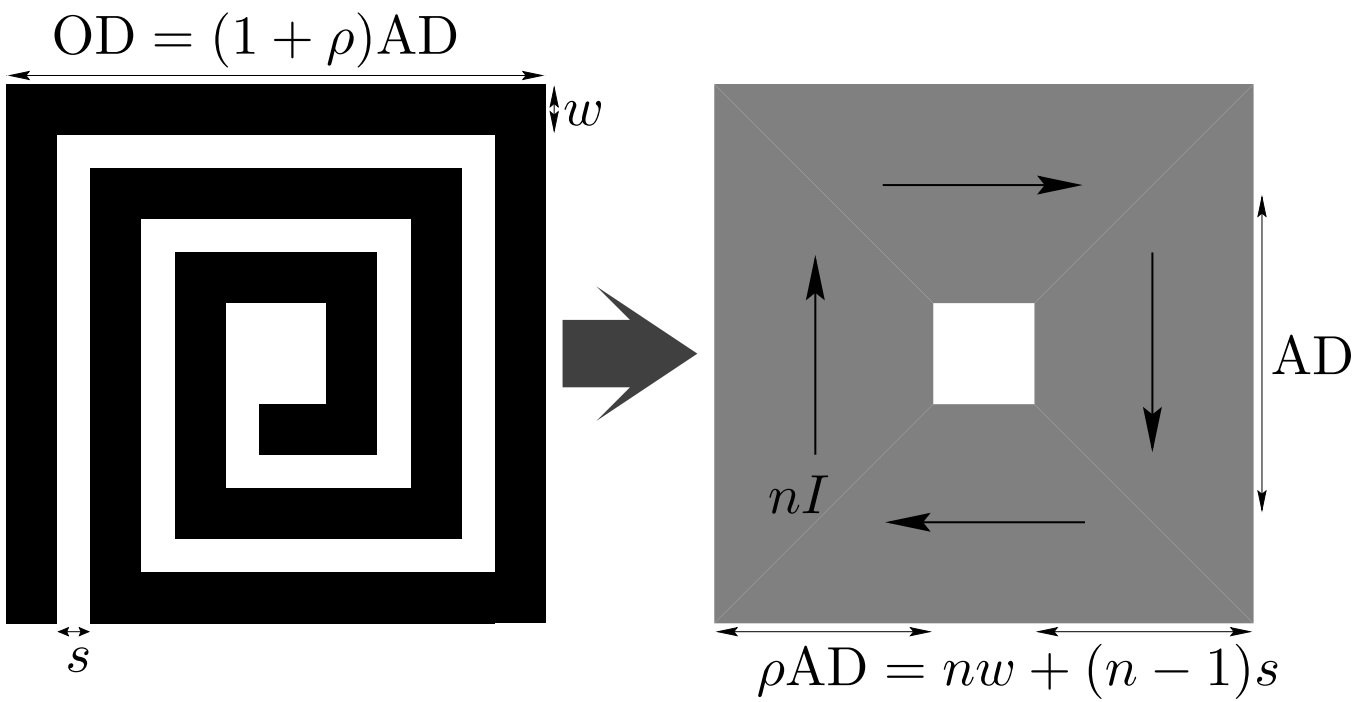
Current Sheet Approach



- Reduce complexity by $4n^2$
- Use symmetry
- Derive simple expression using GMD, AMD and AMSD

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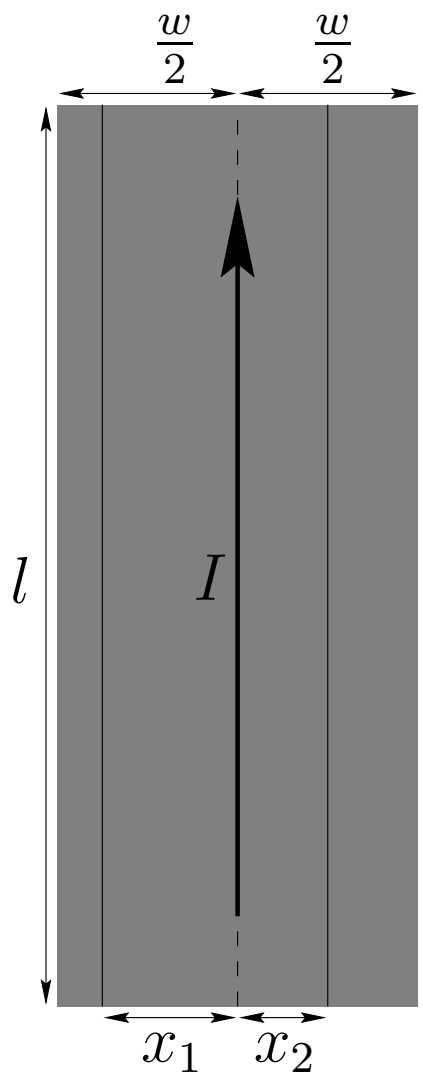
GMD, AMD AND AMSD



$$-\frac{w}{2} < x_1, x_2 < \frac{w}{2}$$

$$\begin{aligned}
\ln(\mathrm{GMD}) &= \overline{\ln|x_1 + x_2|} &&= \ln w - 1.5 \\
\mathrm{AMD} &= \overline{|x_1 + x_2|} &&= \frac{w}{3} \\
\mathrm{AMSD}^2 &= \overline{(x_1 + x_2)^2} &&= \frac{w^2}{6}
\end{aligned}$$

$$\begin{aligned}
L &= \tfrac{\mu l}{2\pi}\left[\ln\left(\tfrac{2l}{\mathrm{GMD}}\right) - 1 + \tfrac{\mathrm{AMD}}{l} - \tfrac{\mathrm{AMSD}^2}{4l^2}\right] \\
&= \tfrac{\mu l}{2\pi}\left[\ln\left(\tfrac{2l}{w}\right) + 0.5 + \tfrac{w}{3l} - \tfrac{w^2}{24l^2}\right]
\end{aligned}$$

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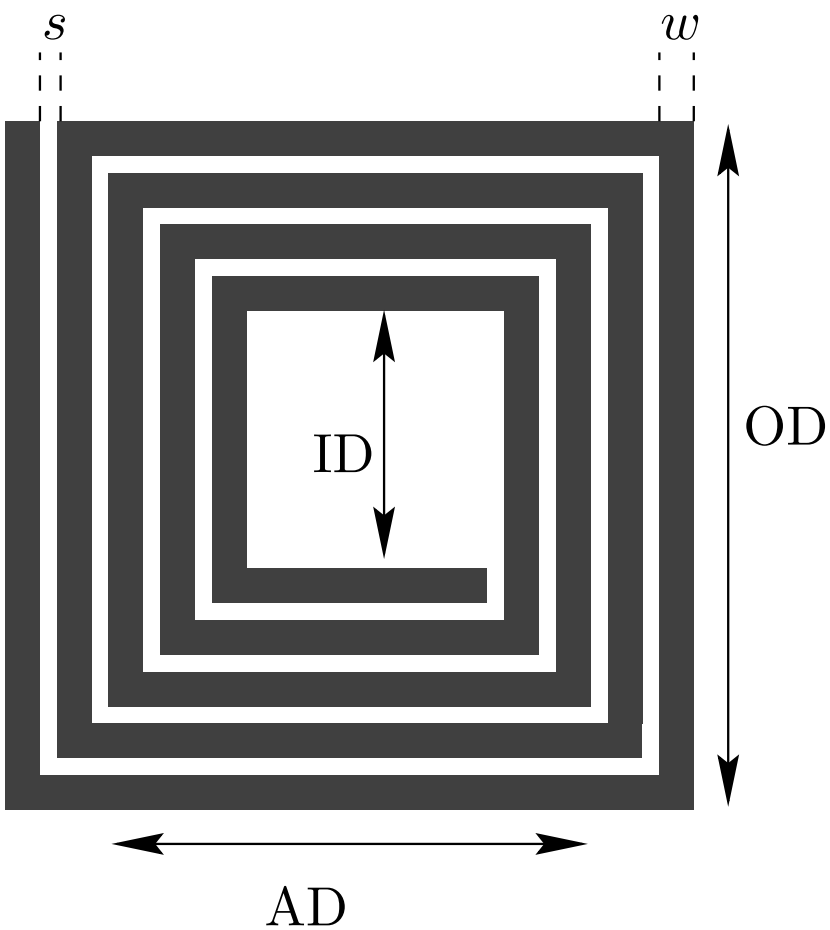
Inductance Expresssion



- $\mathrm{AD} = 0.5(\mathrm{OD} + \mathrm{ID})$
- $\rho = \frac{\mathrm{OD}-\mathrm{ID}}{\mathrm{OD}+\mathrm{ID}}$
- $\rho\mathrm{AD} = nw + (n-1)s$

- $L = \frac{2\mu n^2 \mathrm{AD}}{\pi}\left[\ln\left(\frac{2.067}{\rho}\right) + 0.176\rho + 0.125\rho^2\right]$

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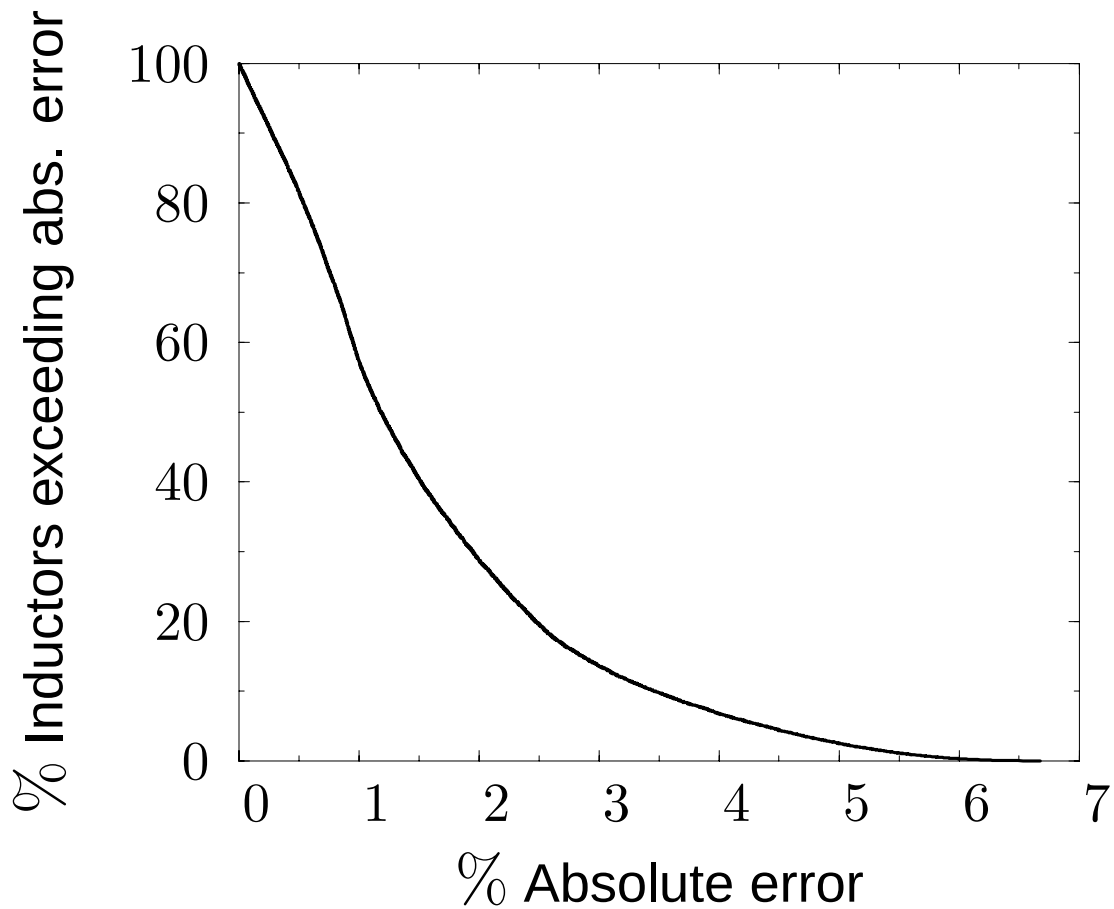
INDUCTANCE EXPRESSSION



	Min	Max
$L(\mathrm{nH})$	0.1	70
$\mathrm{OD}(\mu\mathrm{m})$	100	400
n	1	20
s/w	0.02	3
ρ	0.03	0.95

Verified by measurements (75) and 3-D field solver simulations (19,000)

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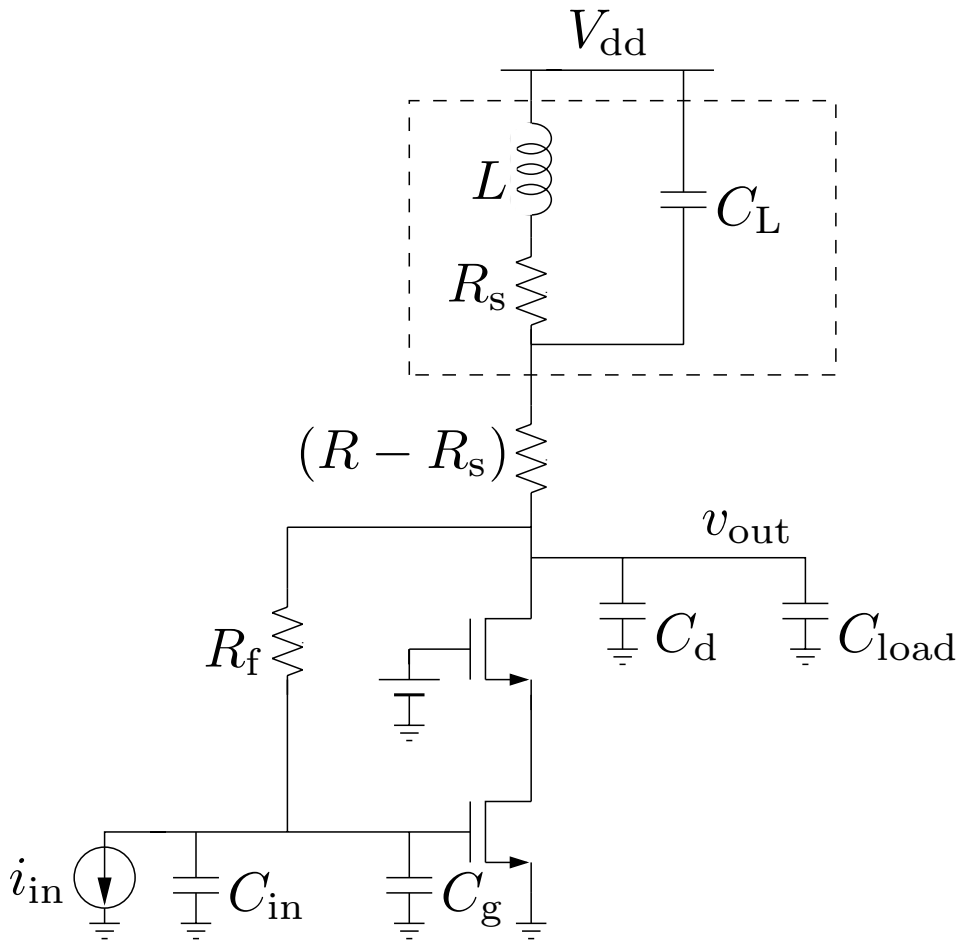
TRANSIMPEDANCE STAGE



- Input current drive
- Cascode stage
- On-chip shunt-peaking
- Feedback

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Design Methodology

1. Design and optimize transimpedance stage without shunt peaking
2. Transistor current determines conductor width, w
3. Lithography sets spacing, s
4. Choose n and AD to realize desired L while minimizing parasitic capacitance and area
5. Increase transimpedance resistance, R_{f}

Optimization via Geometric Programming

- **Simultaneous optimization** of active **and** passive components
- **Global Optimum** or **Proof of Infeasibility**

DAC99, Session 54.3 *(June 24, 1999):*

Optimization of Inductor Circuits via Geometric Programming

Maria del Mar Hershenson, Sunderarajan S. Mohan

Stephen P. Boyd and Thomas H. Lee

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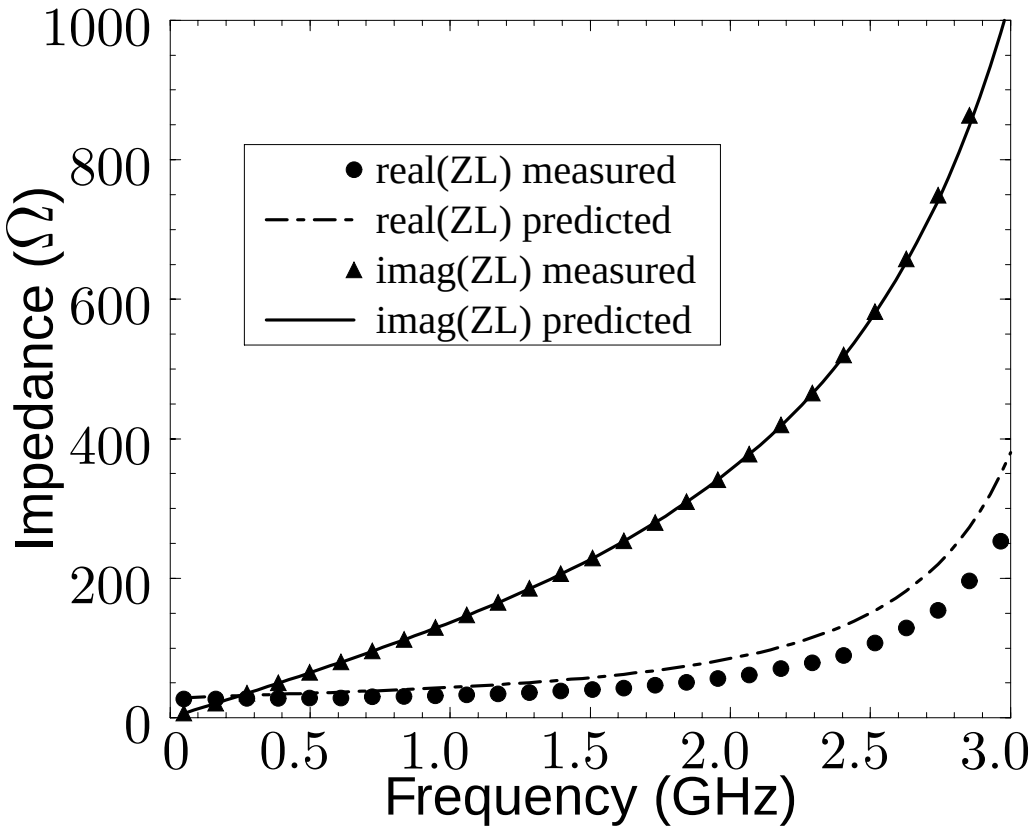
Experimental Verification of Inductor



- OD $= 180\mu m$
- $w = 3.2\mu m$
- $s = 2.1\mu m$
- $n = 11.75$
- $L_{\text{meas}} = 20.5\text{nH}$
- $L_{\text{pred}} = 20.3\text{nH}$

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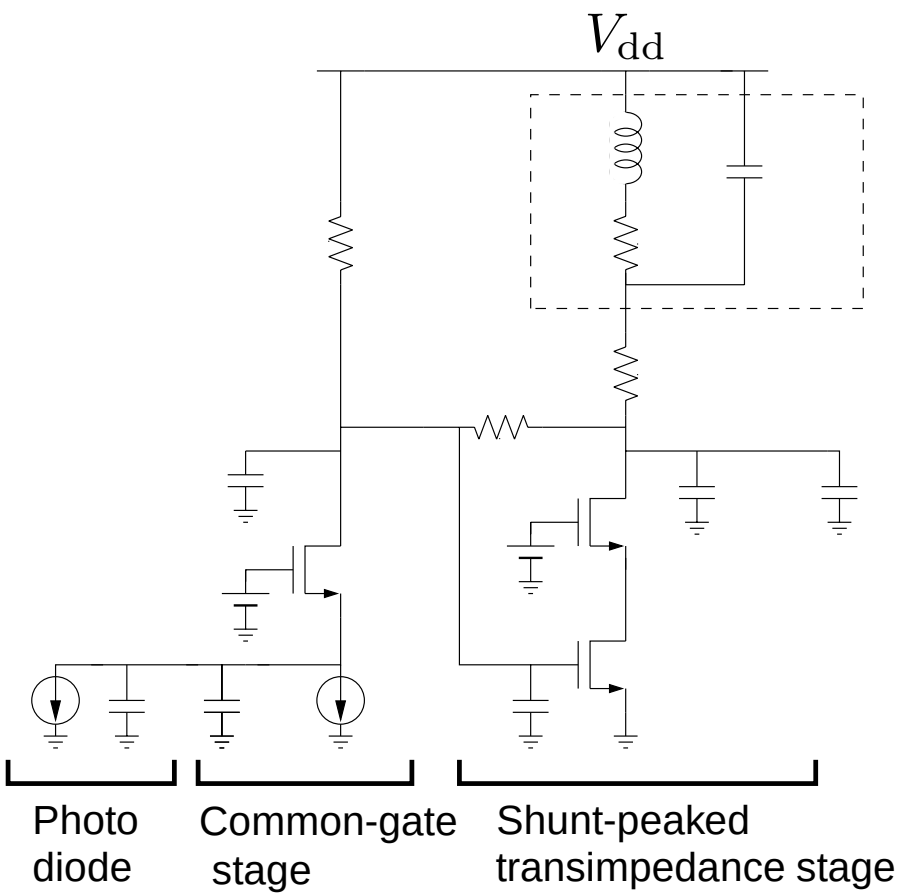
COMMON-GATE STAGE



- Decouple sensitive feedback node from external capacitances
- Realize higher transimpedance
- Extra power
- Additional noise terms
- Junction capacitances degrade noise at high frequency

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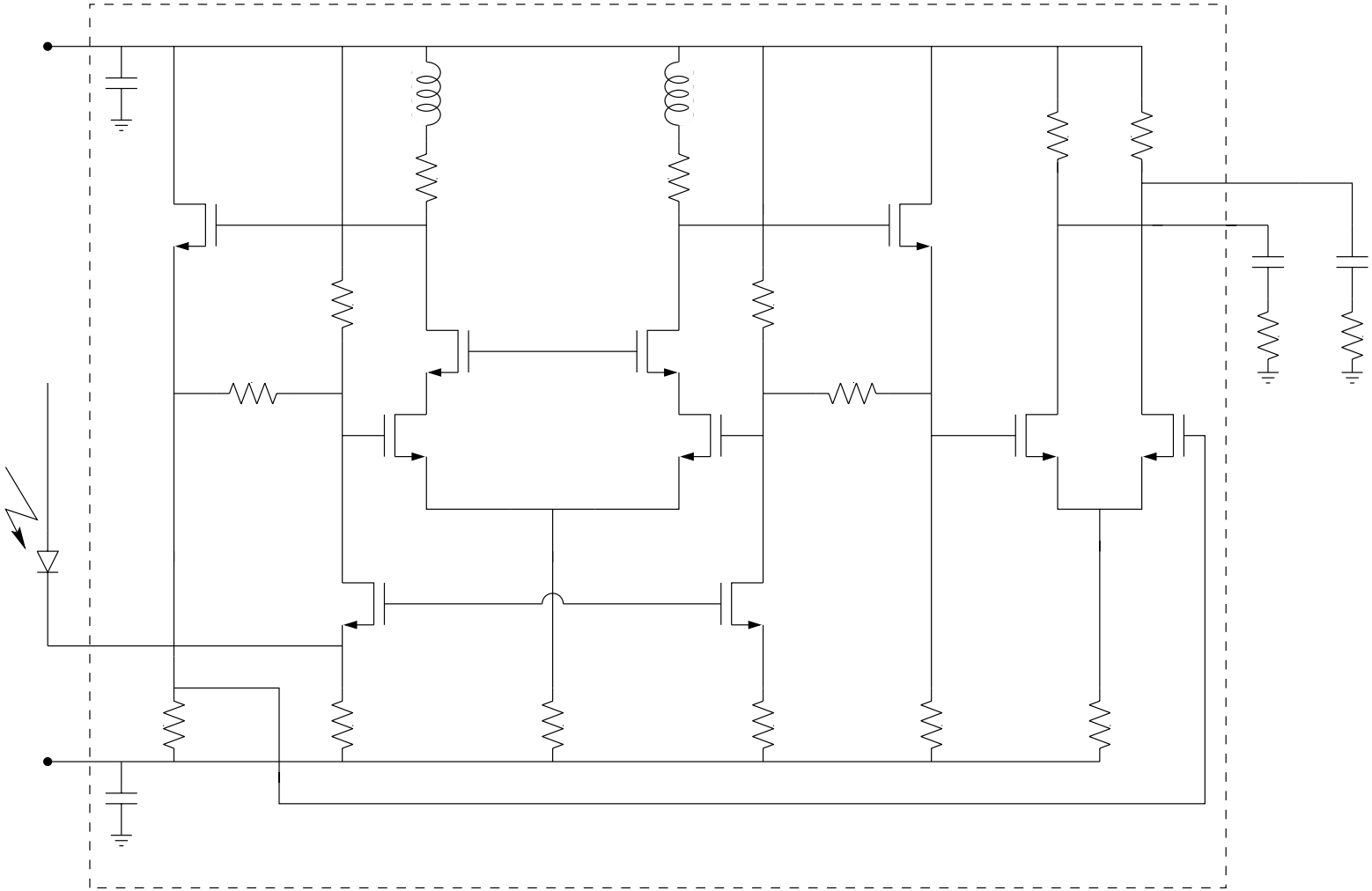
Differential Preamplifier



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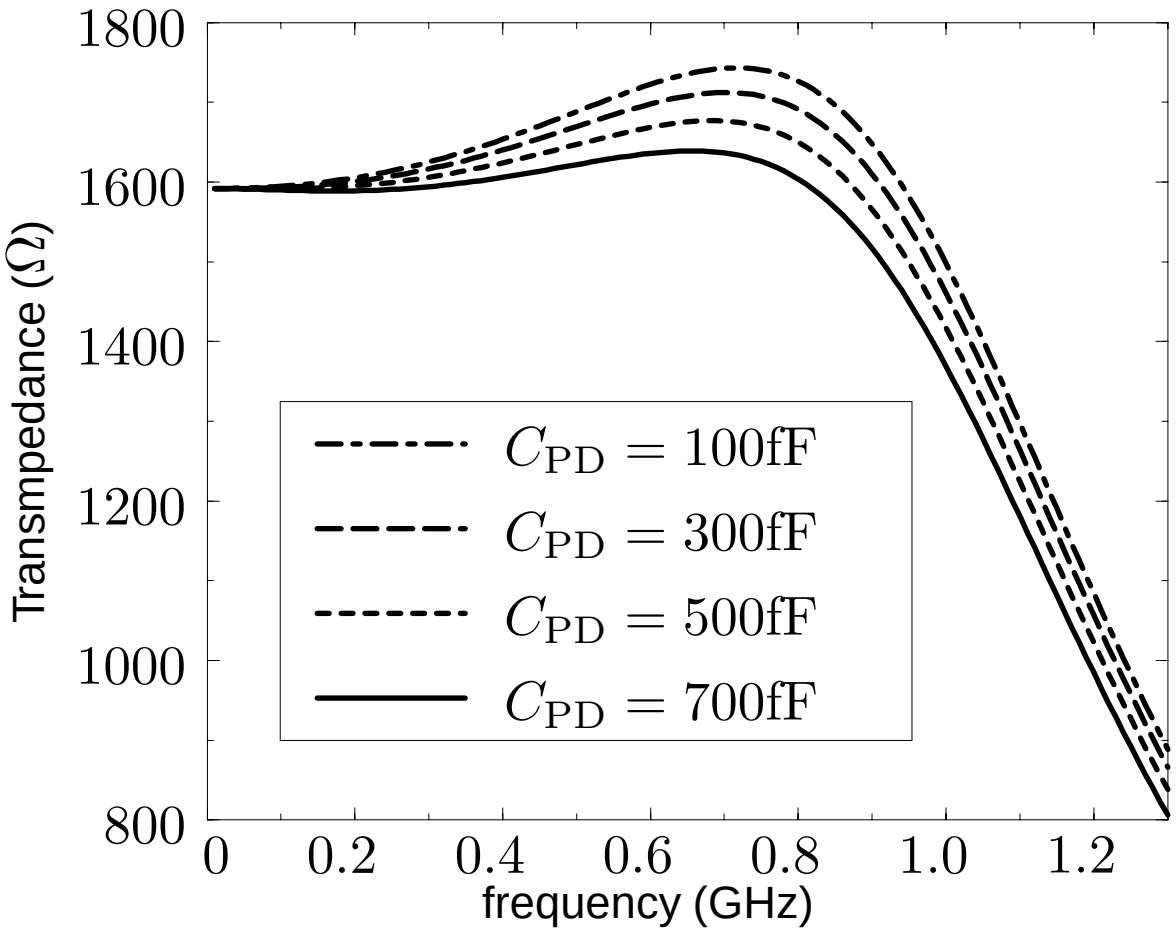
TRANSIMPEDANCE BANDWIDTH



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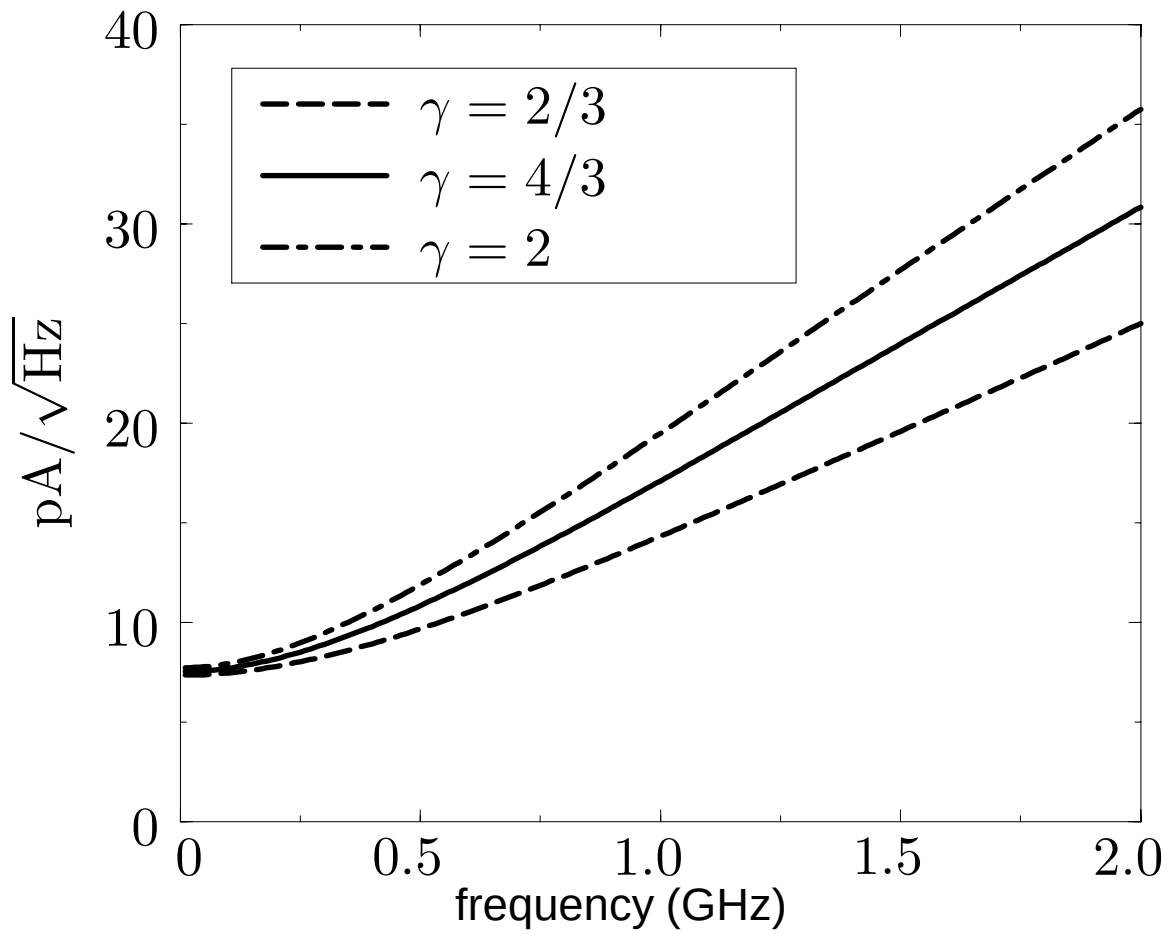
Input Referred Current Noise Density



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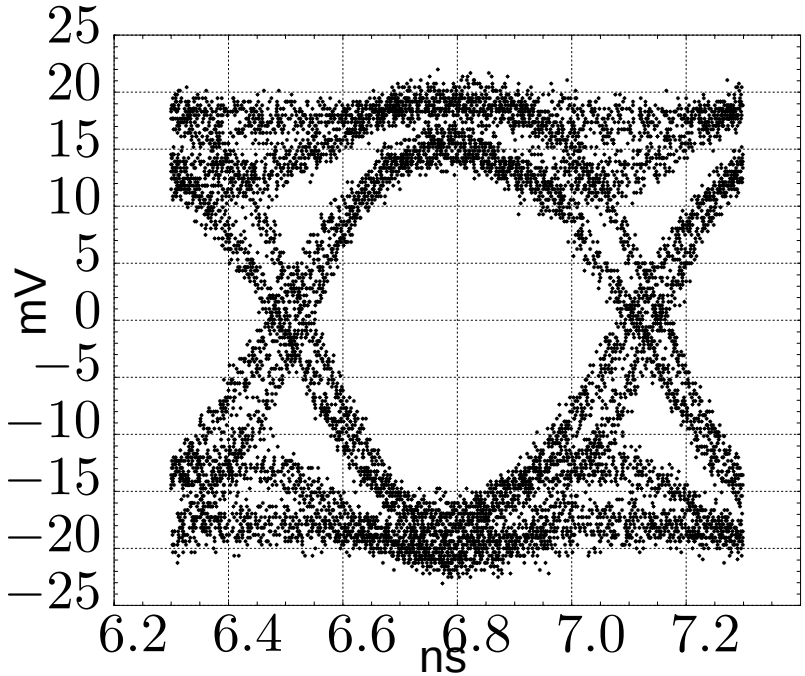
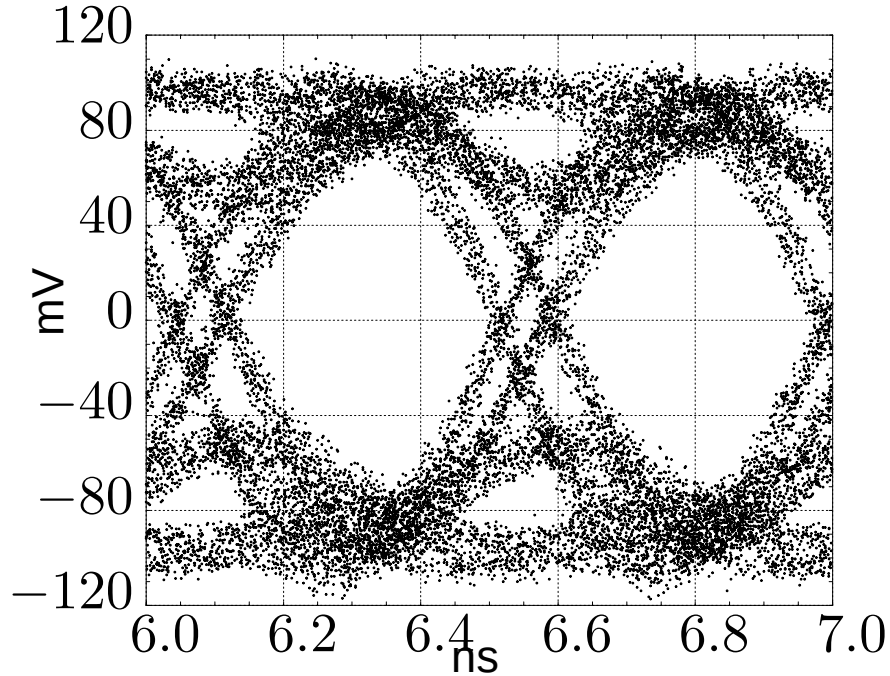
EYE DIAGRAM

1.6 Gb/s



2.1 Gb/s



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PERFORMANCE SUMMARY

Transimpedance (small-signal)	1600Ω (differential)
	800Ω (single-ended)
Bandwidth ($3\mathrm{dB}$)	$1.2\mathrm{GHz}$
Max. photodiode capacitance	$0.6\mathrm{pF}$
Max. input current	$1.0\mathrm{mA}$
Simulated input noise current	$0.6\mu\mathrm{A}$
Max. output voltage swing	$1.0\mathrm{V_{pp}}$ (differential)
(50Ω load at each output)	$0.5\mathrm{V_{pp}}$ (single-ended)
Power consumption	$115\mathrm{mW}$ (core)
	$110\mathrm{mW}$ (50Ω driver)
Die area	$0.6\mathrm{mm}^2$
Technology	$0.5\mu\mathrm{m}$ CMOS

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CONTRIBUTIONS

- Shunt-peaking with optimized on-chip inductor
- Simple accurate expression for inductance
- Common-gate input stage
- CMOS implementation of differential preamplifier

ACKNOWLEDGMENTS

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