Optimization of Inductor Circuits via Geometric Programming

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Abstract

We present an efficient method for optimal design and synthesis of CMOS inductors for use in RF circuits. This method uses the the physical dimensions of the inductor as the design parameters and handles a variety of specifications including fixed value of inductance, minimum self-resonant frequency, minimum quality factor, etc. Geometric constraints that can be handled include maximum and minimum values for every design parameter and a limit on total area.

Our method is based on formulating the design problem as a special type of optimization problem called *geometric programming*, for which powerful efficient interior-point methods have recently been developed. This allows us to solve the inductor synthesis problem *globally* and *extremely efficiently*. Also, we can rapidly compute globally optimal trade-off curves between competing objectives such as quality factor and total inductor area.

We have fabricated a number of inductors designed by the method, and found good agreement between the experimental data and the specifications predicted by our method.

1 Introduction

The rising demand for low-cost radio-frequency integrated circuits (RF-ICs) has generated tremendous interest in on-chip spiral inductors. The parasitic resistances and capacitances associated with these spiral inductors result in several engineering tradeoffs. Unfortunately, no inductor optimization tools exist to aid in circuit design. Currently, most designers are limited to using a library of previously fabricated inductors or generating a large database of inductors using a 3-D field solver. While the former option severely constrains the available design space, the latter one requires a sophisticated search engine, a large computational effort, and the generation of a new library when process parameters change. Moreover, any inductor optimization based on these approaches requires a good starting point and numerous iterations to arrive at an acceptable design. This iterative process is time consuming and inconvenient for obtaining globally optimal designs, determining infeasibility and exploring trade offs. Another drawback is that neither approach is amenable to the application dependent nature of inductor design. For example, while a resonator may require an inductor with high parallel impedance, a shunt-peaked amplifier would require one with low capacitance. The optimal layout of these inductors is determined by related, but somewhat different design goals.

In this paper, we propose a simple and efficient CAD tool for designing on-chip spiral inductors for use in a variety of RF circuits. The tool is based on geometric programming (§2), a special type of optimization problem for which very efficient global optimization methods have been developed. It uses a simple and well accepted inductor model [1], whose elements are given by special expressions that are compatible with geometric programming (§3). In §4, we show how the design specifications of inductor circuits can be formulated in a way suitable for geometric programming. In §5-§8, we give some examples of our approach. Experimental verification and a summary of our results are given in §9.

The method is *global*, meaning that it finds the absolute best design possible, when the specifications are feasible, and unambiguously determines infeasibility when the specifications are infeasible. The method is also very fast and provides valuable information on the sensitivity of the objective to the constraints, permitting the RF CMOS designer to spend more time exploring the fundamental design tradeoffs instead of ad-hoc parameter tuning.

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2 Geometric programming (GP)

Let f be a real-valued function of n real, positive variables $x_1, \ldots, x_n$. It is called a *posynomial* function if it has the form

$$f(x_1, \ldots, x_n) = \sum_{k=1}^{t} c_k x_1^{\alpha_{1k}} x_2^{\alpha_{2k}} \cdots x_n^{\alpha_{nk}}$$

where $c_j \geq 0$ and $\alpha_{ij} \in \mathbf{R}$. When $t = 1$, f is called a *monomial* function. Thus, for example, $0.7 + 2x_1/x_3^2 + x_2^{0.3}$ is posynomial and $2.3(x_1/x_2)^{1.5}$ is a monomial. Posynomials are closed under sums, products, and nonnegative scaling.

A *geometric program* (GP)) has the form

$$\begin{array}{ll} \text{minimize} & f_0(x) \\ \text{subject to} & f_i(x) \leq 1, \quad i = 1, 2, \ldots, m, \\ & g_i(x) = 1, \quad i = 1, 2, \ldots, p, \\ & x_i > 0, \quad i = 1, 2, \ldots, n, \end{array} \tag{1}$$

where f_i are posynomial functions and g_i are monomial functions. If f is a posynomial and g is a monomial, then the constraint $f(x) \leq g(x)$ can be expressed as $f(x)/g(x) \leq 1$ (since f/g is posynomial). From closure under non-negativity, constraints of the form $f(x) \leq a$, where $a > 0$ can also be used. Similarly, if g_1 and g_2 are both monomial functions, the constraint $g_1(x) = g_2(x)$ can be expressed as $g_1(x)/g_2(x) = 1$ (since g_1/g_2 is monomial).

For our purposes, the most important feature of geometric programs is that they can be *globally* solved with great efficiency. GP solution algorithms also determine whether the problem is infeasible. Also, the starting point for the optimization algorithm does not have any effect on the final solution; indeed, a starting point or initial design is completely unnecessary.

To carry out the designs described in this paper we used a very simple (primal barrier) method for solving the convex form of a

GP. Despite the simplicity of the method, and our inefficient implementation, all the design problems in this paper were solved in well under one second, on a simple personal computer.

3 Planar spiral inductors

3.1 Layout variables for optimization

Figure 1 shows the layout of a square planar inductor. The inductor can be implemented with or without a patterned ground shield (PGS) [3] (a grounded polysilicon shield broken regularly in the direction perpendicular to the current flow of the inductor).

The optimization variables that characterize the inductor geometry are number of turns n, the turn width w, the turn spacing s, the outer diameter d_{out} and the average diameter $d_{\text{avg}} = 0.5(d_{\text{out}} + d_{\text{in}})$. These five variables are not independent, but it will be convenient to consider this (redundant) set of variables. We also note that the design variables are discrete; w, s and d_{out} are restricted to take values on a discrete grid while the number of turns n is restricted to take values that are integer multiples of 0.25 (quarter turns). In the rest of the paper, we ignore these grid constraints and consider the variables to be continuous. The final inductor design is then obtained via rounding to the nearest grid point. In every design we have carried out, this step has caused no significant error.

Other geometry parameters of interest that can be expressed as monomial functions of the design variables include the inductor length $l = 4nd_{\text{avg}}$, and the inductor area $A = d_{\text{out}}^2$.

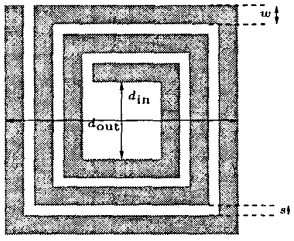

Figure 1: Square inductor layout and geometry.

3.2 Lumped electrical model

The CAD tool presented is based on a simple two port lumped model shown in Figure 2(a) (see [1]). The results are accurate as long as the assumption of a lumped model is valid (see [4]). In this section, we give simple and accurate expressions for the model elements (see [1, 3, 5] for more detail). Each element is a posynomial function of the design variables and a factor k_i that is dependent on technology and frequency.

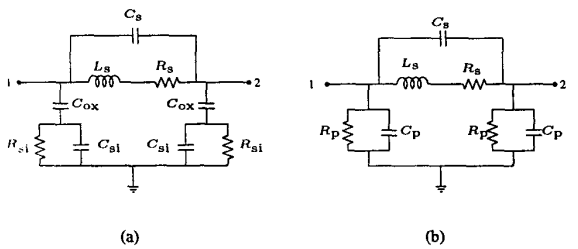

Figure 2: Inductor model: (a) Π model, (b) simplified model.

Inductance L_s. An accurate monomial expression for the inductance can be found in [5] and has the form

$$L_s = \beta d_{\text{out}}^{\alpha_1} w^{\alpha_2} d_{\text{avg}}^{\alpha_3} n^{\alpha_4} s^{\alpha_5}, \tag{2}$$

with inductance in nH and dimensions in μm and where the coefficients β and α_i are only layout dependent and do not depend on the technology. With coefficients $\beta = 1.66 \cdot 10^{-3}$, $\alpha_1 = -1.33$, $\alpha_2 = -0.125$, $\alpha_3 = 2.50$, $\alpha_4 = 1.83$, $\alpha_5 = -0.022$, this expression gives an accurate fit of the inductance as calculated from field solver computations and experimental data with a typical error of a few percent over a very broad design space.

Series resistance R_s. The series resistance is given by the monomial expression

$$R_s = l/(\sigma w \delta(1 - e^{-t/\delta})) = k_1 l/w, \tag{3}$$

where σ is the conductivity, t is the turn thickness and δ is the skin depth. The skin depth is given by $\delta = \sqrt{2/(\omega\mu_o\sigma)}$, where ω is the frequency and $\mu = 4\pi 10^{-7}$H/m is the magnetic permeability of free space.

Spiral-substrate oxide capacitance C_{ox}. The spiral-substrate oxide capacitance accounts for most of the inductor's parasitic capacitance. It can be approximated by the monomial expression

$$C_{ox} = (\epsilon_{ox} l w)/(2t_{ox}) = k_2 l w, \tag{4}$$

where $\epsilon_{ox} = 3.4510^{-13}$F/cm is the oxide permitivity and t_{ox} is the oxide thickness between the spiral and the substrate.

Series capacitance C_s. This capacitance is mainly due to the capacitance between the spiral and the metal under-pass required to connect the inner end of the spiral inductor to external circuitry. It is modeled by the monomial expression

$$C_s = (\epsilon_{ox} n w^2)/(t_{ox,M1-M2}) = k_3 n w^2, \tag{5}$$

where $t_{ox,M1-M2}$ is the oxide thickness between the the spiral and the under-pass.

Substrate capacitance C_{si}. The substrate capacitance is given by the monomial expression

$$C_{si} = (C_{sub} l w)/2 = k_4 l w, \tag{6}$$

where C_{sub} is the substrate capacitance per unit area.

Substrate resistance R_{si}. The substrate resistance can be expressed as the monomial

$$R_{si} = 2/(G_{sub} l w) = k_5/(l w), \tag{7}$$

where G_{sub} is the substrate conductance per unit area.

An equivalent inductor model is shown in Figure 2(b). The elements R_p and C_p, which are frequency dependent, have the following expressions:

Shunt resistance R_p. The shunt resistance is given by the monomial expression,

$$R_p = \frac{1 + [\omega R_{si}(C_{si} + C_{ox})]^2}{\omega^2 R_{si} C_{ox}^2} = k_6/(l w). \tag{8}$$

Shunt capacitance C_p. The shunt capacitance is given by the posynomial expression,

$$C_p = \frac{C_{ox} + \omega^2 R_{si}(C_{si} + C_{ox}) C_{si} C_{ox}}{1 + [\omega R_{si}(C_{si} + C_{ox})]^2} = k_7 l w + k_8 (l w)^2. \tag{9}$$

3.2.1 Lumped model for inductors with PGS

In some cases, the placement of a PGS beneath the inductor improves performance by eliminating the resistive and capacitive coupling to the substrate at the expense of the increased oxide capacitance. With a PGS the expressions for C_{ox}, R_p and C_p, become:

$$R_p = \infty, \quad C_p = C_{ox} = (\epsilon_{ox} l w)/(2t_{ox,po}),$$

where $t_{ox,po}$ is the oxide thickness between the spiral and the polysilicon layer.

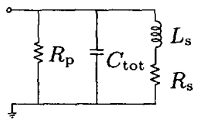

Figure 3: One-port small signal grounded inductor model.

3.2.2 Lumped model for one-port inductors

When the inductor is used as a one-port device, the simplified model shown in Figure 3 can be used. The total shunt capacitance, $C_{tot} = C_s + C_p$, is posynomial since both C_s and C_p are given by monomial expressions.

4 Constraints and specifications for inductor design

In this section we show how a variety of design specifications for inductors can be expressed as either monomial equality constraints, or posynomial inequality constraints, and therefore can be handled by geometric programming.

Constraints on L_s, R_s and C_{tot}. Since the inductance is given by a monomial expression, we can require the inductance to equal some specific value, or to be within some range, *i.e.*,

$$L_s = L_{req} \qquad L_{min} \le L_s \le L_{max}. \tag{10}$$

The series resistance, being monomial, may be bounded similarly. We can also impose a limit on the capacitance contributed by the inductor with the posynomial constraint $C_{tot} \le C_{tot,max}$.

Quality factor. The quality factor of an inductor is defined as the ratio of peak magnetic energy minus peak electric energy to energy loss in one cycle (see [3]),

$$Q_L = \frac{\omega L_s}{R_s} \cdot \frac{\overline{R_p}\left(1 - \frac{R_s{}^2\overline{C_{tot}}}{L_s} - \omega^2 L_s \overline{C_{tot}}\right)}{\overline{R_p} + \left[\left(\frac{\omega L_s}{R_s}\right)^2 + 1\right] R_s}, \tag{11}$$

where $\overline{R_p} = 2R_p$ and $\overline{C_{tot}} = C_{tot}/2$ for two-port devices and $\overline{R_p} = R_p$ and $\overline{C_{tot}} = C_{tot}$ for one-port devices. Equation (11) is not posynomial in nature. However, the specification for minimum quality factor ($Q_L \ge Q_{L,min}$) can be written as a posynomial inequality in the design variables and $Q_{L,min}$,

$$\frac{Q_{L,min} R_s}{\omega L_s \overline{R_p}}\left[\overline{R_p} + \frac{(\omega L_s)^2}{R_s} + R_s\right] + \frac{R_s{}^2\overline{C_{tot}}}{L_s} + \omega^2 L_s \overline{C_{tot}} \le 1. \tag{12}$$

We can therefore specify a minimum required quality factor. We may also maximize the quality factor by maximizing $Q_{L,min}$ subject to constraint (12).

Minimum self-resonance frequency. The self-resonance frequency ω_{sr} is the frequency at which the quality factor Q_L is zero (see [3]). A condition on minimum self-resonance frequency $\omega_{sr} \ge \omega_{sr,min}$, can be written as the posynomial inequality

$$\omega_{sr,min}^2 L_s \overline{C_{tot}} + \frac{R_s^2 \overline{C_{tot}}}{L_s} \le 1. \tag{13}$$

Therefore we can handle a specification on minimum self-resonance frequency and we can maximize the self-resonance frequency (by maximizing $\omega_{sr,min}$ subject to constraint (13)).

Geometry constraints. The monomial inequalities $w \ge w_{min}$ and $s \ge s_{min}$ handle the processing constraints that limit the minimum feature size. The inductor area can be constrained or minimized using the monomial inequality, $d_{out}^2 \le A_{max}$.

The average radius d_{avg} is related to the other design variables by the expression $d_{avg} + (n-1)s + nw = d_{out}$. Noting that spacing s is typically small compared to d_{avg}, d_{out} and w, we can recast this last equation as the posynomial constraint,

$$d_{avg} + ns + nw \le d_{out}. \tag{14}$$

For all the design examples shown in this paper constraint (14) is always tight. However, there could be cases where this would not be the case and then the validity of the assumption must be checked.

5 Optimal design of inductors

A common problem in inductor design is to maximize the quality factor for a given inductance value and for a minimum self-resonance frequency. For example, in narrow-band LNA's (see Figure 4), the matching inductor L_s is required to take a value $L_s = R_s C_{gs}/g_m$ where C_{gs} and g_m are determined by the transistor choice. Ideally, the inductor must have a high quality factor.

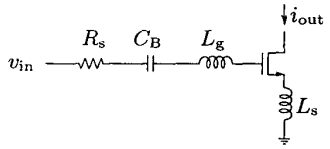

Figure 4: Narrow-band LNA (simplified circuit).

The design problem of the inductor can be formulated as,

$$\begin{array}{ll} \text{maximize} & Q_{L,min} \\ \text{subject to} & Q_L \ge Q_{L.min} \\ & L = L_{req} \\ & \omega_{sr} \ge \omega_{sr,min} \\ & \cdots \end{array} \tag{15}$$

Other constraints may be added (such as the minimum spacing and turn width, the maximum area available, the maximum parallel capacitance, etc...). The point is that the design problem can be formulated as a geometric program.

By repeatedly solving optimal design problems as we sweep over values of some constraint, we obtain globally optimal trade-off curves. For example, we can fix all other constraints, and repeatedly maximize the quality factor as we vary the required inductance. The resulting curve shows the globally optimal trade-off between quality factor and inductance value. In Figure 5 we show the maximum quality factor at 2.5GHz versus inductance value for inductors with PGS. The design constraints are $A > 400\mu m^2$, $w > 1.9\mu m$, $s > 1.9\mu m$ and $\omega_{sr} > 7GHz$ for curve 1 and unconstrained ω_{sr} for curve 2. Note that when the self-resonance frequency is not constrained one obtains a higher Q_L. The details on the test inductors built are shown in Table 1.

In Figure 6 we compare the performance of inductors with and without PGS at an operating frequency of 1.5GHz while meeting $A > 400\mu m^2$, $w > 1.9\mu m$, $s > 1.9\mu m$ and $\omega_{sr} > 5GHz$. The PGS option is preferable for small inductors because the increase in Q_L due to the elimination of substrate losses more than offsets the degradation due to the increased oxide capacitance. However, determining the point at which the use of a PGS is detrimental is challenging. Each inductor design was obtained in approximately one second real-time, and each trade-off curve was obtained in a few seconds.

6 Design of inductors for LC resonators

Tuned amplifiers are widely used to provide gain at selective frequencies. A simple tuned amplifier is shown in Figure 7. A sim-

Name	n	d_{out}	w	s	L_{s}
L1	4.75	206.3	7.8	1.9	6
L2	7.5	166.5	3.2	1.9	12
L3	9.5	152.9	1.9	1.9	18
L4	8	221.6	4.3	1.9	18
L5	3.75	292.2	13	1.9	6
L6	6.5	216.7	5.4	1.9	12

Table 1: Test inductors (dimensions in μm, inductance in nH, $t_{\text{ox,M5-poly}}$=5.2μm, t_{M5}=0.9μm, σ_{M5}=3 $\cdot$ $10^5(\Omega\text{cm})^{-1}$).

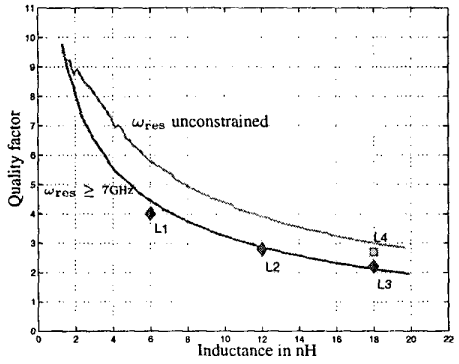

Figure 5: Maximum Q_{L} at 2.5GHz versus inductance value.

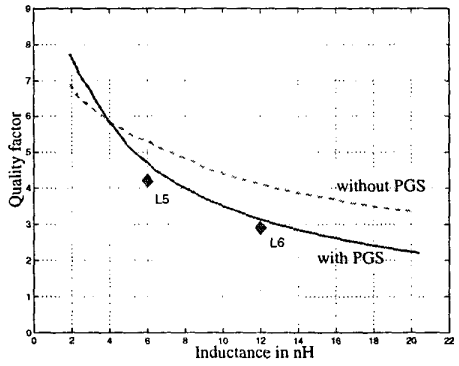

Figure 6: Maximum Q_{L} at 1.5GHz versus inductance value.

plified small-signal circuit is shown in Figure 8(a), where the transistor has been replaced by an ideal transconductance amplifier, the ideal inductor has been replaced by a real inductor, and C_{ad} represents the additional load capacitance C_{load}. An equivalent small-signal circuit is shown in Figure 8(b). For this application we define the quality factor of the tank as $Q_{\text{tank}} = R_{\text{tank}}/(\omega_{\text{res}} L_{\text{tank}})$. Note that this quality factor is not the same as the inductor quality factor Q_{L} since Q_{tank} does not account for capacitive losses.

Here, the design objective is to maximize the total parallel tank impedance at a given resonance frequency ω_{res}. For practical tank quality factors ($Q_{\text{tank}} > 1.5$), this is equivalent to maximizing the real impedance at resonance. The tank can be modeled as,

- **Tank inductance** (L_{tank}), given by a posynomial,

$$L_{\text{tank}} = \left[1 + (R_{\text{s}}/(L_{\text{s}}\omega))^2\right] L_{\text{s}}$$

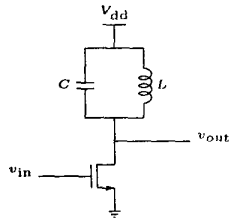

Figure 7: LC resonator.

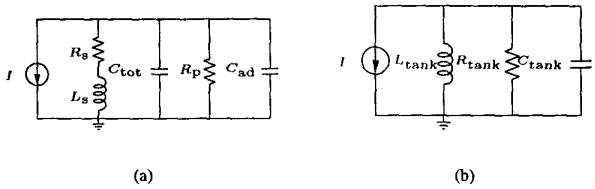

Figure 8: LC resonator small-signal circuit

- **Tank capacitance** (C_{tank}), given by a posynomial,

$$C_{\text{tank}} = C_{\text{ad}} + C_{\text{tot}} = C_{\text{load}} + C_{\text{tot}}$$

- **Tank resistance** (R_{tank}), given by

$$R_{\text{tank}} = R_{\text{p}} \parallel R_{\text{s,p}} = (1/R_{\text{p}} + 1/R_{\text{s,p}})^{-1}$$

where $R_{\text{s,p}}$ is the parallel equivalent of R_{s}. For $Q_{\text{tank}} > 1.5$, $R_{\text{s,p}}$ can be approximated by a monomial,

$$R_{\text{s,p}} = \left[(1 + (L_{\text{s}}\omega/R_{\text{s}})^2\right] R_{\text{s}} \approx (L_{\text{s}}\omega)^2 / R_{\text{s}}.$$

Since both R_{p} and $R_{\text{s,p}}$ are given by monomial expressions, the inverse of R_{tank} is a posynomial function of the design variables and therefore we can maximize R_{tank}.

- **Tank quality factor** (Q_{tank}). Since L_{tank} and the inverse of R_{tank} are posynomial functions of the design variables, the inverse of Q_{tank} is posynomial and we can therefore maximize Q_{tank} or impose a minimum required value.

Thus, a typical design problem can be posed as a geometric program,

$$\begin{array}{ll} \text{maximize} & R_{\text{tank}} \\ \text{subject to} & L_{\text{tank}} C_{\text{tank}} \leq 1/\omega_{res}^2 \\ & Q_{\text{tank}} \geq Q_{\text{tank,min}} \\ & C_{\text{load}} \leq C_{\text{load,max}} \\ & \ldots \end{array} \tag{16}$$

Note that the inequality on the resonance frequency ($L_{\text{tank}} C_{\text{tank}} \leq 1/\omega_{res}^2$) is always tight if there is no limit on the inductor area (*i.e.*, it is practically an equality). The reason is that if it were not tight, the inductor could contribute additional capacitance to the tank, which in turn would improve Q_{tank} and R_{tank}. One can also add other design constraints (such as the ones shown in §4) and the design problem will still be a geometric program.

7 Design of inductors for LC tunable oscillators

We now extend the work of §6 to the design of tuned resonators, commonly found in LC oscillators. Figure 8 shows the differential half-circuit of the LC oscillator of Figure 9. In this case C_{ad} is the sum of the load capacitance C_{load} and a variable capacitor C_{var}

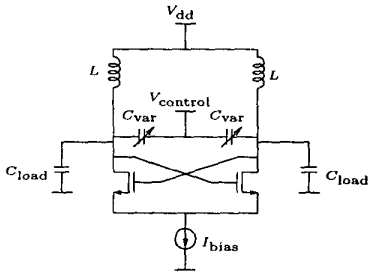

Figure 9: LC oscillator.

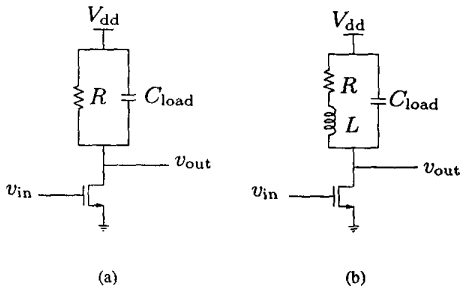

Figure 10: Shunt peaking example.

whose range is $C_{\min} \leq C_{\text{var}} \leq C_{\max}$. The ratio $C_{\max}/C_{\min}$ is limited ($\leq \alpha$) but the values of $C_{\max}$ and $C_{\min}$ are not limited. Typically, the design goal is to maximize the parallel resistance for a given tuning range. The tuning range is specified with two constraints

$$L_{\text{tank}}\left(C_{\text{load}} + C_{\text{tot}} + C_{\min}\right) \leq 1/\omega_{\max}^2 \quad (17)$$

$$L_{\text{tank}}\left(C_{\text{load}} + C_{\text{tot}} + C_{\max}\right) \geq 1/\omega_{\min}^2. \quad (18)$$

Constraint (18) is not posynomial and cannot be handled directly by GP. Note though, that constraint (17) is generally tight (if it were loose it would mean that an inductor with wider turns could be used and a better R_{tank} could be obtained). The fact that constraint (17) is always tight allows us to indirectly handle constraint (18). We can rewrite constraint (18) as,

$$\omega_{\min}^2\left(C_{\text{load}} + C_{\text{tot}} + C_{\max}\right) \geq \omega_{\max}^2\left(C_{\text{load}} + C_{\text{tot}} + C_{\min}\right).$$

Now we let $r = \omega_{\text{res,max}}^2/\omega_{\text{res,min}}^2$, and obtain

$$(r-1)(C_{\text{tot}} + C_{\text{load}})/C_{\max} + rC_{\min}/C_{\max} \leq 1. \quad (19)$$

Therefore, we can substitute the constraint (18) by the posynomial constraint (19). The typical design problem can be written as,

$$\begin{array}{ll} \text{maximize} & R_{\text{tank}} \\ \text{subject to} & L\left(C_{\text{load}} + C_{\text{tot}} + C_{\min}\right) \leq 1/\omega_{\max}^2 \\ & (r-1)(C_{\text{tot}} + C_{\text{load}})/C_{\max} + rC_{\min}/C_{\max} \leq 1 \\ & C_{\min} \geq \alpha C_{\max} \\ & Q_{\text{tank}} \geq Q_{\text{tank,min}} \\ & \cdots \end{array} \quad (20)$$

8 Design of inductors for shunt-peaked amplifiers

Consider a single-pole common source amplifier (Figure 10(a)) with $\omega_{3\text{dB}} \approx 1/RC_{\text{load}}$. The introduction of an inductance in series with the resistance (see Figure 10(b)) generates a double-pole, single-zero system whose frequency response is determined by the time constant ratio $m = R^2C_{\text{load}}/L$. The optimal value of m is determined by whether the design goal is to maximize bandwidth, minimize group delay or achieve a maximally flat response [6].

In on-chip implementations, the series resistance of the spiral inductor is absorbed within the gain resistor, R, and the capacitance of the inductor C_{tot} is added to the load capacitance C_{load}. The goal is to minimize the capacitance added by the inductor so that a large bandwidth extension can be obtained. The shunt-peaked amplifier problem can then be written as a geometric program,

$$\begin{array}{ll} \text{minimize} & C_{\text{tank}} \\ \text{subject to} & L_{\text{tank}} = R^2C_{\text{tank}}/m \\ & w > w_{\min} \\ & C_{\text{tank}} \geq C_{\text{load}} + C_{\text{tot}} \\ & \cdots \end{array} \quad (21)$$

Note that the constraint $C_{\text{tank}} \geq C_{\text{load}} + C_{\text{tot}}$ is always tight. If it were not tight we would be able to obtain a smaller value for C_{tank}, and the result would not be optimal.

9 Conclusions and Extensions

In this paper, we have exhibited how the design specifications of many inductor circuits can be represented by posynomial expressions. This representation enables us to translate the design goals into geometric programs which permit the circuits to be optimized efficiently and globally. The results of such optimization have been verified by experiments.

One can quickly plot tradeoff curves between different specifications, allowing an easy exploration of the design space. The versatility of geometric programming allows this method to be applied to a more general class of circuit design [7], and gives the designer the luxury of simultaneously optimizing all passive and active components in a variety of circuit architectures.

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