Distributed ESD Protection for High-Speed Integrated Circuits

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***Abstract*—Conventional ESD guidelines dictate a large protection device close to the pad. The resulting capacitive load causes a severe impedance mismatch and bandwidth degradation. A distributed ESD protection scheme is proposed to enable a low-loss impedance-matched transition from the package to the chip. A simple resistive model adequately predicts the ESD behavior under stress according to the charged device and human body models. The large area of the distributed ESD scheme would limit its application to designs such as distributed amplifiers, rf transceivers, A/D converters, and serial links with only a few dedicated high-speed interfaces. The distributed ESD protection is compatible with high-speed layout guidelines, requiring only low-loss transmission lines in addition to a conventional ESD device.**

***Index Terms*—Distributed amplifiers, electrostatic discharges, impedance matching, transceivers.**

I. Introduction

THE CONTINUOUS scaling of integrated circuits has enabled a rapid increase in operating frequencies. But the electrostatic discharge (ESD) requirements to protect the circuits during packaging and handling have not scaled accordingly. The capacitance associated with the ESD protection is therefore progressively becoming a bottleneck. The parasitic I/O capacitance which is often dominated by ESD in a state-of-the-art CMOS technology is typically in the range 2 to 8 pF. At high frequencies, the reactance associated with this large capacitance becomes comparable to the 50-Ω characteristic impedance of the package and board interfaces. This causes significant reflections and severely limits the chip-to-chip signal bandwidth. There is therefore only limited or no ESD protection in multi-GHz designs [1]–[4]. However, yield loss due to ESD failures is expected to become increasingly important as high-volume designs enter the GHz regime [5]. In this work, a distributed ESD protection scheme is described. It can achieve high bandwidth with minimal compromise in ESD performance [4].

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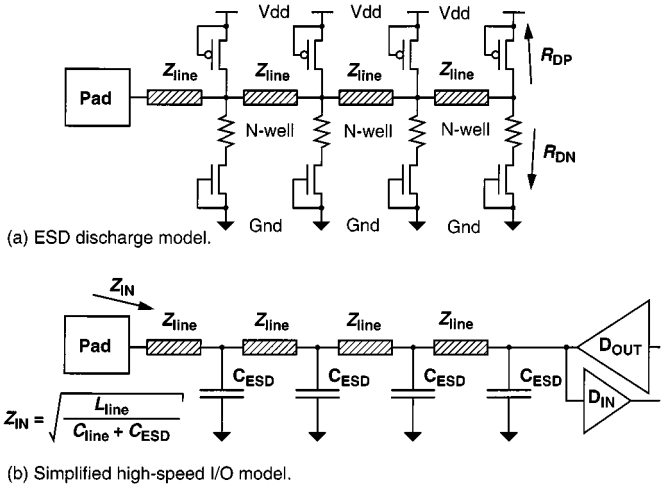


Fig. 1. Simplified distributed ESD electrical models. To avoid the impedance discontinuity due to a large lumped capacitance at the pad, the four segments of the ESD protection device are separated by high characteristic impedance lines (Z_{line}). The device capacitance is thereby effectively absorbed in this artificial transmission line, providing a continuous transmission line with the same characteristic impedance (Z_0) from the board to the receiver. (a) During ESD stress the dynamic resistance snap-back characteristics of the grounded gate is modeled as R_{DP} to Vdd and R_{DN} to ground, and during normal operation, (b) the parasitic capacitance of the ESD protection is modeled as $C_{\rm ESD}$ to ac ground. The frequency-dependent loss components associated with the transmission line, the finite output conductance of the turned-off protection device and the N-well resistor are omitted in the schematic.

II. Distributed ESD Design

The distributed ESD structure is illustrated in Fig. 1(a). The four CMOS grounded gate protection devices are separated by line segments (Z_{line}). The dynamic device resistance during the ESD event is modeled with R_{DN} and R_{DP}. A simplified model of the ESD structure for high-speed operation is shown in Fig. 1(b). The ESD protection devices are off during normal operation. By providing sufficient on-chip decoupling capacitance between Vdd and Ground, the protection devices can be modeled as parasitic capacitors ($C_{\rm ESD}$) to ac ground. A more detailed model should incorporate the voltage-dependent device capacitance, the frequency-dependent loss components associated with the transmission line, the finite output conductance of the turned-off protection device, and the N-well resistance. The design optimization will be similar to that used in our approach: by using high-Z_0 line segments, the effective characteristic impedance including the additional device capacitance can be designed to match external components [$Z_{\rm IN} = Z_0$ in

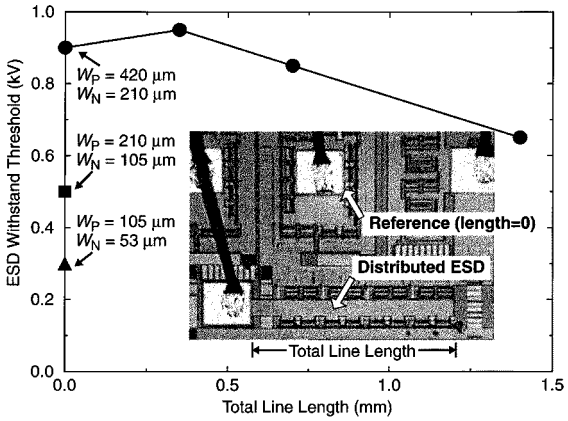
Fig. 1(b)], yielding excellent broadband performance [2]–[4]. The idea of distributed ESD protection is controversial since the protection device is typically placed as close to the I/O pad as possible. In fact, even slight non-uniformities in the via placement can severely limit the ESD protection effectiveness [6]. The distributed device would seem to exaggerate this nonuniformity. However, if low-resistive lines that are common in high-frequency designs are used [2]–[4], [7], the voltage drop due to metal line ohmic heating during the ESD event could be minimal [8], [9]. A small resistor in series with the ESD devices could further improve the snap-back triggering uniformity [10].

III. Experiment

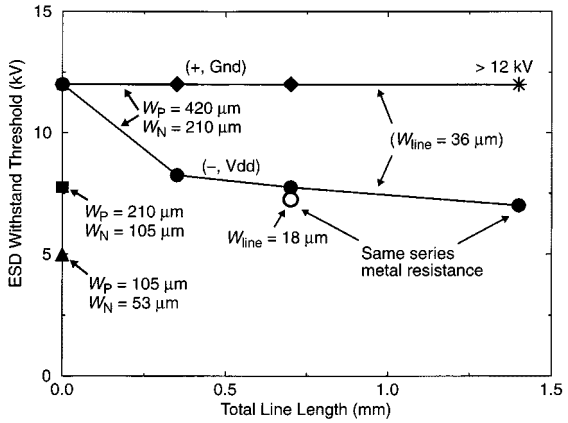
In order to investigate both the high-frequency and ESD aspects of a distributed ESD protection scheme, an advanced process would be preferred. The high frequency behavior of distributed amplification has been studied elsewhere [2]–[4]. This paper will focus on the ESD aspect of the distributed protection scheme. A testchip was implemented in a triple metal (AlCu) 0.5-μm CMOS technology. Line widths in the range 10 to 20 μm are typical for low-loss transmission lines on Si substrate [2], [7]. To emulate the top level metal of an advanced process with thick and low resistivity material such as Cu, wider lines were used. Conventional CMOS output buffers with 210-μm wide n-FETs and 420-μm wide p-FETs were designed to drive a 50-Ω external impedance in normal operation and act as protection devices during the ESD event. The output buffer was partitioned into four equal segments separated by 36-μm wide, 1-μm thick Al metal lines with total lengths in the range of 0.35–1.4 mm. Reference lumped ESD protection devices with full ($W_N = 210\,\mu$m, $W_P = 420\,\mu$m), half, and quarter the device widths were also implemented. Common Vdd and Ground lines with ESD clamps were employed [11]. The chips were packaged in ceramic dual-in-line and leadless chip carrier packages. They were stressed according to the charged device model (CDM, Oryx 9000 [12]) and the human body model (HBM, IMCS 2400C [13]).

IV. Results and Discussions

The CDM stress results for a leakage threshold of 1 μA at 3 V are shown in Fig. 2(a) accompanied with a die micrograph of a lumped reference and a distributed ESD device. The reference devices exhibit the expected performance: the full-width device fails at the highest voltage (900 V) and the quarter-width device fails at the lowest voltage (300 V). Only a minor degradation is observed for the distributed ESD protection. Devices with line lengths up to 0.7 mm fail above 800 V while the 1.4-mm long device fails at 650 V. Since the smallest reference ($W_N = 53\,\mu$m, $W_P = 105\,\mu$m) is similar to one of the four segments of the distributed buffers, it is clear that several segments conduct current during the ESD event. Although this minimal reduction in withstand threshold seems to contradict previous data [6], it is consistent with observations of uniform triggering for short ESD pulses [14]. For comparison, CDM stress was also applied to an amplifier with a unity gain of 23 GHz [2]. In order to enable the high operating frequency, no ESD protection was incorporated, and a withstand threshold of only 200 V was observed. The HBM stress results are shown in Fig. 2(b). There is negligible



(a)



(b)

Fig. 2. Experimental withstand threshold versus total line length. (a) CDM. Withstand threshold after negative and positive CDM discharge stress. The reference devices are located around the pad as shown in the die micrograph insert. The lumped reference devices (total line length $= 0$) have the expected withstand thresholds. The distributed ESD yields a minimal degradation compared to the reference device indicating that several segments conduct current during the ESD event. The 5% *higher* withstand threshold of the 0.35-mm distributed ESD compared to the reference is unexpected. It appears to be due to finite Vdd/Gnd layout variations in the power grid resulting in a slightly lower resistance Vdd/Gnd return for the 0.35-mm distributed ESD than for the lumped reference. (b) HBM. Positive stress to ground (+, Gnd) results in negligible performance degradation (12 kV or above—instrument limit) for the distributed ESD devices. Negative stress to Vdd (−, Vdd) results in a more significant line length dependence but still a better performance than the reference device with half the width (only two of the four segments). The 0.7-mm distributed ESD with half the line width and the 1.4-mm distributed ESD have the same metal resistance and also the same withstand thresholds suggesting a simple resistive correlation.

performance degradation versus line length for positive stress to Ground. The withstand threshold is 12 kV for line lengths as long as 1.4 mm. For a 210-μm n-FET, this threshold may appear too high ($I_{t2} > 30$ mA/μm). The failure is observed to be near the drain of the p-FET transistor, indicating that the current flows in both the n-FET and the drain-to-well diode of the p-FET, thereby reducing the stress on the n-FET. A resistor is not included in series with the p-FET transistor, hence the effective dynamic resistance (R_D) is lower for negative stress to Vdd. This results in a reduction of the withstand threshold from 12–8 kV for a total line length of 0.35 mm. Nevertheless, the withstand threshold is higher than the 5 kV of the quarter-width reference device ($W_N = 53\,\mu$m, $W_P = 105\,\mu$m), indicating that more than one segment conducts current.

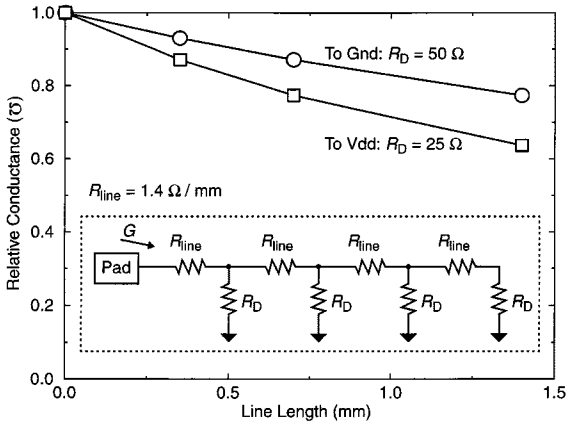


Fig. 3. Simplified analytical dc conductance model relative to the reference ($R_{line} = 0, G = 4/R_D$) based on extracted dynamic ESD device resistance ($R_D = 25\,\Omega$ to Vdd and 50 Ω to Gnd) plotted versus line length for the 36-μm wide top-level metal line ($R_{line} = 1.4\,\Omega$/mm). Insert illustrates simple conductance model with metal line components (R_{line}) and ESD protection device dynamic on-resistors (R_D).

The ESD pulse rise time is between 0.1 ns and 10 ns [15]. The time-of-flight of an on-chip transmission line is more than an order of magnitude smaller (about 10 ps/mm [2]). The distributed ESD protection therefore appears as a lumped load at the dominant frequencies of the ESD pulse. A dc resistive network that neglects the on-chip transmission line delay is appropriate to model the ESD performance as a function of line length. This simplification is supported by the fact that a 0.7-mm distributed ESD device with half the metal width (18 μm) has the same series metal resistance as a 1.4-mm distributed ESD device. The time-of flight differs by almost $2\times$, yet a similar withstand threshold is observed [7 kV, Fig. 2(b)]. The line impedance is modeled as $Z_{line} = R_{line}$, and the dynamic resistance for each device segment, R_D, is extracted from current–voltage (I–V) characterization. The relative conductance of the resistive ladder (insert of Fig. 3) is plotted versus line length in Fig. 3. For line lengths up to 0.7 mm the conductance is reduced to 80% and 90% relative to $G = 4/R_D$ for $R_D = 25\,\Omega$ and 50 Ω, respectively. This reduction in conductance is consistent with the degradation in withstand threshold observed for the CDM data in Fig. 2(a) as well as for the HBM data with positive stress to ground in Fig. 2(b). Notice that the simple model does not include any temperature-related resistive increase in the metal line. Typically, up to two times increase in resistance is observed at the onset of metal melting during ESD stress [9]. However, in our design a large metal cross-sectional area is used (36 μm^2) which is more than three times what is usually recommended [9], [16]. This reduces the temperature increase during ESD stress and the transmission line loss in normal operation.

The simple model underestimates the degradation for negative HBM stress to Vdd as shown in Fig. 2(b). This is believed to be due to the different stress levels for the two ESD models. The reference device has a high tolerance to HBM stress (12 kV) but only a moderate tolerance to CDM stress (0.9 kV) due to the relatively long N-well (3.6 μm) in series with the n-FET. It protects the n-FET during the HBM stress, but also limits the effectiveness of the n-FET to snap back and provide a low-resistance current path to ground during the CDM stress. The metal heating and the corresponding increase in metal resistance will therefore be larger during the HBM stress tests. This adversely affects the distributed ESD structure since the increase in metal resistance will occur close to the pad. In addition, the parallel conduction in the p-FET and the diode of the n-FET results in an effective lowering of the dynamic resistance which is more severe at high current levels. Hence, at extreme stress conditions, the conductance model needs to account for the current-dependent and temperature-dependent resistances [16].

V. Conclusion

A distributed ESD protection scheme that provides sufficient safeguard against ESD damage and simultaneously enables a low-loss, impedance-matched transition from the package to the chip was demonstrated. A simple dc model explains the ESD performance to be related to the ratio of the dynamic on-resistance of the protection device and the series resistance of the line segments in the distributed structure.

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