A 10Gb/s NRZ Receiver with Feedforward Equalizer and Glitch-Free Phase-Frequency Detector

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***Abstract*—A 10Gb/s NRZ receiver with feedforward equalizer and CDR is described. The CDR incorporates an LC oscillator with a range of 8.3 to 11.1 GHz and a new glitch-free binary PFD. The glitch-free architecture minimizes the jitter generation of the CDR and increases jitter tolerance. The CDR loop employs a V/I converter with two independent charge-pumps for FD and PD signals to achieve fast acquisition and low jitter generation simultaneously.**

I. INTRODUCTION

High-speed serial communications systems such as SONET and Ethernet have gradually transitioned to operating speeds of 10Gb/s and beyond. A 10Gb/s NRZ receiver with programmable feedforward equalizer (FFE) and a clock and data recovery (CDR) circuit is fabricated in a 0.25µm SiGe BiCMOS process with a 50GHz peak f_t. The FFE provides a programmable high frequency boost to compensate for channel loss. The CDR circuit employs a new glitch-free phase and frequency detector (PFD). The new PFD architecture removes erroneous phase and frequency detections that can result from clock and data jitter. By doing so, CDR jitter generation decreases and its high frequency jitter tolerance increases. The frequency acquisition time also decreases, for the same loop parameters.

II. CIRCUIT ARCHITECTURE

The receiver architecture is illustrated in Fig. 1. The CDR block samples the received signal after equalization by the FFE. The CDR consists of a VCO and a binary PFD. The phase detector (PD) and frequency detector (FD) signals are fed back to the VCO using two V/I converters after low-pass filtering by a second-order RC loop filter. The RC filter is fully integrated on-chip.

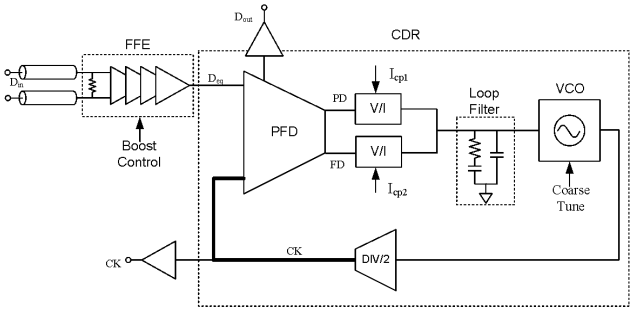

Figure 1. Receiver architecture.

A. Feedforward Equalizer

At multi-Gb/s data rates the transmission medium limits the signal bandwidth. The high frequency roll-off of the channel frequency response, as well as its nonlinear phase, introduces ISI.

A programmable feedforward equalizer is designed to invert the effect of the channel. The FFE consists of four cascaded stages of a high frequency boost circuit, illustrated in Fig. 2. The boost circuit uses simple capacitive bypassing across degenerating resistors to compensate the channel's high frequency roll-off [1]. The peak boost occurs at 5-7GHz and is variable between 3 and 20dB. A 3-bit word controls R_E and C_E and therefore the poles and zeros of the equalizer. This boost range suffices to match the magnitude of the equalizer's frequency response to the inverse of the channel response with reasonable accuracy. However, their phases will generally not match well, leaving the equalized signal with some residual ISI.

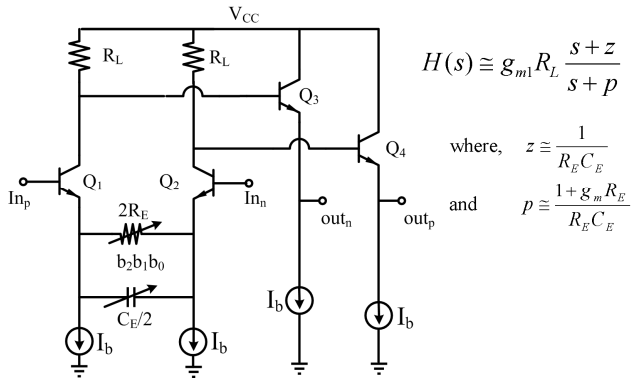

Figure 2. Feedforward equalizer boost circuit.

The boost stages are ac-coupled to minimize the dc offset.

B. VCO

As shown in Fig. 3, the VCO is an LC oscillator with fine and coarse tuning. The fine tuning is performed using MOS varactors. A 6-bit controlled capacitor bank provides the coarse tuning, allowing the VCO to function over a frequency range of 8.3 to 11.1 GHz. The varactor is large enough so that any frequency can be synthesized using three adjacent coarse settings. The tank Q is limited by loss in the capacitor bank due to the MOS switches' series resistances. The spiral inductors in this process technology have a much higher Q than the capacitor-switch combination. The MOS switches' parasitic capacitance decreases the tuning range of the VCO [2]. Bigger switches result in lower resistance and therefore higher Q, but also lower tuning range. The sizes of these switches are consequently chosen to achieve a 40 percent tuning range, while maintaining a Q of at least 5.

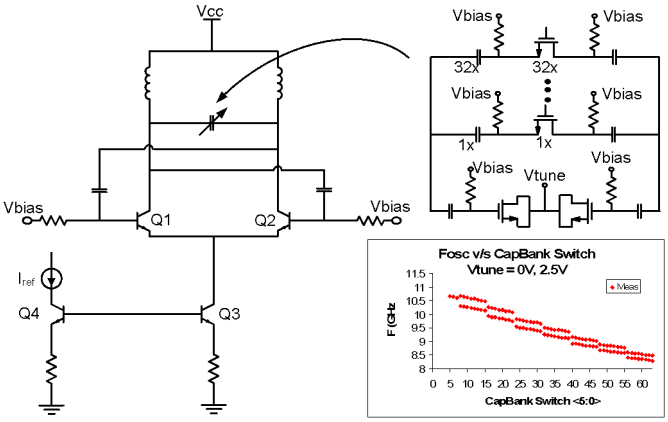

Figure 3. VCO.

C. Phase and Frequency Detector

A binary PD determines if the clock zero crossing (edge) is early or late with respect to the data edge [3]. As illustrated in Fig. 4, two sets of flip-flops latch the data signal using in-phase and quadrature-phase signals of a half-rate clock. A double-edge flip-flop architecture is used to overcome the speed limitations of the process [4].

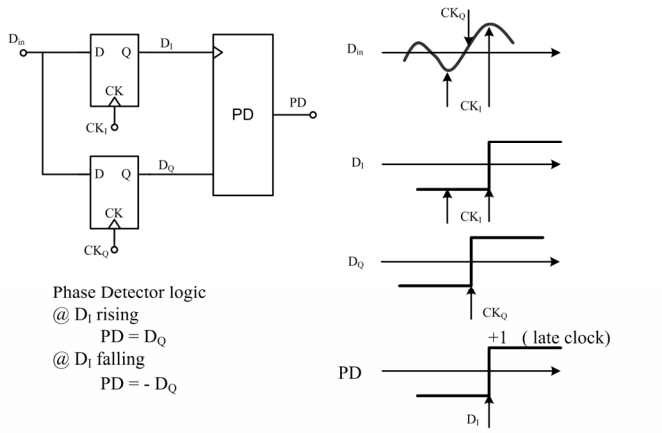

Figure 4. Binary phase detector.

When the data rate differs slightly from the clock frequency, the PD output toggles between the early and late states every time the clock edge passes the data edge. The result is a beat signal with a frequency approximately equal to the difference (Δf) between the clock frequency and the data rate. The PD generates the same beat signal whether Δf is positive or negative.

A second PD with a shifted clock reference allows determination of the polarity of Δf [5]. The two reference clocks are chosen approximately one quarter of a bit period apart. The frequency detector determines if the data rate is higher or lower than the clock, depending on the direction that the data edge is moving with respect to the two reference clocks. If PD1's transition from the early to late state precedes that of PD2, it means that the clock is slower than the data. The FD logic is described in Fig. 5.

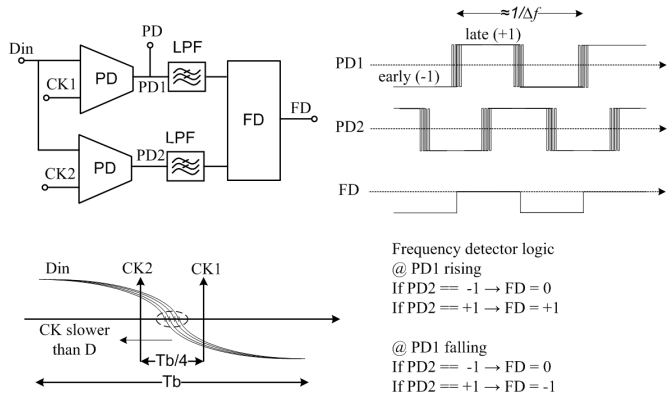

Figure 5. Phase and frequency detector.

The FD signal resets to zero (ternary level) after a frequency detection is made [5]. This action guarantees that the FD signal goes to zero when frequency lock is achieved. A trade-off is a doubling of the frequency acquisition time. When the loop achieves phase and frequency lock, FD = 0,

PD2 = -1 and PD1 goes to a limit cycle and alternates between early and late.

In the presence of jitter on the data and clock signals, there will be glitches on the PD signals when the PD transitions between the early and late states. This glitching results from erroneous phase detections when the edges of the data and clock signals approach each other. Setup and hold time violations in the PD flip-flops also produce PD errors.

Fig. 6 shows that an "early" detection can result from jitter, even when the edges of the clock are actually late on average with respect to those of data.

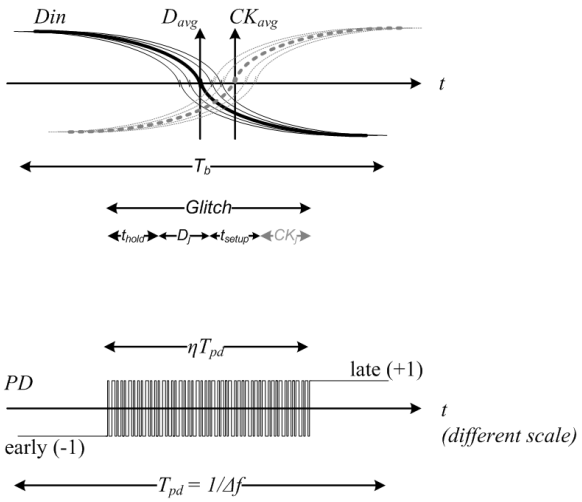

Figure 6. Phase detector glitch generation.

The percentage of the time that these errors might occur is:

$$\eta = \frac{CK_j + D_j + t_{setup} + t_{hold}}{T_b} \tag{1}$$

where D_j is the data peak-to-peak jitter, including the data-dependent jitter resulting from residual ISI, in addition to random jitter; CK_j is the clock peak-to-peak jitter; t_{setup} and t_{hold} are the setup and hold time of the PD flip-flops, respectively, and T_b is the bit period. For proper operation, $\eta << 1$.

In conventional implementations, any PD glitches are left to be filtered by the loop filter. Wrong PD decisions (glitches) increase the jitter generation because they temporarily move the loop in the wrong direction. However, the loop still generally moves in the right direction, because there will be more correct phase detections than wrong ones on average. These PD glitches also undermine FD operation, causing erroneous frequency detections that result in lower jitter tolerance and narrower frequency capture range for the CDR. For higher η values the CDR loop may even become unstable.

To avoid these conventional problems, this work adds two lowpass filters (see Fig. 5) to remove PD glitches *before* FD determination. The bandwidth of each lowpass filter is much higher than the loop bandwidth of the CDR, so it does not interfere with the loop dynamics, but is much lower than the data rate to make sure that all the narrow pulses on the PDs are filtered. This inequality is readily satisfied because the widths of the PD glitches are typically one to several bit periods (depending on the jitter statistics).

By removing erroneous PD and FD decisions, CDR jitter generation decreases. Furthermore its high-frequency jitter tolerance approaches the fundamental limit set by flip-flop setup and hold time. The frequency acquisition time also decreases, by up to a factor of two (in high-jitter cases), for the same loop parameters.

III. CDR Loop Dynamics

Fig. 7 shows how the PD and FD signals are used in the CDR loop. During frequency acquisition, the CDR loop is driven by the FD signal because the PD is a beat signal with an average value of zero. The FD signal has an average value of one-half. During acquisition, the rate of the VCO's frequency change is approximately:

$$\frac{df}{dt} = \frac{I_{fd}}{2C} \cdot K_{VCO} \tag{2}$$

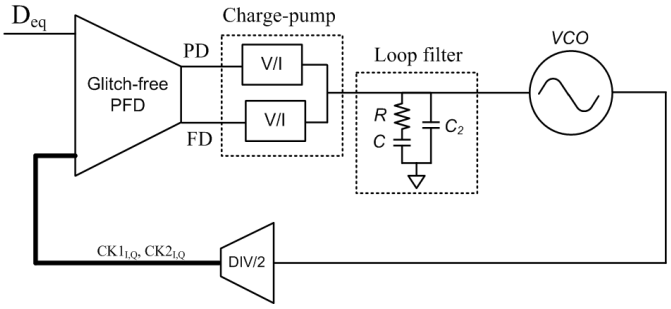

Figure 7. CDR Loop.

where I_{fd} is the FD charge-pump current and C is the loop filter integration capacitance. Therefore, the frequency acquisition time is approximately:

$$T_a = |\Delta f| \cdot \frac{2C}{I_{fd} \cdot K_{VCO}} \tag{3}$$

After frequency acquisition, the FD output becomes zero, and loop behavior is controlled by the PD signal. Fig. 8 illustrates a small-signal model for the CDR loop [6]. φ_{dn} and φ_n are the samples of the data and clock phases at $t_n = nT_b$.

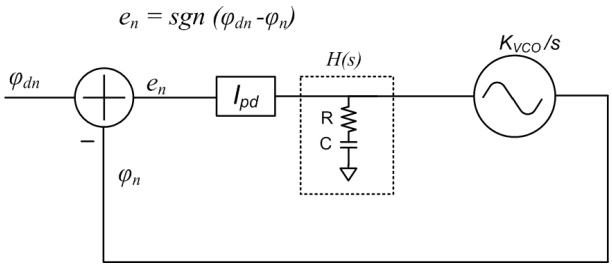

Figure 8. CDR loop small-signal model.

A discrete-time equivalent of the CDR system is shown in Fig. 9.

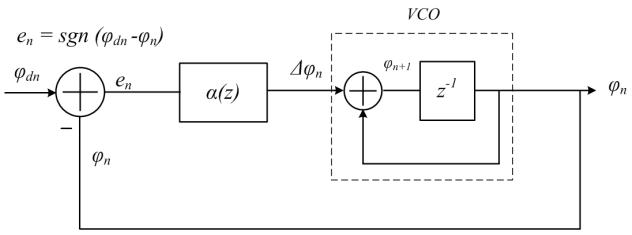

Figure 9. CDR loop discrete-time model.

Here,

$$\alpha(z) = k_{vco} I_{pd} \left(\left(RT_b + \frac{T_b^2}{2C} \right) + \frac{T_b^2 z^{-1}}{C(1 - z^{-1})} \right) \quad (4)$$

where I_{pd} is the PD charge-pump current. The jitter generation is directly proportional to the charge-pump current. However, the frequency acquisition time is inversely proportional to the charge-pump current, see (3).

To overcome this trade-off, the PD and FD signals are summed in the current domain with different weights using two independent charge-pump circuits. The FD uses a higher charge-pump current for faster acquisition while the PD uses a smaller charge-pump current to ensure low jitter generation.

The FFE and VCO core consume 10mW and 8.3mW from a 2.5V supply, respectively. The total power consumption (excluding the output buffers) is 260mW; more than half is used for data and clock buffering and distribution. The die size (including drivers) is 2.7×2.4mm2 and it is packaged in a standard leadless package. The die micrograph is shown in Fig. 10.

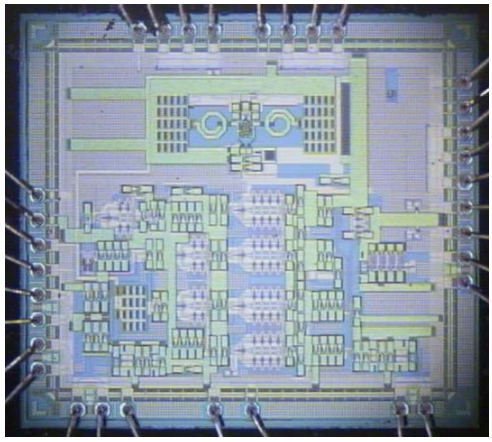

Figure 10. Die micragh.

IV. MEASUREMENT RESULTS

Fig. 11 shows the recovered data and clock at 10.2Gb/s. The transmitted pattern is PRBS7 and the channel is 91cm of copper trace on an FR4 board, BER < 10^{-12}. The recovered clock rms jitter is 1.1ps. Fig. 11 also illustrates the CDR jitter tolerance to sinusoidal jitter.

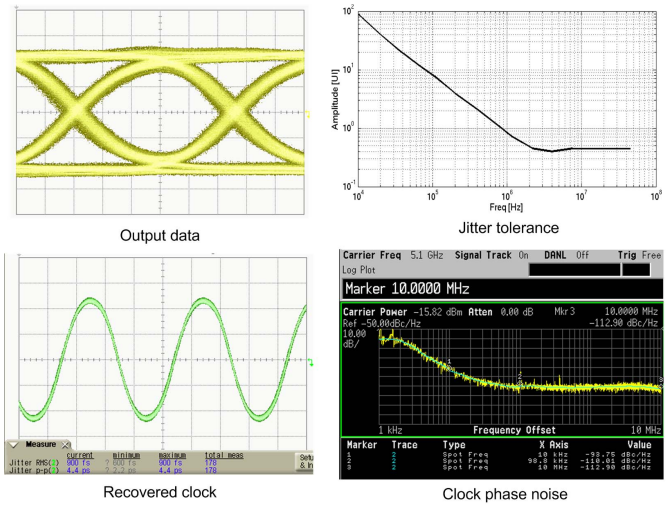

Figure 11. The output eye, CDR jitter tolerance, the recovered clock and its phase noise.

The CDR tracking bandwidth is approximately 4MHz. The jitter tolerance outside the tracking bandwidth is 0.45UI. The CML flip-flops' setup-plus-hold time is approximately 30ps or 0.3UI in this process.

V. CONCLUSION

A 10-Gb/s NRZ receiver with a new glitch-free PFD is implemented. The receiver equalizes the channel, acquires the frequency, achieves phase-lock, and samples the data. The glitch-free PFD architecture minimizes CDR jitter generation and maximizes its jitter tolerance. Having two independent V/I converters for FD and PD signals enables the CDR to perform an automatic charge-pump current gearshift when it transitions from the frequency acquisition mode to the phase-lock mode.

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