Modeling and Characterization of On-Chip Transformers

Sunderarajan S. Mohan, C. Patrick Yue, Maria del Mar Hershenson, S. Simon Wong, and Thomas H. Lee

Center for Integrated Systems, Stanford University, Stanford, CA 94305

Abstract

We present a scalable analytical model for on-chip transformers that is suitable for design optimization and circuit simulation. We also provide simple and accurate expressions for evaluating the self inductance and the mutual coupling coefficient (k). The model agrees very well with measurements for a variety of transformer configurations.

1 Introduction

The rising demand for low-cost radio frequency integrated circuits (RF-IC's) has generated tremendous interest in on-chip passive components. Transformers are important elements in RF designs for impedance conversion, impedance matching and bandwidth enhancement. Although on-chip transformers have been employed in RF-IC's [1, 2], models for providing design guidelines have not been reported. In this paper, we present an analytical model for monolithic transformers that is suitable for circuit simulation and design optimization. We also provide simple expressions for calculating the mutual coupling coefficient (k).

We first discuss different on-chip transformers and discuss their advantages and disadvantages (§2). We then present an analytical model along with expressions for the elements in it and the mutual coupling coefficient (§3). In §4 we present experimental verification for the model and finally summarize our findings in §5.

2 Monolithic Transformer Realizations

Fig. 1 illustrates three common configurations of monolithic transformers. The different realizations offer varying trade-offs among the self inductance and series resistance of each port, the mutual coupling coefficient, the port-to-port and port-to-substrate capacitances, resonance frequencies, symmetry and area. Our models and coupling expressions allow these tradeoffs to be systematically explored, thereby permitting transformers to be customized for a variety of circuit design requirements.

The desired characteristics for a transformer are application dependent. Transformers can be configured as three or four terminal devices. They may be used for narrowband or broadband applications. For example, in single sided to differential conversion, the transformer might be used as a four terminal narrowband device. In this case, a high mutual coupling coefficient and high self-inductance are desired along with low series resistance. On the other hand, for bandwidth extension applications, the transformer is used as a broadband three terminal device. In this case, a small mutual coupling coefficient and high series resistance are acceptable while all capacitances need to be minimized [3].

The tapped transformer (Fig. 1.a) is best suited for three-port applications. It permits a variety of tapping ratios to be realized. This transformer relies only on lateral magnetic coupling. All windings can be implemented with the top metal layer, thereby minimizing port-to-substrate capacitances. Since the two inductors occupy separate regions, the self-inductance is maximized while the port-to-port capacitance is minimized. Unfortunately, this spatial separation also leads to low mutual coupling ($k \approx 0.3 - 0.5$).

The interleaved transformer (Fig. 1.b) is best suited for four-port applications that demand symmetry. Once again, capacitances can be minimized by implementation on top level metal so that high resonant frequencies may be realized. The interleaving of the two inductances permit moderate coupling ($k \approx 0.7$) to be achieved at the cost of reduced self-inductance. This coupling may be increased at the cost of higher series resistance by reducing the turn width (w) and spacing (s).

The stacked transformer (Fig. 1.c) uses multiple metal layers and exploits both vertical and lateral magnetic coupling to provide the best area efficiency, the highest self-inductance and highest coupling ($k \approx 0.9$). This configuration is suitable for both three and four terminal configurations. The main drawback is the high port-to-port capacitance, or equivalently a low self-resonance frequency. In some cases, such as narrowband impedance transformers, this capacitance may be incorporated as part of the resonant circuit. Also, in modern multi-level processes, the capacitance can be reduced by increasing the oxide thickness between spirals. For example, in a five metal process, $50 - 70\%$ reductions in port-to-port capacitance can be achieved by implementing the spirals on layers five and three instead of five and four. The increased vertical separation will reduce k by less than 5%. One can also trade off reduced coupling for reduced capacitance by displacing the centers of the stacked inductors (Fig. 1.d,1.e).

3 Analytical Transformer Model

Fig. 2 presents the analytical models for tapped and stacked transformers. The expressions for the series resistances ($R_{\mathrm{s,o}}$, $R_{\mathrm{s,i}}$, $R_{\mathrm{s,t}}$, $R_{\mathrm{s,b}}$), the port-substrate capacitances ($C_{\mathrm{ox,o}}$, $C_{\mathrm{ox,i}}$, $C_{\mathrm{ox,t}}$, $C_{\mathrm{ox,b}}$, $C_{\mathrm{ox,m}}$) and the crossover capacitances ($C_{\mathrm{ov,o}}$, $C_{\mathrm{ov,i}}$, C_{ov}) are taken from [4]. Note that the model accounts for the increase in series resistance with frequency due to skin effect. Patterned ground shields (PGS) are placed beneath the transformers to isolate them from resistive and capacitive coupling to the substrate [5]. As a result, the substrate parasitics can be neglected.

The inductance values are computed using a modified version of Wheeler's formula [6]. This expression does not take into account the variation in inductance due to conductor thickness and frequency. In practical inductor and transformer realizations, the thickness is small compared to the lateral dimensions of the coil and has only a small impact on the inductance. For typical conductor thickness variations ($0.5\mu\text{m}-2.0\mu\text{m}$), the change in inductance is within a few percent for practical inductor geometries. The inductance also changes with frequency due to changes in current distribution within the conductor. However, over the useful frequency range of a spiral, this variation is negligible [4]. When compared to field solver simulations, the inductance expression exhibits a maximum error of 8% over a broad design space (OD varying from $100\mu\text{m}$ to $480\mu\text{m}$, L varying from 0.5nH to 100nH, w varying from $2\mu\text{m}$ to 0.3OD, s varying from $2\mu\text{m}$ to w and ID varying from 0.2OD to 0.8OD).

For the tapped transformer, the mutual inductance is determined by first calculating the inductance of the whole spiral (L_T), the inductance of the outer spiral (L_o), the inductance of the inner spiral (L_i), and then using the expression $M = (L_\text{T} - L_\text{o} - L_\text{i})/2$. For the stacked transformer, the spirals have identical lateral geometries and therefore identical inductances. In this case, the mutual inductance is determined by first calculating the inductance of one spiral (L_t), the coupling coefficient (k) and then using the expression $M = kL_\text{t}$. In this last case the coupling coefficient is given by $k \approx (0.9 - d_\text{s}/\text{AD})$ for $d_\text{s} < 0.7\text{AD}$, where d_s is the center-to-center spiral distance and AD is the average diameter of the spirals. As d_s increases beyond 0.7AD, the mutual coupling coefficient becomes harder to model. Eventually, k crosses zero and reaches a minimum value of approximately -0.1 at $d_\text{s} \approx \text{AD}$. As d_s increases further, k asymptotically approaches zero. At $d_\text{s} \approx 2\text{AD}$, $k \approx -0.02$, indicating that the magnetic coupling between closely spaced spirals is negligible.

The self inductances, series resistances and mutual inductances are independent of whether a transformer is used as a three or four terminal device. The only elements that require recomputation are the port-to-port and port-to-substrate capacitances. This situation is analogous to that of a spiral inductor being used as a single or dual terminal device.

4 Experimental Verification

The measurements were conducted on structures designed for operation as three terminal devices. One of the ports was grounded while the other two ports were terminated in the 50Ω environment of the test equipment. Two-port S-parameter measurements were obtained using an HP8720B Network Analyzer and coplanar ground-signal-ground probes.

The expression for k is verified in the experiment shown in Fig. 3, which plots the coupling coefficient between two stacked 20nH spirals as a function of shift. Good agreement between measured and modeled values of k (Fig. 3) is observed. In practical transformers, the lateral dimensions are much larger than the vertical dimensions. In such cases, variations in the vertical dimension result in k changing by less than 10% and can therefore be neglected.

The predictions of the analytical models were compared with measurements for a variety of transformers. Fig. 4 shows good agreement for a tapped transformer (L_o=3nH, L_i=2nH, k=0.35) fabricated on a quartz substrate which has negligible parasitic capacitances. Fig. $5-7$ show good agreement for stacked transformers (L_t=20nH, L_b=20nH) with various shifts (k=0.9, k=0.55, k=0.3). The stacked transformers are fabricated on the third and second layers of a triple-metal $0.5\mu\text{m}$ CMOS epi-process with the patterned ground shields (PGS) being implemented on the polysilicon layer.

Just as in the modeling of any distributed system, the lumped circuit model breaks down at higher frequencies. The model is accurate up to the self-resonance frequencies of the individual ports, which is the useful range for transformers applications. The close match between measured and modeled S-parameters over a wide range of coupling coefficients, processes and configurations confirms the accuracy, scalability and robustness of the models presented.

5 Conclusions

We have presented an analytical model for on-chip transformers. The model has been compared to measurement results over a variety of configurations, processes and coupling coefficients. The predicted and measured S-parameters show very good agreement. The model is scalable and robust and can be easily incorporated in an optimization algorithm.

6 Acknowledgments

The authors are grateful to Dr. Christopher Hull and Dr. Paramjit Singh for help during layout and to Rockwell Inc. for fabricating the dice. Finally, they would like to thank the Stanford Nanofabrication Facility staff for their assistance in processing. This work has been supported in part by the industrial sponsors of the Center for Integrated Systems and NSF contract MIP-9313701.

References

[1] J. Zhou et al., "A fully integrated CMOS 900MHz LNA using monolithic transformers," in *ISSCC'98*, pp. 132–133.

[2] J. R. Long et al., "A 1.9 GHz low-voltage silicon bipolar receiver front-end for wireless personal communications systems," *IEEE JSSC*, vol. 30, pp. 1438–1448, Dec. 1995.

[3] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, Cambridge University Press, Cambridge, 1998.

[4] C. P. Yue et al., "A physical model for planar spiral inductors on silicon," in *Proc. IEEE IEDM'96*, pp. 155–158.

[5] C. P. Yue et al., "On-chip spiral inductors with patterned ground shields for Si-based RF IC's," *IEEE JSSC*, vol. 33, pp. 743–752, May 1998.

[6] H. A. Wheeler, "Simple inductance formulas for radio coils," *Proc. of the IRE*, vol. 16, no. 10, pp. 1398–1400, Oct. 1928.

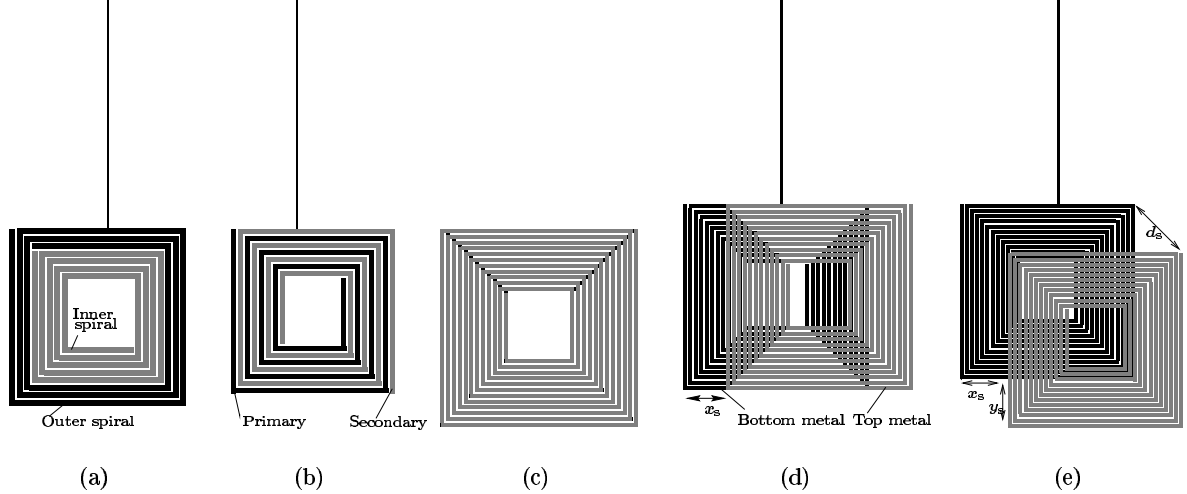
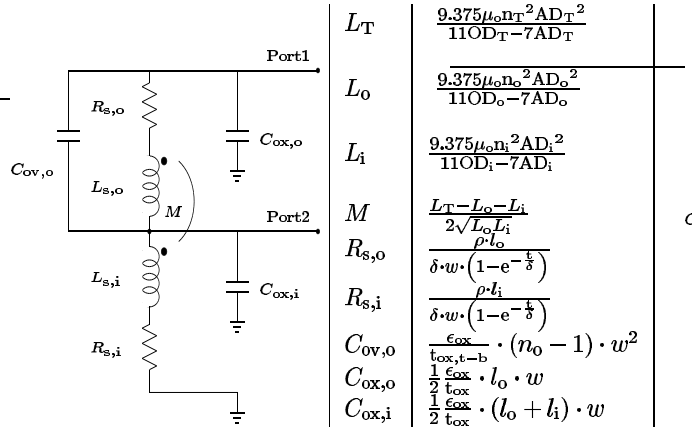
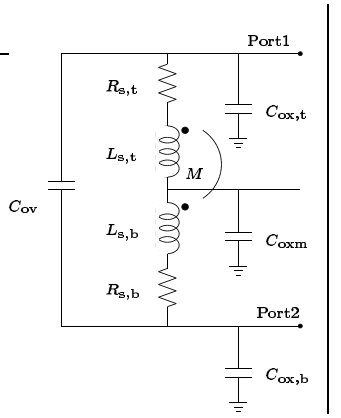


Figure 1: On-chip transformer realizations. (a)Tapped, (b)interleaved, (c)stacked with top spiral overlapping the bottom one, (d)stacked with top and bottom spirals laterally shifted, (e)stacked with top and bottom spirals diagonally shifted.



L_T	$\frac{9.375\mu_o n_T{}^2 AD_T{}^2}{11OD_T - 7AD_T}$
L_o	$\frac{9.375\mu_o n_o{}^2 AD_o{}^2}{11OD_o - 7AD_o}$
L_i	$\frac{9.375\mu_o n_i{}^2 AD_i{}^2}{11OD_i - 7AD_i}$
M	$\frac{L_T - L_o - L_i}{2\sqrt{L_o L_i}}$
$R_{s,o}$	$\frac{\rho \cdot l_o}{\delta \cdot w \cdot \left(1 - e^{-\frac{t}{\delta}}\right)}$
$R_{s,i}$	$\frac{\rho \cdot l_i}{\delta \cdot w \cdot \left(1 - e^{-\frac{t}{\delta}}\right)}$
$C_{ov,o}$	$\frac{\epsilon_{ox}}{t_{ox,t-b}} \cdot (n_o - 1) \cdot w^2$
$C_{ox,o}$	$\frac{1}{2}\frac{\epsilon_{ox}}{t_{ox}} \cdot l_o \cdot w$
$C_{ox,i}$	$\frac{1}{2}\frac{\epsilon_{ox}}{t_{ox}} \cdot (l_o + l_i) \cdot w$

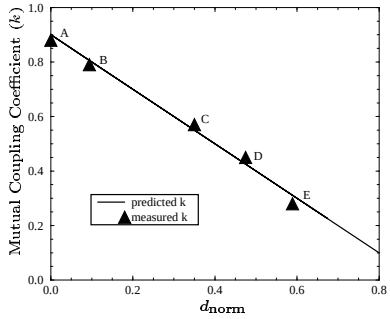
(a) Tapped transformer physical model. (Subscript 'o' refers to outer spiral, 'i' to inner spiral and 'T' to whole spiral)



L_t	$\frac{9.375\mu_o n^2 AD^2}{11OD - 7AD}$
L_b	L_t
k	$0.9 - d_s/\mathrm{AD}$
M	$k\sqrt{L_t L_b}$
$R_{s,t}$	$\frac{\rho_t \cdot l}{\delta_t \cdot w \cdot \left(1 - e^{-\frac{t_t}{\delta_t}}\right)}$
$R_{s,b}$	$\frac{\rho_b \cdot l}{\delta_b \cdot w \cdot \left(1 - e^{-\frac{t_b}{\delta_b}}\right)}$
C_{ov}	$\frac{1}{2}\frac{\epsilon_{ox}}{t_{ox,t-b}} \cdot l \cdot w \cdot \frac{A_{ov}}{A}$
$C_{ox,t}$	$\frac{1}{2}\frac{\epsilon_{ox}}{t_{ox,t}} \cdot l \cdot w \cdot \frac{A - A_{ov}}{A}$
$C_{ox,b}$	$\frac{1}{2}\frac{\epsilon_{ox}}{t_{ox,b}} \cdot l \cdot w$
C_{oxm}	$C_{ox,t} + C_{ox,b}$

(b) Stacked transformer physical model. (Subscript 't' refers to top spiral and 'b' to bottom spiral)

Figure 2: Analytical models for transformers. (ρ=DC metal resistivity, δ=skin depth, $t_{ox,t}$=oxide thickness from top metal to substrate, $t_{ox,b}$=oxide thickness from bottom metal to substrate, $t_{ox,t-b}$=oxide thickness from top level metal to bottom level metal, k is the coupling coefficient, n=number of turns, OD=outer diameter, AD=average diameter(= $(OD + ID)/2$), ID=inner diameter, l=length of spiral, w=turn width, t=metal thickness, A=area, A_{ov}=overlapped area of top and bottom spirals, d_s=center-to-center spiral distance)



	x_s (μm)	y_s (μm)	$d_s = \sqrt{{x_s}^2 + {y_s}^2}$	$d_{norm} = (\frac{d_s}{AD})$	$k_{predict} = (0.9 - d_{norm})$	k_{meas}
A	0	0	0	0	0.9	0.88
B	8	8	11	0.09	0.81	0.79
C	42	0	42	0.35	0.55	0.57
D	57	0	57	0.48	0.42	0.45
E	50	50	71	0.59	0.31	0.28

Figure 3: Coupling coefficient (k) versus normalized shift (d_{norm}) for 20nH inductors on a patterned ground shield [5]. (n = 11.75, OD = 180μm, w = 3.2μm, AD = 120μm, t_t = 2.1μm, t_b = 0.6μm, $\rho_t = 3\mu\Omega \cdot$ cm, $\rho_b = 5\mu\Omega \cdot$ cm, $t_{ox,t}$ = 3.5μm, $t_{ox,b}$ = 2.2μm, $t_{ox,t-b}$ = 0.8μm)

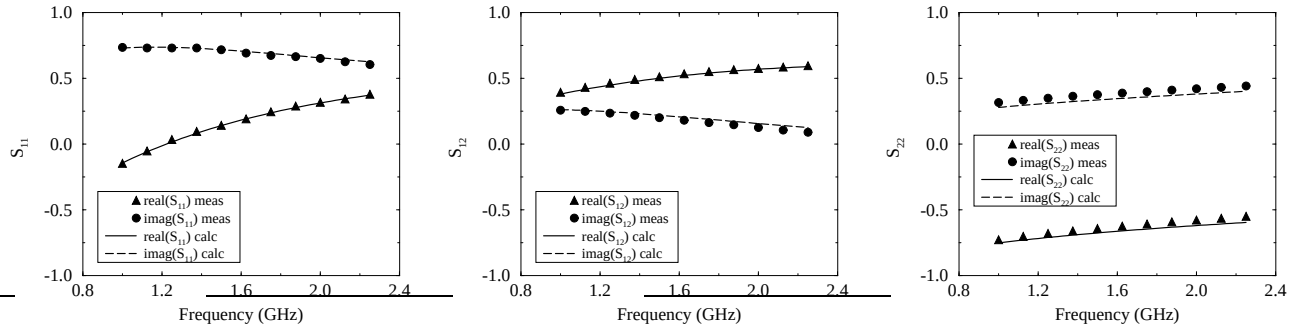


Figure 4: Tapped transformer on quartz wafer. ($n_o = 2.5$, $n_i = 4.25$, $OD_o = 290\mu m$, $OD_i = 190\mu m$, $AD_o = 247\mu m$, $AD_i = 112\mu m$, $w = 13\mu m$, $t = 2\mu m$, $\rho = 3\mu\Omega \cdot cm$, $t_{ox} = 3.5\mu m$, $t_{ox,t-b} = 0.8\mu m$)

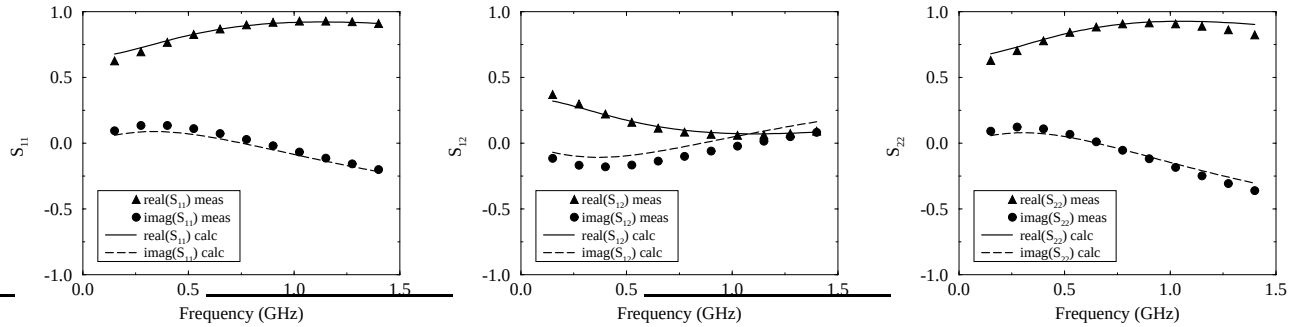


Figure 5: Stacked transformer on PGS with top spiral overlapping the bottom one. (Transformer A in Fig. 3).

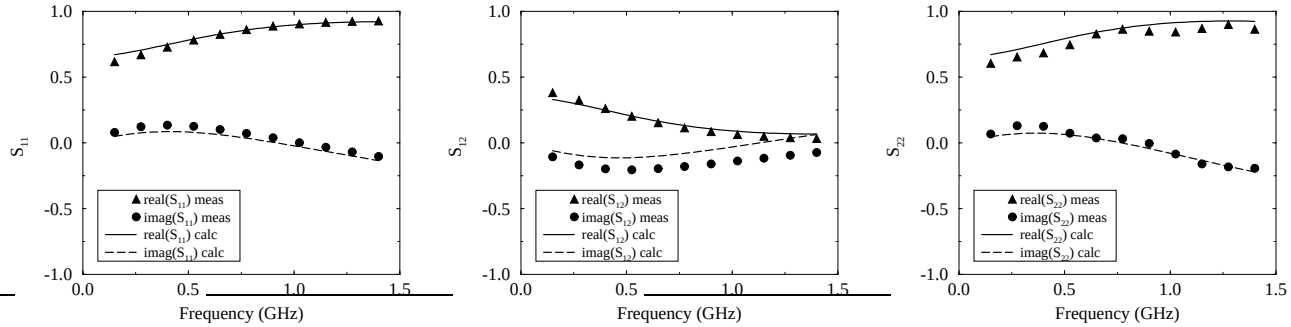


Figure 6: Stacked transformer on PGS with top and bottom spirals laterally shifted. (Transformer C in Fig. 3).

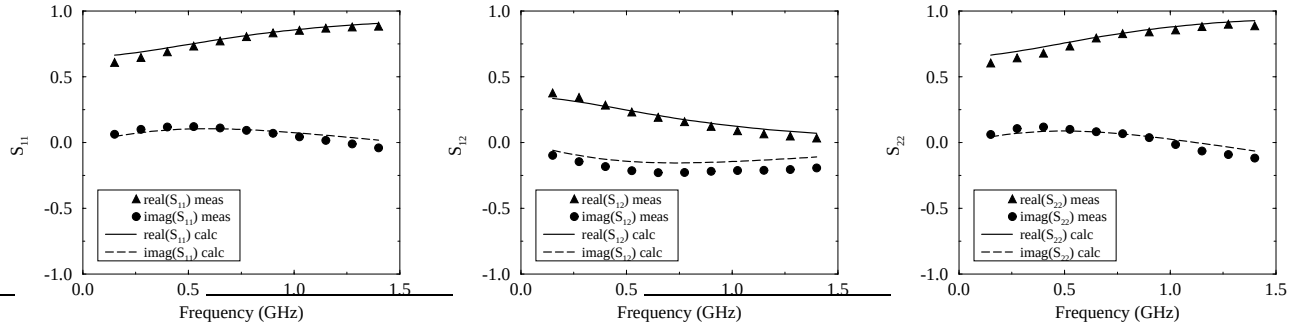


Figure 7: Stacked transformer on PGS with top and bottom spirals diagonally shifted. (Transformer E in Fig. 3).