Modeling and Characterization of On-Chip Transformers

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OUTLINE

- Motivation
- Background
- On-chip transformer realizations
- Models
- Experimental verification
- Summary

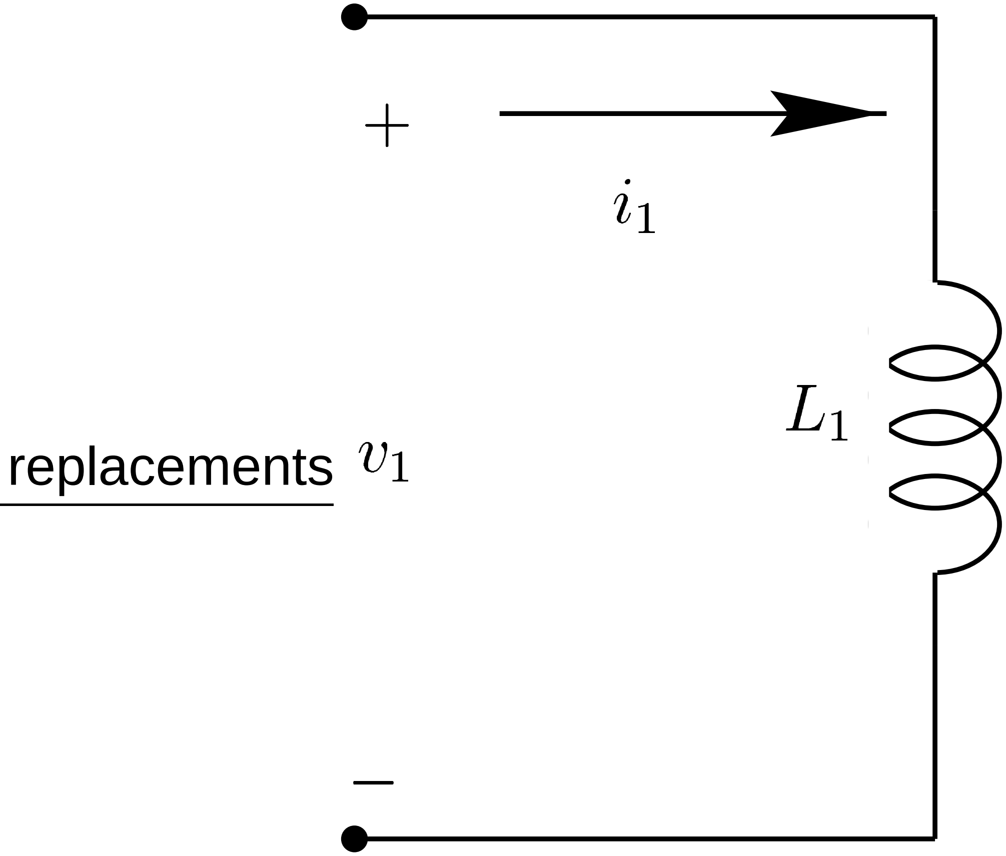
MOTIVATION FOR TRANSFORMER MODELING

- Essential for Radio Frequency Integrated Circuits (RFICs)

- 3-D field solvers are **inconvenient**
  - Numerically expensive and cumbersome
  - Good for **verification** but not for **design**

- **Scalable, analytical models**
  - Design **guidelines** and explore **trade-offs**
  - Circuit **design** and **optimization**

SELF-INDUCTANCE

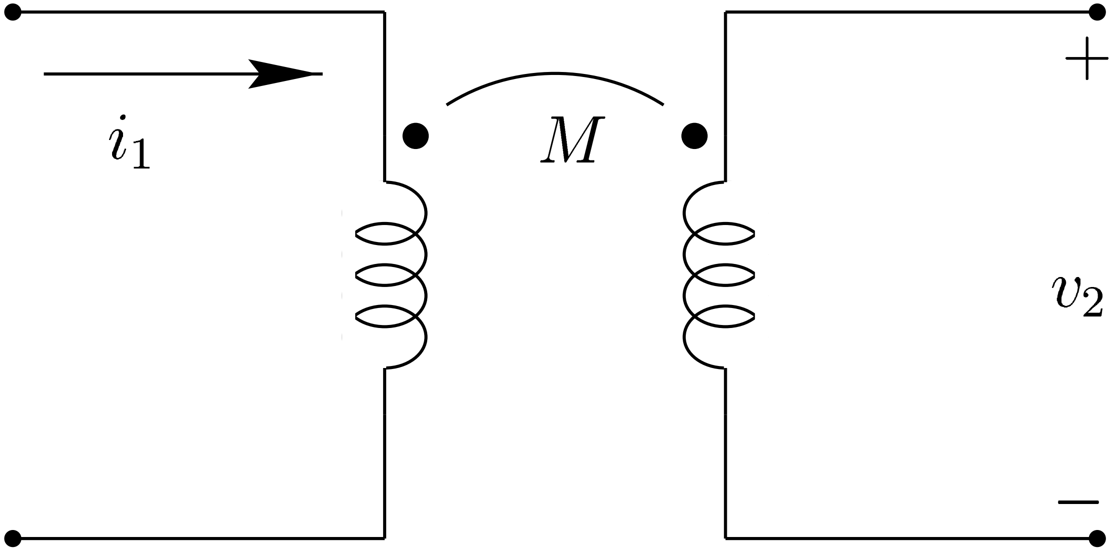


Quantity	Units
i_1	A
v_1	V
t	s
L_1	H

- $v_1 = L_1 \frac{\partial i_1}{\partial t}$
- nH typical in RF On-chip environment

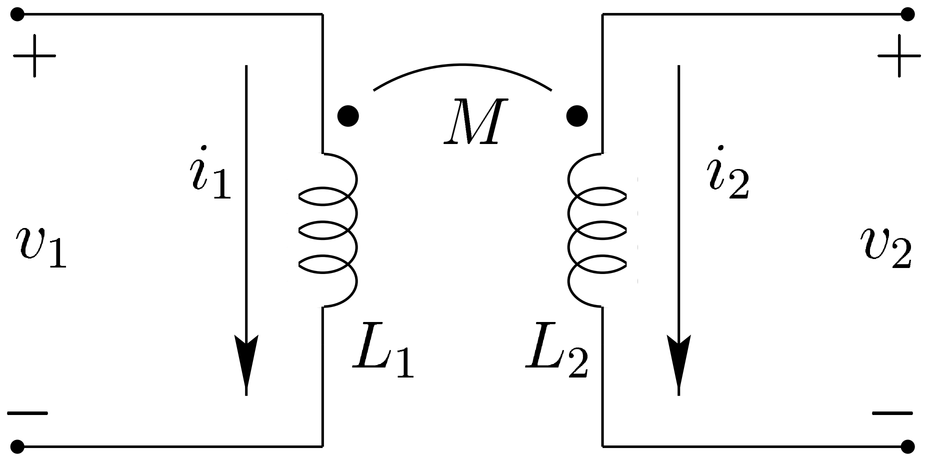
MUTUAL INDUCTANCE

PSfrag replacements



$$v_2 = M\frac{\partial i_1}{\partial t}$$

TRANSFORMER



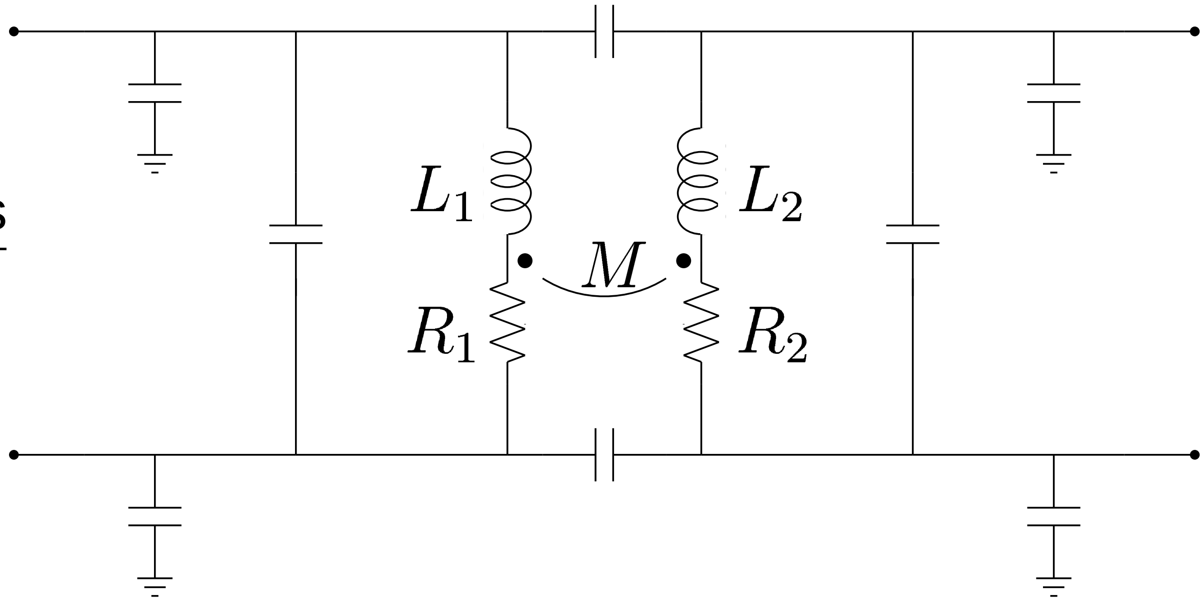
- $v_1 = L_1 \frac{\partial i_1}{\partial t} + M \frac{\partial i_2}{\partial t}$

  $v_2 = L_2 \frac{\partial i_2}{\partial t} + M \frac{\partial i_1}{\partial t}$

- Mutual coupling coefficient, $k = \frac{M}{\sqrt{L_1 L_2}}$
- $|k| \leq 1$

NON-IDEAL TRANSFORMER

nents



- $k = \frac{M}{\sqrt{L_1 L_2}} < 1$.
- Series resistance.
- Port-to-port & port-to-substrate capacitances

CONFIGURATIONS

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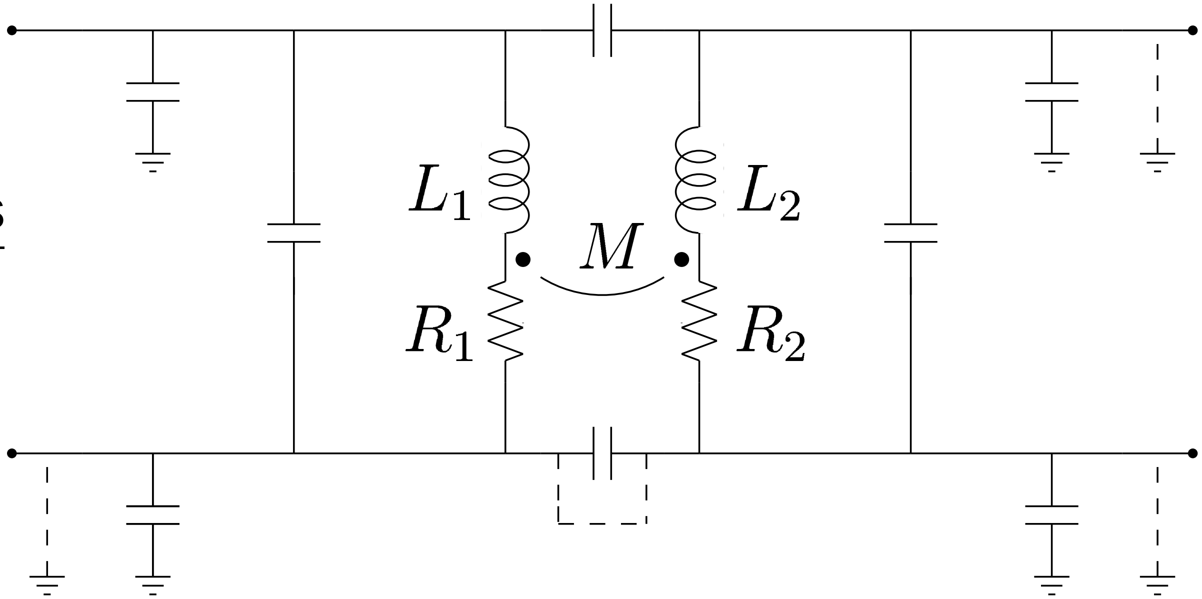
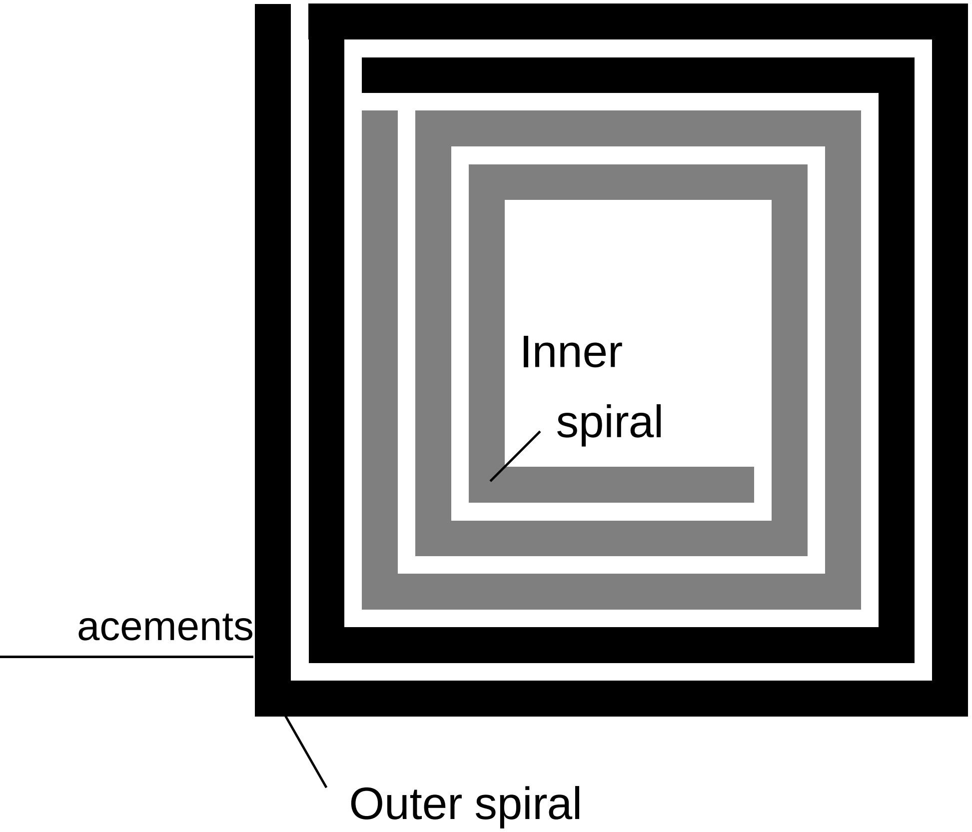


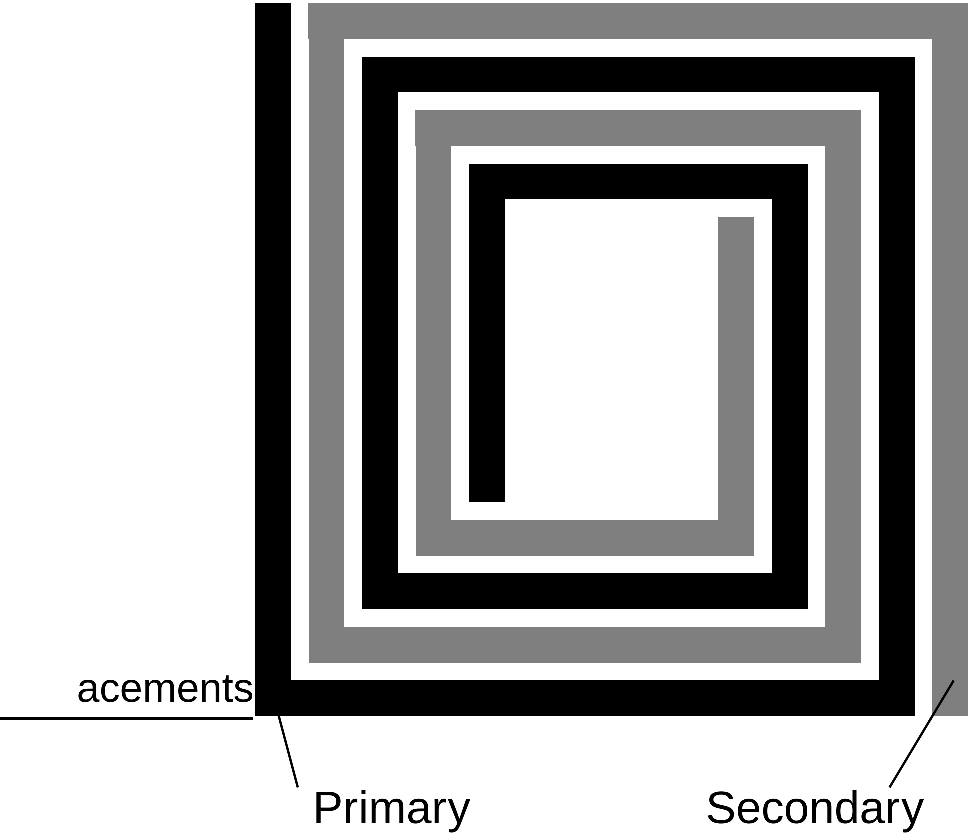
- Three or four terminal device
- Grounded terminals

TAPPED TRANSFORMER



- Low $k (\approx 0.3 - 0.5)$
- High L_1, L_2
- Top metal layer
- Asymmetric
- Low port-to-port capacitance

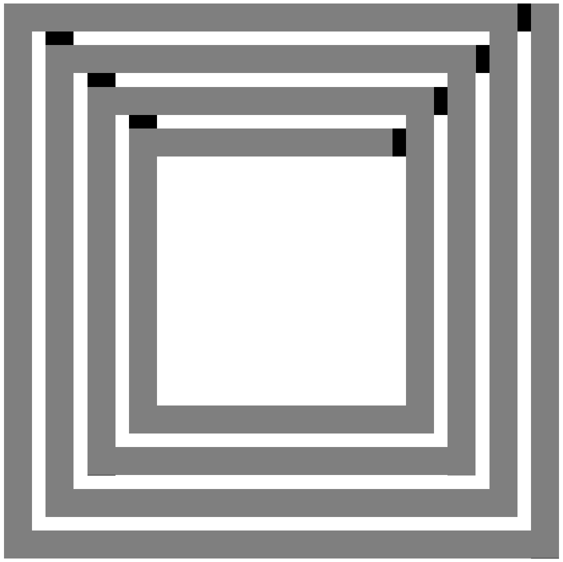
INTERLEAVED TRANSFORMER



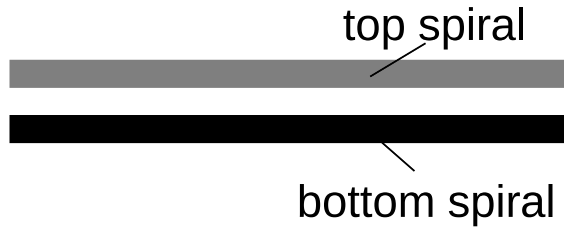
- Medium $k (\approx 0.7 - 0.8)$
- Low L_1, L_2
- Top metal layer
- Symmetric
- Medium port-to-port capacitance

STACKED TRANSFORMER

Top View

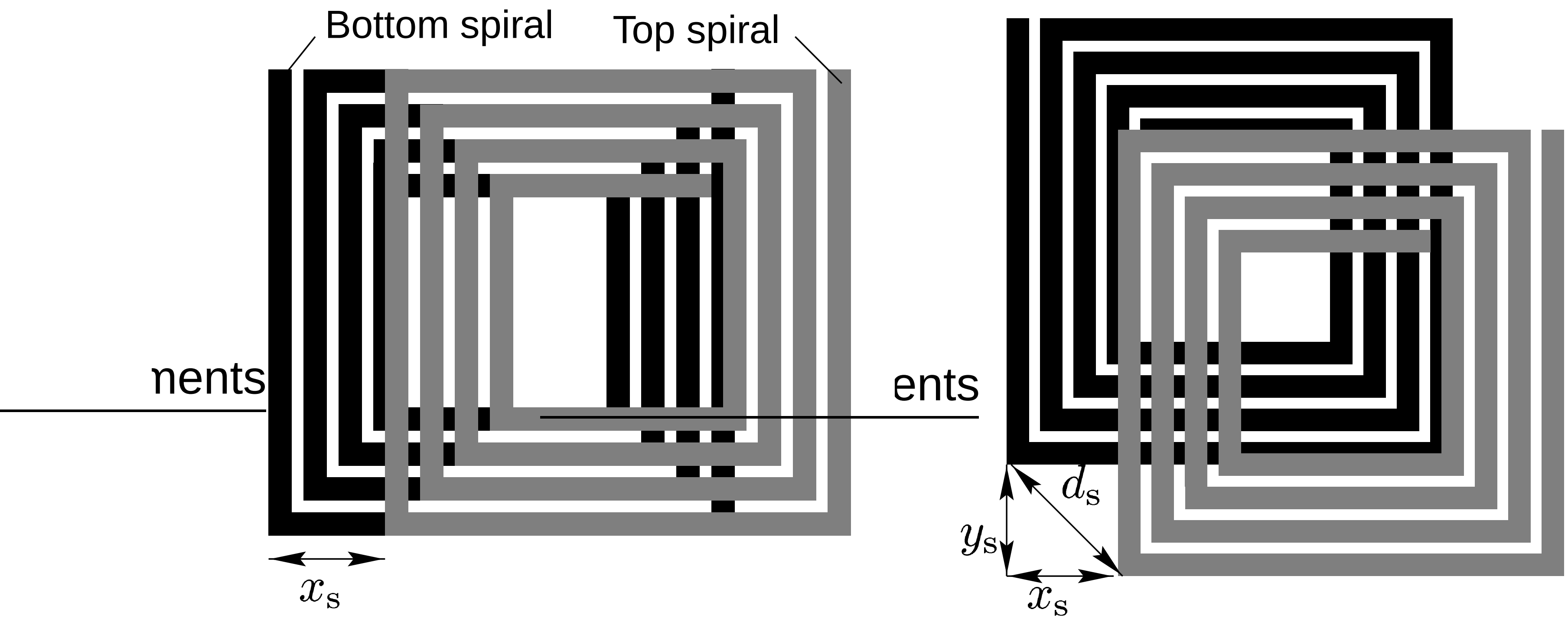


Side View



- High $k (\approx 0.9)$
- High L_1, L_2
- Multiple metal layers
- Area efficient
- High port-to-port & port-to-substrate capacitances

STACKED TRANSFORMER VARIATIONS



- Shift top and bottom spirals laterally or diagonally
- Trade-off lower k for reduced port-to-port capacitance

COMPARISON OF TRANSFORMER REALIZATIONS

Transformer type	**Area**	**Coupling coefficient, k**	**Self-inductance**	**Self-resonant frequency**
Tapped	High	Low	Mid	High
Interleaved	High	Mid	Low	High
Stacked	Low	High	High	Low

- Non-idealities result in trade-offs
- Optimal choice determined by circuit application
- Transformer **models** needed for comparison

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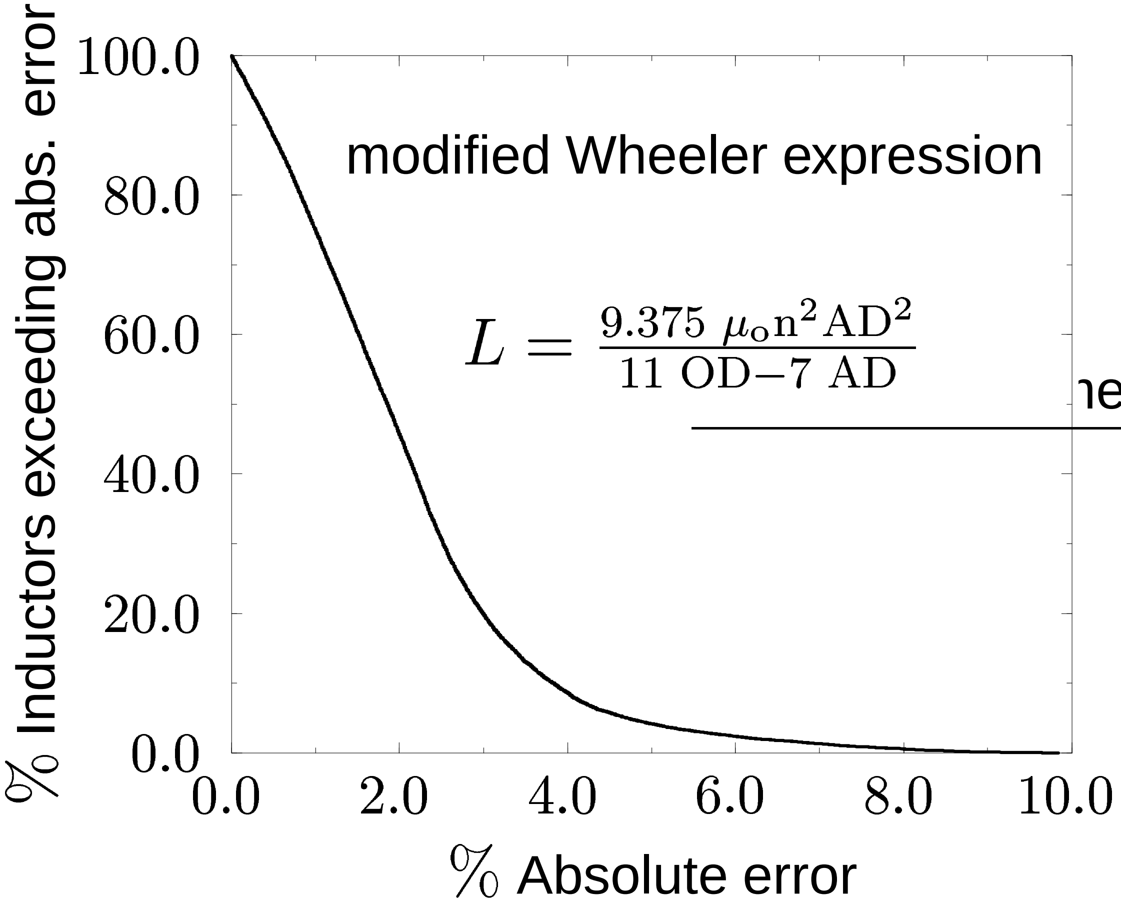
SELF-INDUCTANCE CALCULATION



modified Wheeler expression

$$L = \frac{9.375\ \mu_o \mathrm{n}^2 \mathrm{AD}^2}{11\ \mathrm{OD} - 7\ \mathrm{AD}}$$

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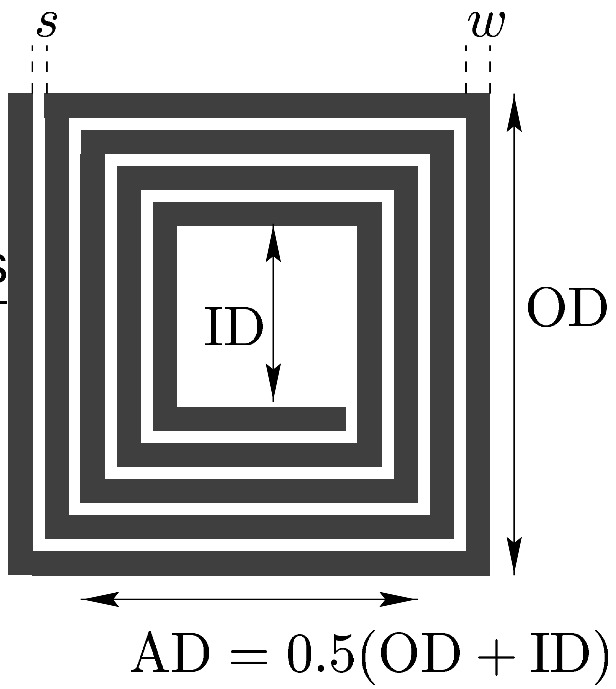
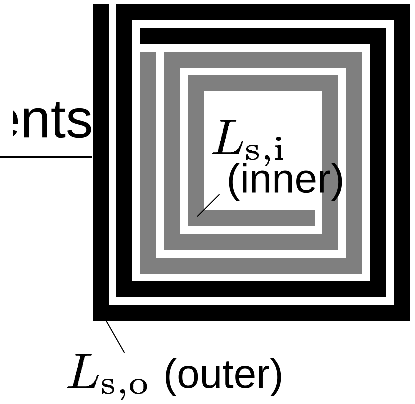


$\mathrm{AD} = 0.5(\mathrm{OD} + \mathrm{ID})$

- Verified by measurements (75) and 3-D field solver simulations (17,000)

TAPPED TRANSFORMER MODEL



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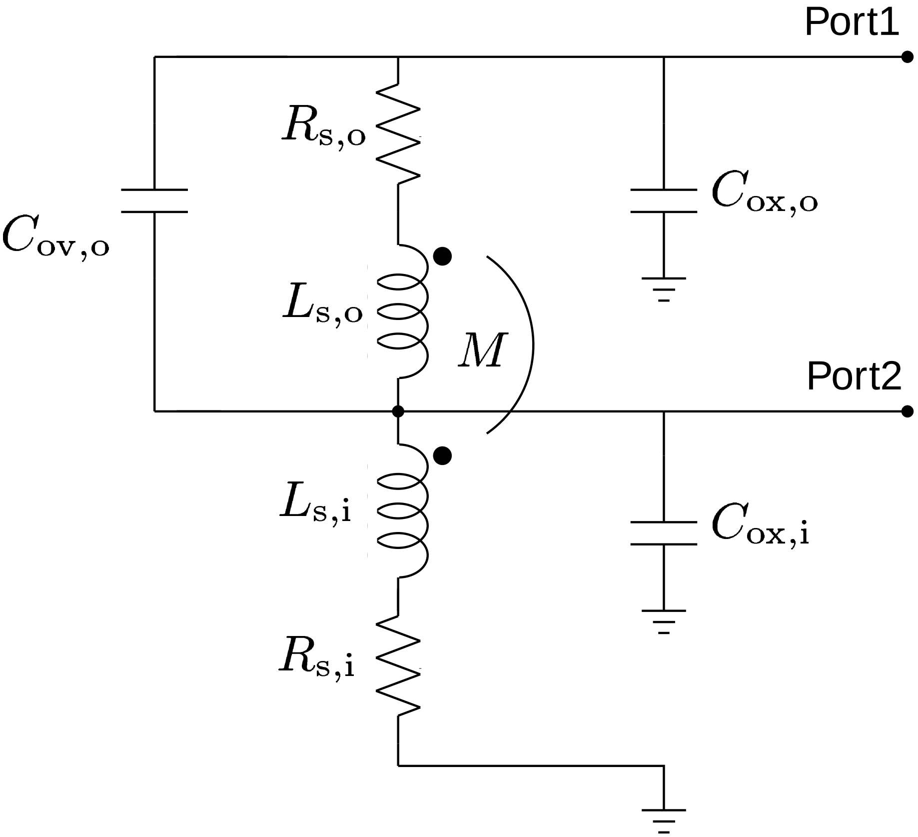
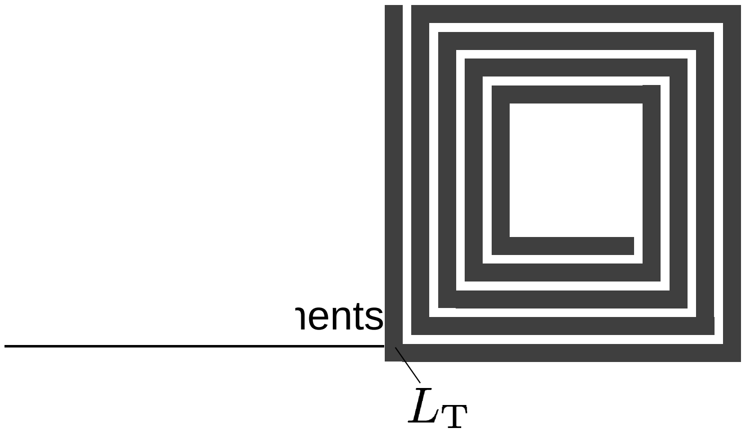


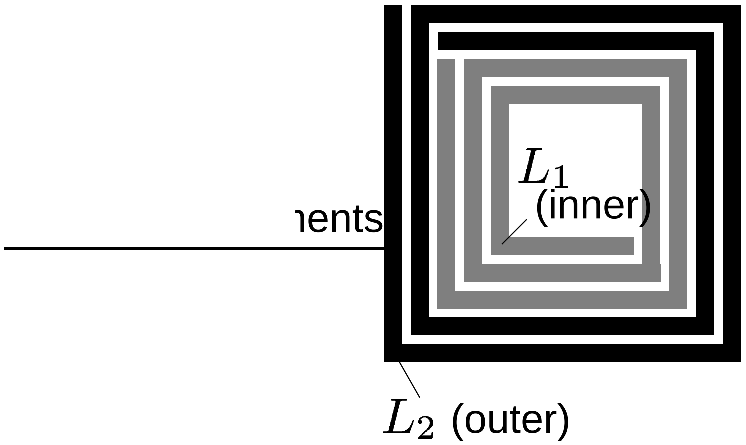
- Evaluate $C_{\mathrm{ov,o}}$, $C_{\mathrm{ox,o}}$, $C_{\mathrm{ox,i}}$, $R_{\mathrm{s,o}}$ & $R_{\mathrm{s,i}}$ by extending previous work
- Use modified Wheeler expression for $L_{\mathrm{s,o}}$, $L_{\mathrm{s,i}}$
- Calculate M

MUTUAL INDUCTANCE CALCULATION

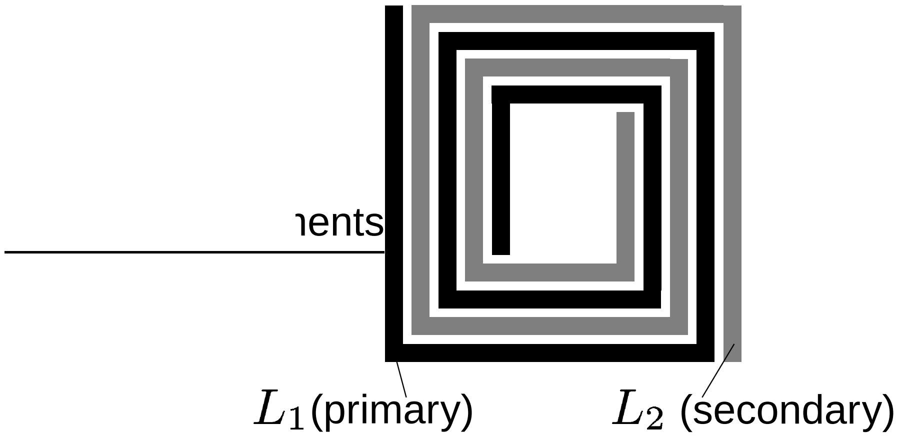
Single inductor.



Tapped transformer.



Interleaved transformer.



- $L_T = L_1 + L_2 + 2M$

k FOR TAPPED AND INTERLEAVED TRANSFORMERS

1. Find L_1, L_2 and L_T
2. Determine M from $M = 0.5(L_\mathrm{T} - L_1 - L_2)$
3. Evaluate $k = \frac{M}{\sqrt{L_1 L_2}}$

STACKED TRANSFORMER MODEL

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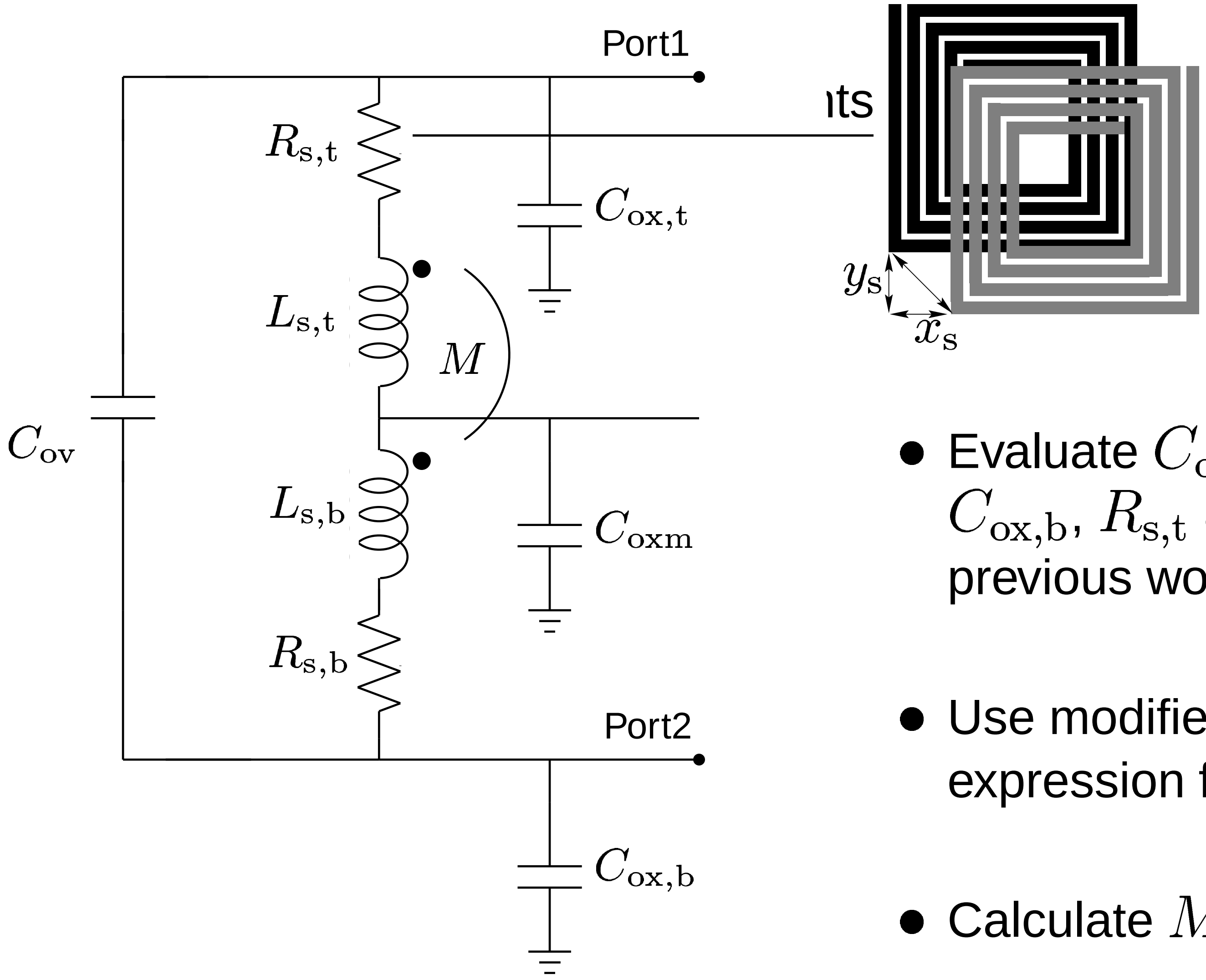
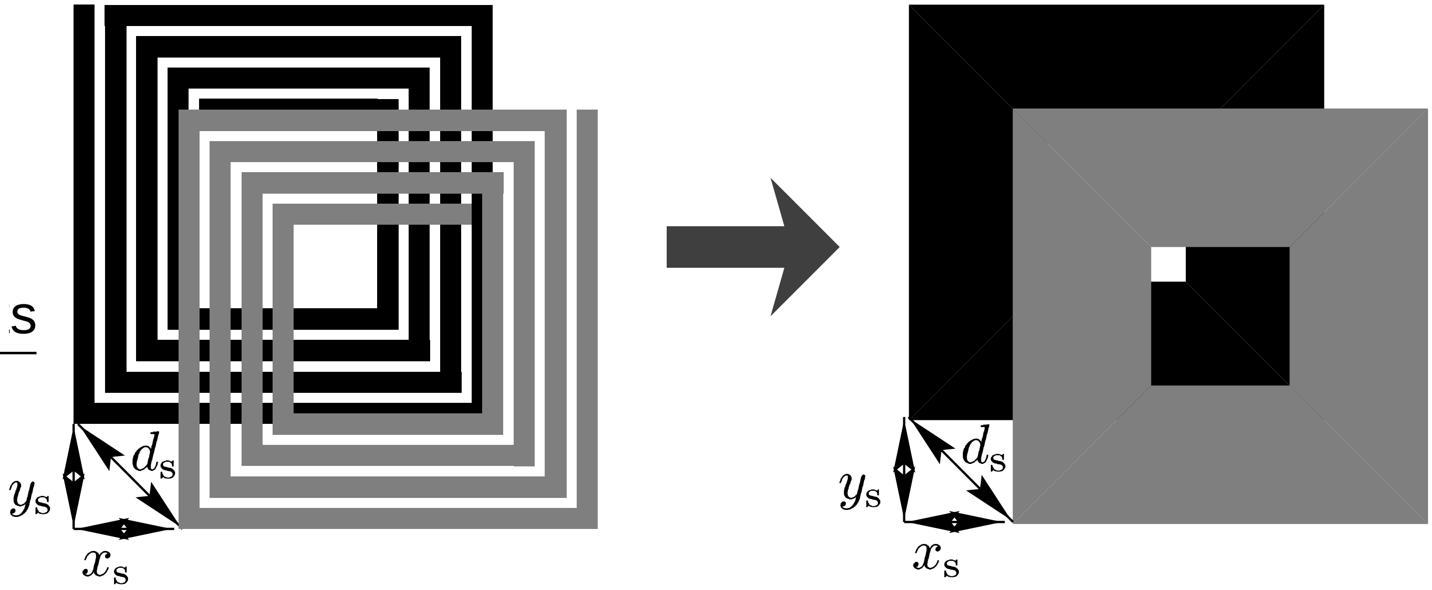


- Evaluate C_{ov}, $C_{\mathrm{ox,t}}$, C_{oxm}, $C_{\mathrm{ox,b}}$, $R_{\mathrm{s,t}}$ & $R_{\mathrm{s,b}}$ by extending previous work
- Use modified Wheeler expression for $L_{\mathrm{s,t}}$, $L_{\mathrm{s,b}}$
- Calculate M

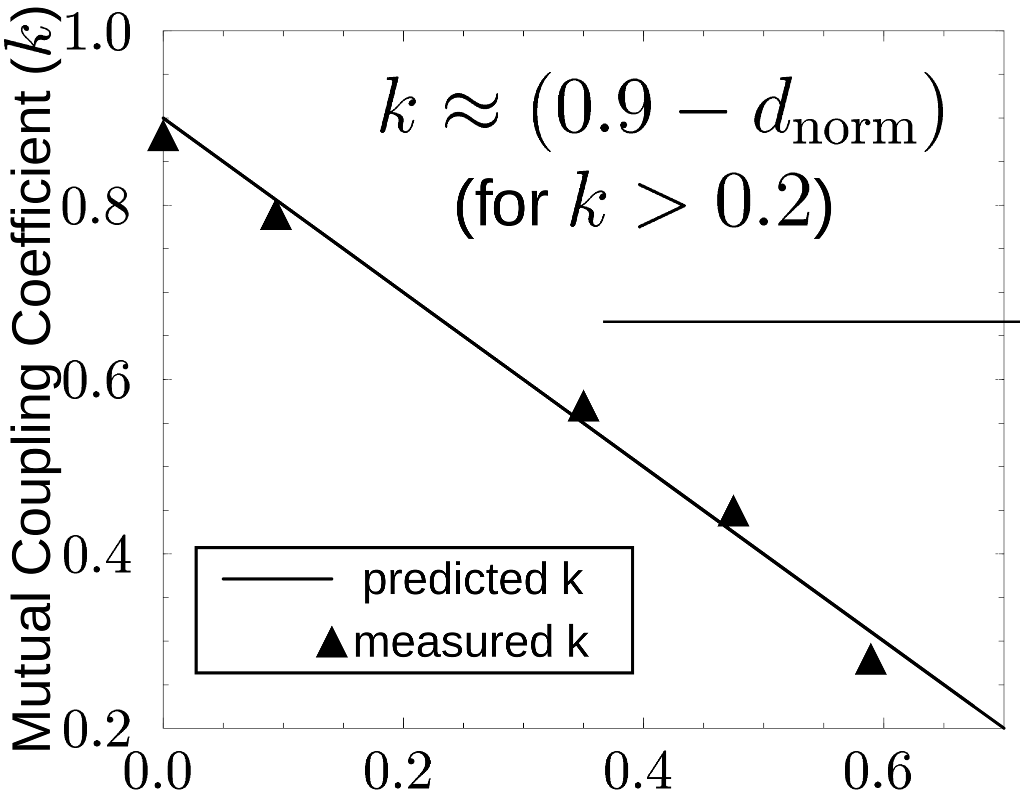
CURRENT SHEET APPROACH FOR k



- Reduce complexity by $4n^2$
- Use symmetry
- Derive simple expression using electromagnetic theory

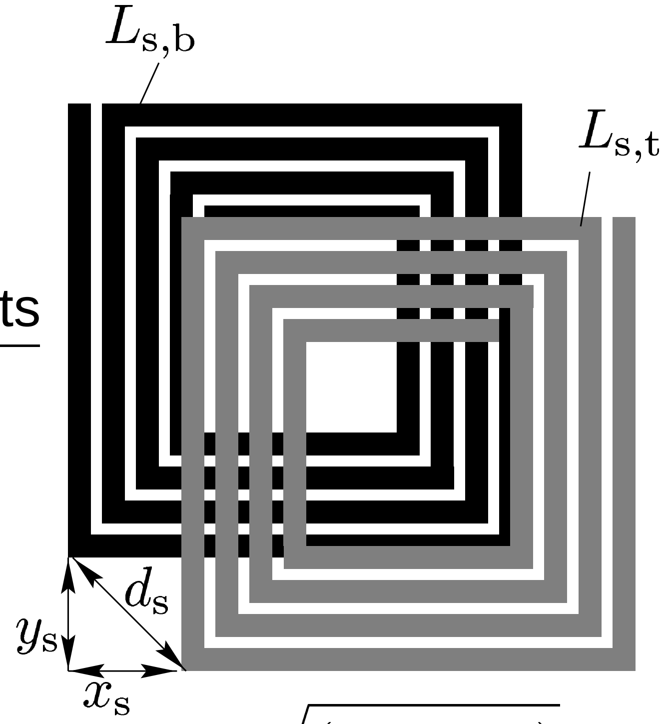
k FOR STACKED TRANSFORMERS

acements



$$k \approx (0.9 - d_{\mathrm{norm}})$$

(for $k > 0.2$)



$$M = k\sqrt{(L_{\mathrm{s,t}} L_{\mathrm{s,b}})}$$

$$d_{\mathrm{norm}} = \frac{\sqrt{{x_{\mathrm{s}}}^2 + {y_{\mathrm{s}}}^2}}{\mathrm{AD}} = \frac{d_{\mathrm{s}}}{\mathrm{AD}}$$

- Metal and oxide thicknesses have only 2nd order effects on k

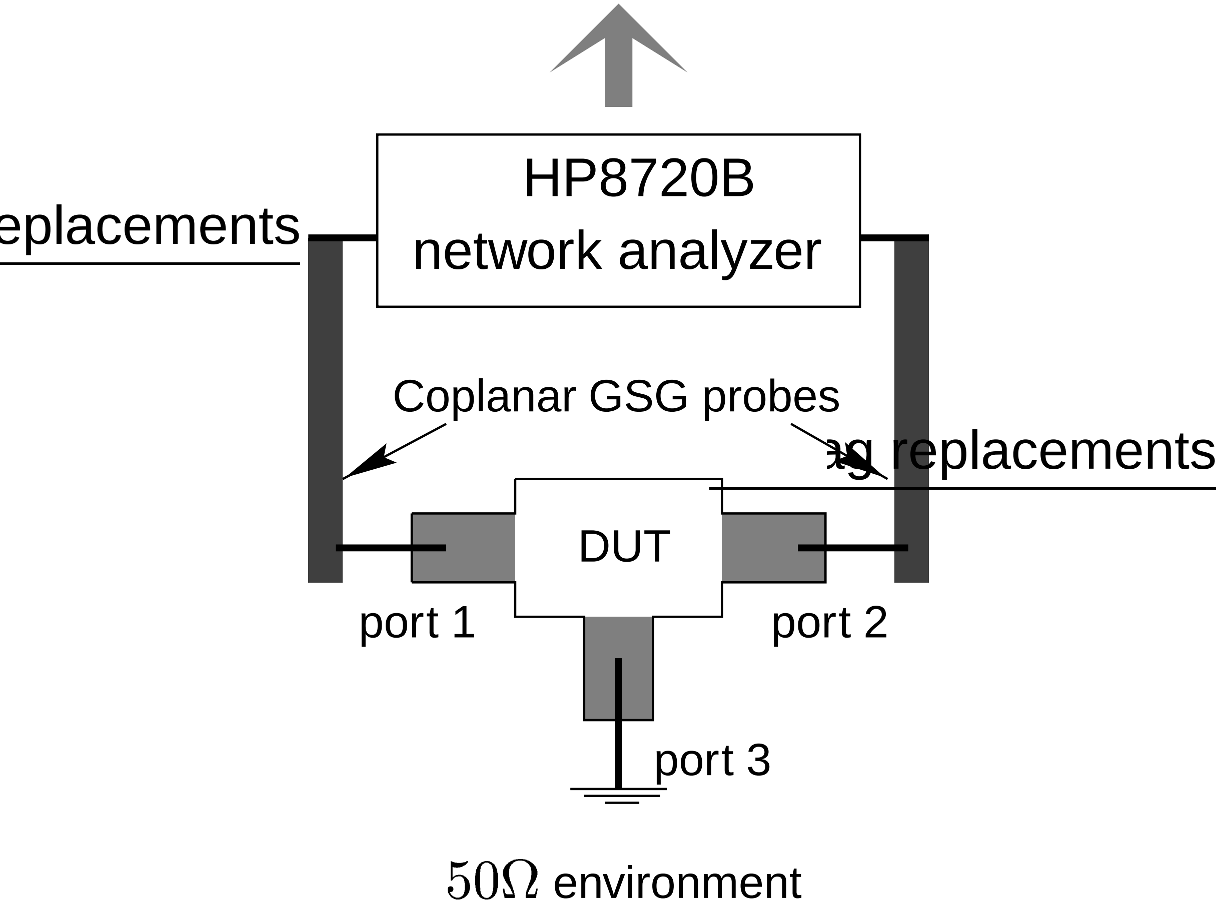
M FOR STACKED TRANSFORMERS

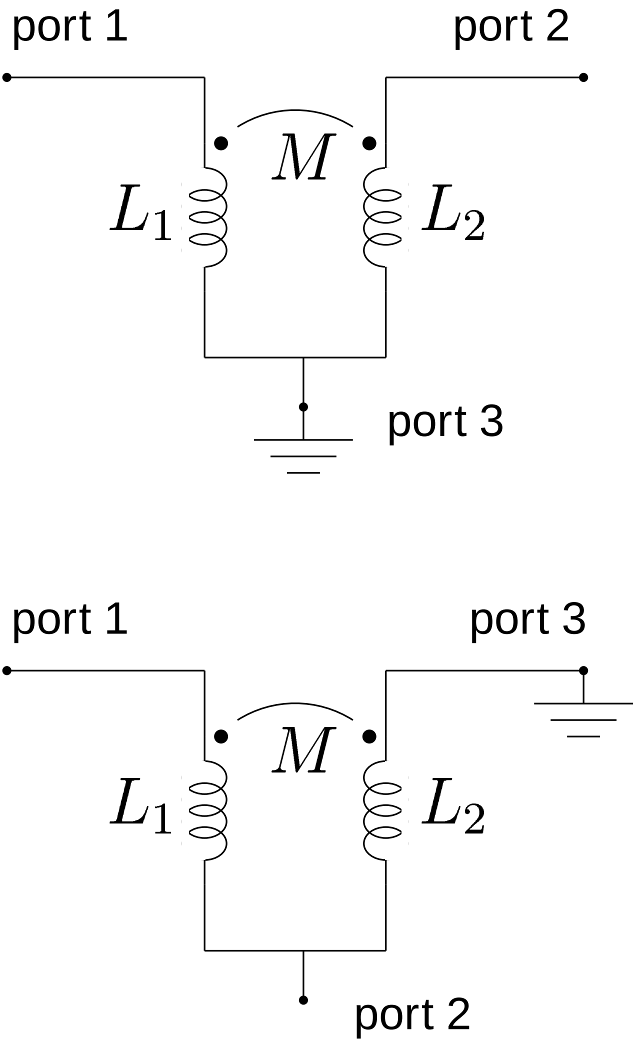
1. Find L_1 and L_2
2. Determine k
3. Evaluate $M = k\sqrt{L_1 L_2}$

ACCURACY OF MODELS

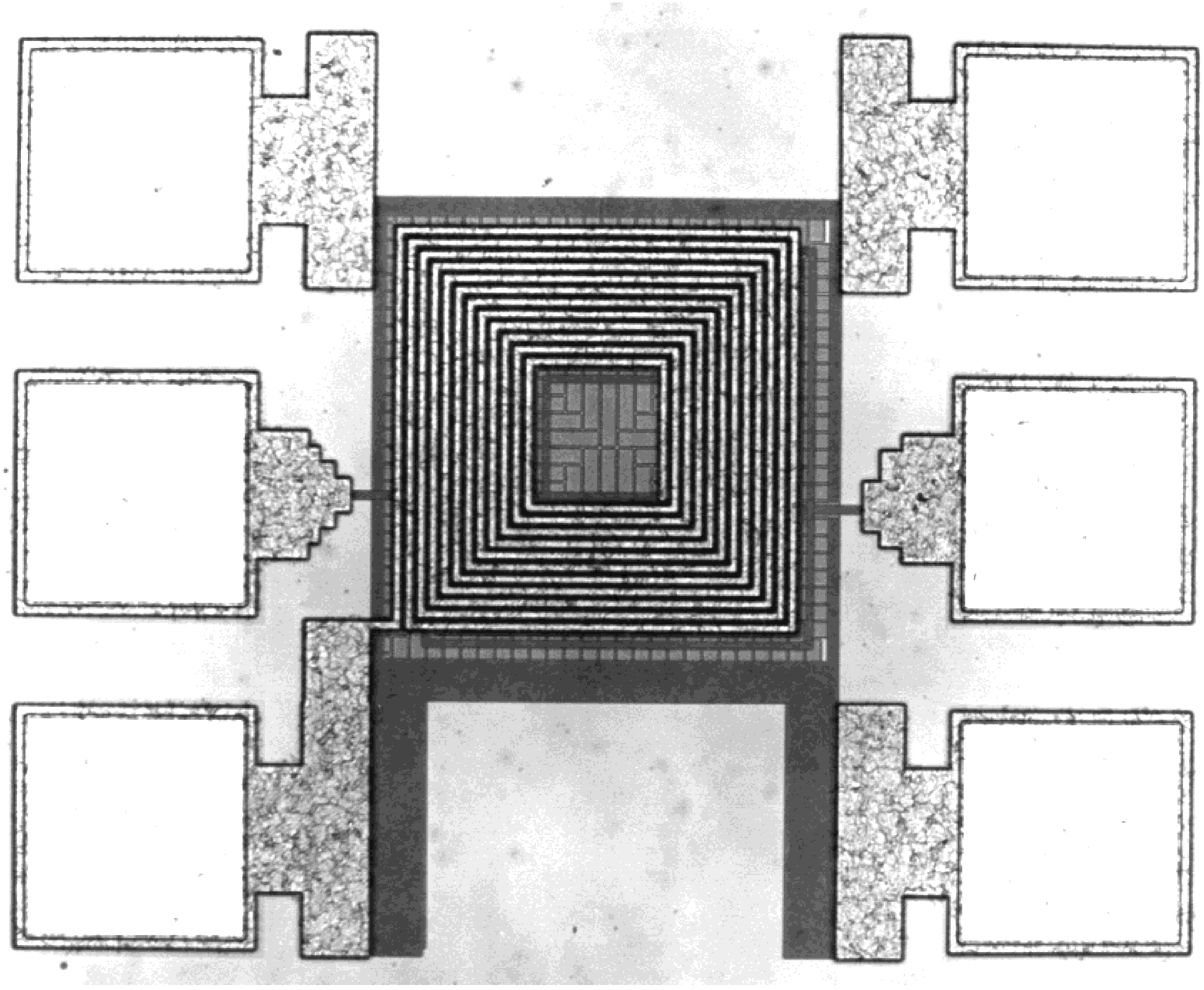
- Lumped model of distributed structure
- Substrate not modeled
- Patterned Ground Shield (PGS)
  - Eliminates resistive and capacitive coupling to substrate
  - Inductive coupling to substrate may degrade performance at high frequencies

EXPERIMENTAL SET-UP





DIE PHOTO

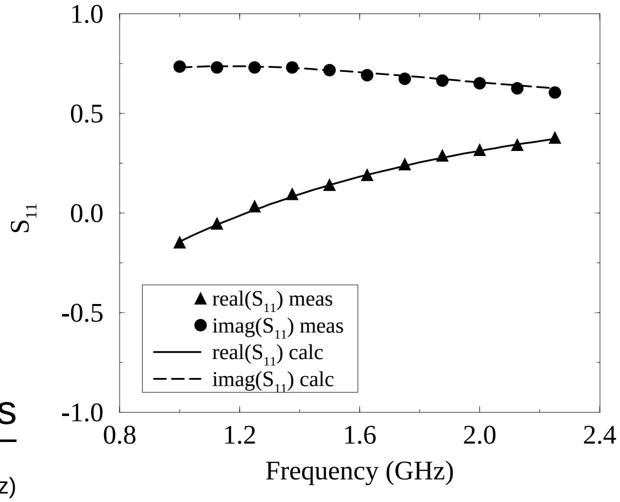


EXPERIMENTAL VERIFICATION: TAPPED

- $\mathrm{OD_o} = 290\mu\mathrm{m}$,
  $n_\mathrm{o} = 2.5$
- $\mathrm{OD_i} = 190\mu\mathrm{m}$,
  $n_\mathrm{i} = 4.25$
- $w = 13\mu\mathrm{m}$, $s = 7\mu\mathrm{m}$

PSfrag replacements

Frequency(GHz)



PSfrag replacements

Frequency(GHz)

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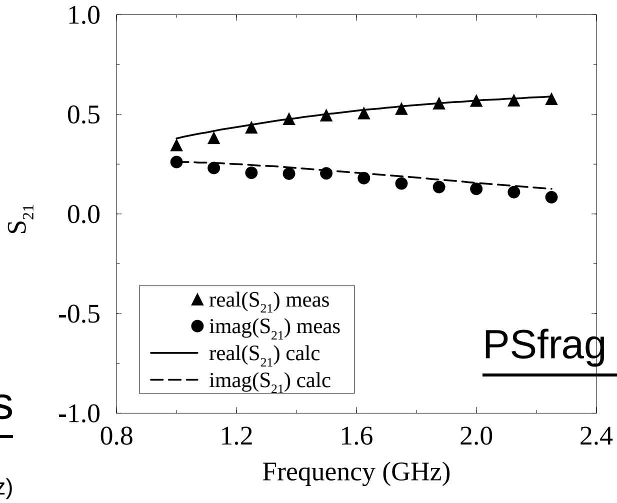
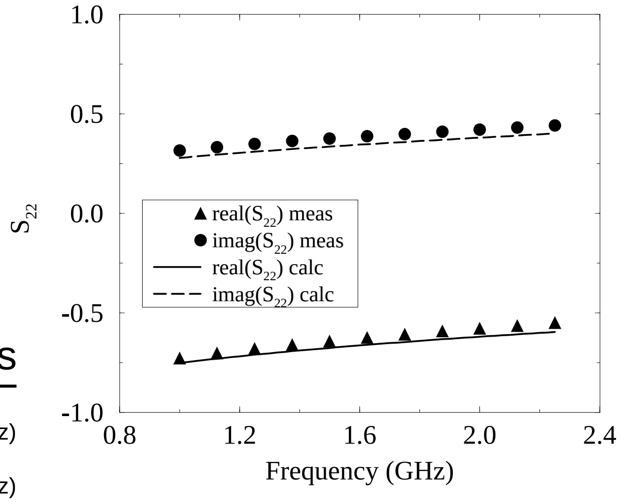


ag replacements

Frequency(GHz)

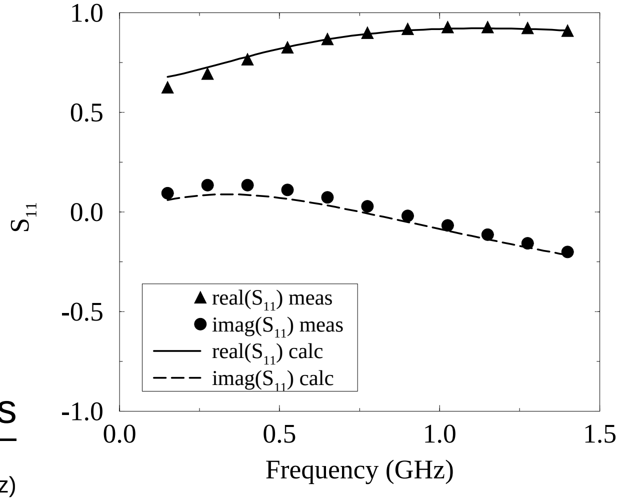


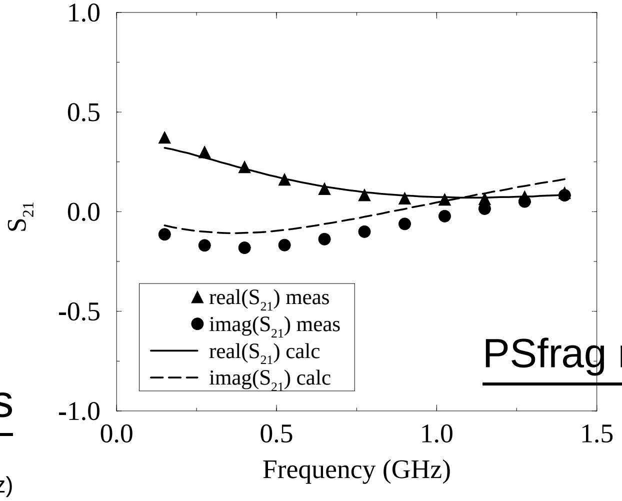
EXPERIMENTAL VERIFICATION: STACKED 1

- Stacked transformer with top spiral overlapping bottom one
- $\mathrm{OD} = 180\mu\mathrm{m}, n = 11.75$, $w = 3.2\mu\mathrm{m}$, $s = 2.1\mu\mathrm{m}$
- $x_\mathrm{s} = 0\mu\mathrm{m}$, $y_\mathrm{s} = 0\mu\mathrm{m}$, $d_\mathrm{s} = 0\mu\mathrm{m}$

PSfrag replacements

Frequency(GHz)





PSfrag replacements

Frequency(GHz)

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ag replacements

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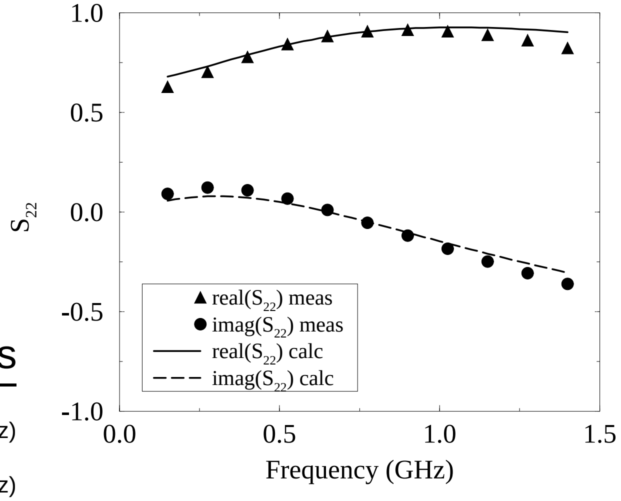

CONTRIBUTIONS

- On-chip transformer models
- Expressions for mutual inductance and mutual coupling coefficient
- Models verified by measurements
- Basis for design and optimization of transformer circuits

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