29.10 A 17mW 0.66mm² Direct-Conversion Receiver for 1Mb/s Cable Replacement

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Currently, there is an increasing demand for low-cost nodes that consume very little power for wireless personal area network (WPAN) applications. Much of the difficulty in hardware design for such devices comes from early design decisions made at the system level, and is thus highly dependent on the applications for which the system is being designed. For example, Bluetooth, currently a popular WPAN standard in the 2.4GHz ISM band, aims to remove wires for both voice and data applications that require data rates less than 1Mbps over distances less than 10m. Until now, however, the cost of a Bluetooth node that meets its minimum requirements (Class 3) is still too high for wide consumer acceptance. A major reason is that Bluetooth is designed to accommodate a wide range of applications. For example, the Bluetooth standard supports synchronous connections due to latency requirements associated with voice traffic. To allow for such flexibility the demands on the hardware are stringent, resulting in high cost. In this work, we focus on the design of an RF receiver front-end for a system where cost is the primary concern. For this receiver, we integrate the high-pass filter (HPF) following the mixer by employing a new coding scheme that shapes the data spectrum away from baseband. Additionally, we eliminate the expensive, external band-preselect filter by using an extremely linear low-noise amplifier (LNA) and mixer capable of accommodating out-of-band blockers. Also, we integrate the loop filter in the frequency synthesizer by employing MOS capacitors and unsilicided poly resistors. The only off-chip components that would be required for this receiver are a crystal and an antenna. This makes it possible to lower the cost of this receiver to 30 cents.

The system specification, which we call 'Zero-G', supports the same data rates over similar distances as Bluetooth, except that we make some system-level trade-offs to ease the circuit design to reduce cost and power. Zero-G allows for operation of wireless devices in the 2.4GHz ISM band, with 6 channels of operation at frequencies of $(2400 + 12n)$MHz, where n = 1..6. It utilizes a differential binary phase-shift keying (DBPSK) modulation scheme, and a 10b 'offset code' for spectrum shaping [1]. This coding scheme allows us to easily use the area-efficient direct-conversion architecture in the receiver. This scheme allows for size reduction in the capacitor in the HPF following the downconversion mixer, and shapes the spectrum of the differentially-encoded data to meet the FCC CFR47.15.247 bandwidth requirement [3]. A higher cut-off frequency (50kHz) in the HPF also results in faster overload recovery in the receiver.

The block diagram of the whole receiver is shown in Fig. 29.10.1. The 0dB/20dB dual-gain LNA drives two I/Q passive transmission-gate mixers and passive filtering chain, the outputs of which are buffered and driven off-chip. A frequency synthesizer, which utilizes a multiply-by-3 voltage-controlled ring oscillator (VCO) [5], generates the local oscillator (LO) signal for the quadrature passive mixers. The output of the synthesizer feeds the I-Q phase-splitting buffers that drive the LO port of the mixers, and provides desired isolation between the mixers and the VCO.

According to the Bluetooth out-of-band blocker specification [2], signals as strong as –10dBm may exist 500MHz away from the desired band at the output of the antenna. Since we have eliminated the expensive band-preselect external filter, the receiver front-end must have sufficient linearity to handle the out-of-band blockers. The LNA (Fig. 29.10.2) has a pseudo-differential architecture, allowing for a large linear operating range without a large quiescent tail current source. The two gain settings of the LNA are determined by the cascode voltages LNA1 and LNA10. Capacitors C1 and C2 are present to increase design flexibility in the LNA [4]. Next, since the blocker linearity demands on the mixer following the LNA are stringent, a transmission-gate passive mixer is used (Fig. 29.10.3). If the transmission gate is conducting, the individual I-V characteristics of the NMOS and PMOS devices saturate for large V_{DS} variations about the nominal biasing point. This occurs because the devices go into the saturation region of operation. However, it can be seen from Fig 29.10.3 that the combined I-V characteristic of the NMOS/PMOS pair remains linear over a wide range of V_{DS}, resulting in enhanced conversion gain over a wider range of input amplitudes. After downconversion, a second-order low-pass passive filtering chain attenuates the strong blockers. The first-order low-pass filtering of the mixer itself provides additional filtering. To study the behavior of a transmission-gate mixer, a stand-alone passive chain structure was built and tested at 1GHz. Figure 29.10.4 shows the measured results of the 1-dB compression point test due to a blocker (P_{b1dB}). Two input signals were input into the mixer, 500MHz apart. The conversion gain of the weak desired signal was observed while the power of the blocker signal was varied. For this test, all the input ports of the mixer were resistively terminated, and the LO signal was applied externally. According to the figure, a 7dB improvement was observed when the PMOS devices were active, resulting in a P_{b1dB} of +5dBm. We also measured a 7dB improvement in the IIP3 of the standalone passive chain, resulting in an IIP3 value of +16dBm. There was an improvement of 6dB in the P_{b1dB} for the full implemented receive chain with the activation of the PMOS device in the transmission gate. The receiver chain was characterized at 1.87GHz rather than the desired 2.4GHz since some capacitance estimation errors shifted the resonance frequency.

The frequency synthesizer in this chip (Fig. 29.10.5) employs a multiply-by-3 VCO [5], which provides frequency outputs at 800MHz and 2.4GHz. The PLL closes around the low-frequency output, while the high-frequency output drives the LO buffers. The inter-channel spacing specification for the Zero-G system results in a –111dBc/Hz phase noise requirement for the oscillator, at an offset frequency of 24MHz. The multiply-by-3 ring oscillator easily meets this specification and allows for power savings in the input prescaler of the frequency synthesizer. The fully-integrated integer-N frequency synthesizer has a second-order loop filter, implemented with MOS capacitors and an unsilicided resistor. The charge pump has been implemented without cascoding to allow ease of operation with a single 1.8V power supply. Although this results in larger reference spurs in the output spectrum, they are comfortably within the requirements for the Zero-G system. The 4MHz and 8MHz spurs are –35dBc (–20dBc required), and the 24MHz spur is at –45dBc (–40dBc required).

Figure 29.10.6 summarizes the receiver performance. The whole receiver (not including the on-chip buffers) achieves a noise figure of 8.8dB. The P_{b1dB}, reference spurs, and phase noise for this receiver are sufficiently low to achieve a data rate 1Mb/s over 10m. The total power consumption of the receiver is 17mW, and the active chip area of the receiver is 0.66mm². Although an off-chip matching network was utilized for the test chip, it would not be required in the end design of the differential LNA. The parasitics of the package and the inductance of the antenna would be absorbed into the design.

References:

[1] M. Hamada, S. Verma, J. Xu, T.H. Lee, "Completely DC-Free Direct Sequence Spectrum Spreading Scheme for Low Power, Low Cost, Direct Conversion Transceiver," *WNCG Wireless Networking Symposium*, Oct., 2003.

[2] https://www.bluetooth.org/spec/.

[3] http://www.fcc.gov/.

[4] P. Andreani, H. Sjoland, "Noise Optimization of an Iinductively Degenerated CMOS Low Noise Amplifier," *IEEE TCAS II,* vol. 48, pp. 835-841, Sept., 2001.

[5] S. Verma, J. Xu, T.H. Lee, "A Multiply-by-3 Coupled-Ring Oscillator for Low-power Frequency Synthesis," *IEEE J. Solid-State Circuits*, vol. 39, pp. 709-713, Apr., 2004.

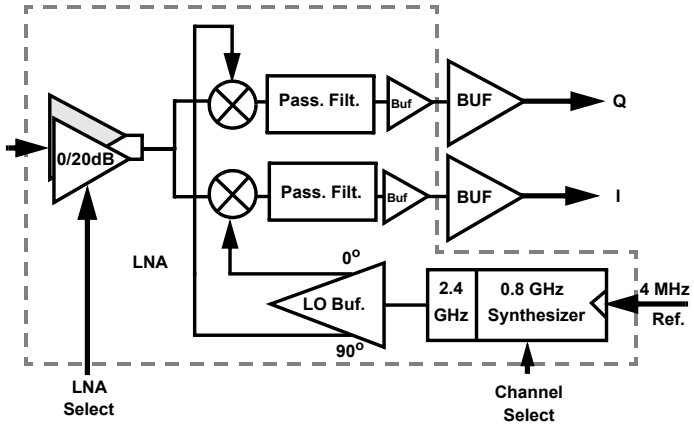

Figure 29.10.1: Receiver architecture.

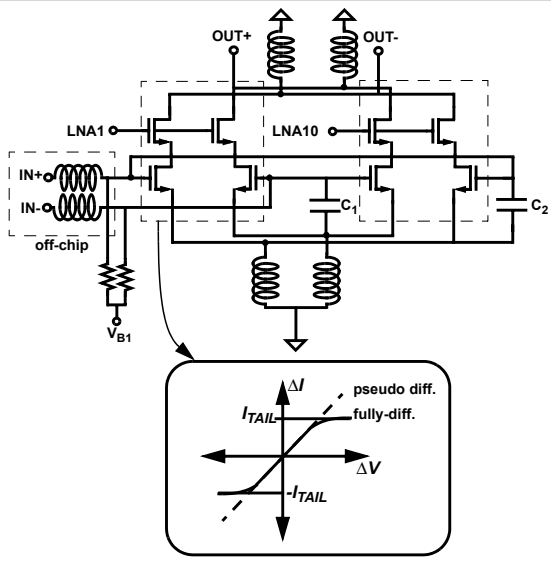

Figure 29.10.2: 0dB/20dB LNA design.

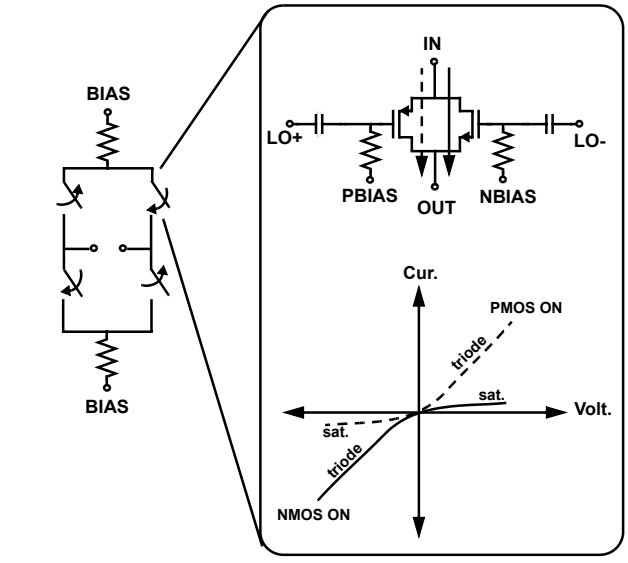

Figure 29.10.3: Transmission-gate mixer design.

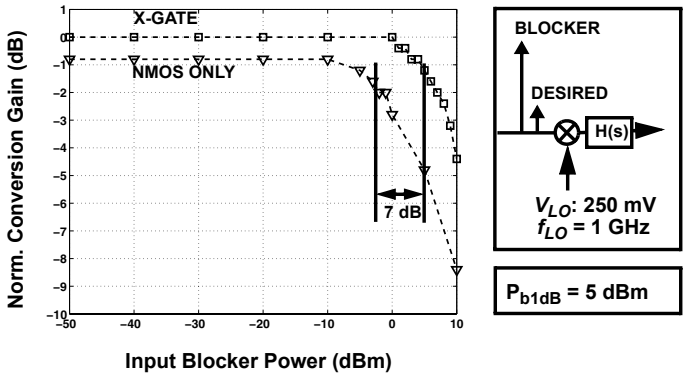

Figure 29.10.4: Measured blocker P_{b1dB} improvement for stand-alone passive chain.

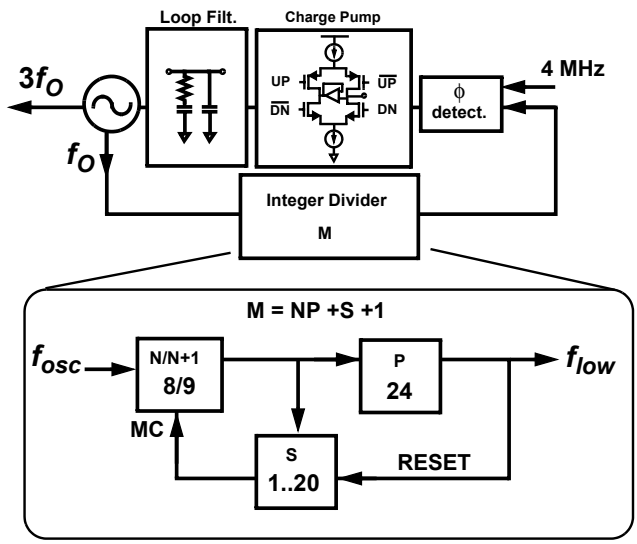

Figure 29.10.5: Integer-M frequency synthesizer with multiply-by-3 VCO.

Performance	Achieved	Required
Passband Noise Fig. (@1.9 GHz)	8.8 dB[a]	< 18 dB
1-dB Blocker Compress. Pt.	-15 dBm	-20 dBm (Q_{in} = 3)
LO Phase Noise @24 MHz	< -115 dBc/Hz	<-111 dBc/Hz
Ref. Spur @24 MHz	-45 dBc	< -40 dBc
Signal Path Current	3 mA	
Synth. Current @2.45 GHz	2.5 mA	
LO Buffer Current	4 mA	
Total Current	9.5 mA	
Supply Voltage	1.8 V	
Active Chip Area	0.66 mm^2	
Off-chip Components	Inductor (ant.), crystal	
Technology	0.25 μm CMOS	

a. VGA needed after passive chain - not included in design.

Figure 29.10.6: Receiver performance summary.

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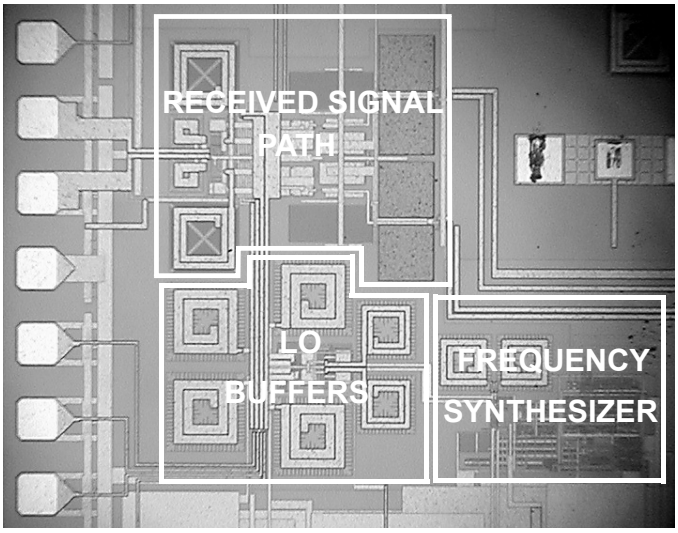

Figure 29.10.7: Receiver die micrograph.

