30.7 A 10GHz Broadband Amplifier with Bootstrapped 2kV ESD Protection

Wolfgang Soldner[1], Moon-Jung Kim[2], Martin Streibl[3], Harald Gossner[3], Thomas H. Lee[2], Doris Schmitt-Landsiedel[1]

[1]Technical University Munich, Munich, Germany
[2]Stanford University, Stanford, CA
[3]Infineon Technologies, Munich, Germany

ESD designers have to consider two shrinking design windows. On one hand, the oxide breakdown voltage of a thin-oxide transistor melted down from 12V in a 0.25µm technology to 4.5V at the 90nm node. On the other hand, the continuing demand for narrowband and broadband communication systems pushes the carrier frequencies (e.g. up to 10GHz for UWB). This reduces the tolerable capacitive load of the ESD elements. To guarantee a 2kV human body model (HBM) target, the state of the art ESD protection concepts require parasitic capacitances in the order of 100 to 150fF. This capacitive load leads to an extrapolated frequency limit of about 5GHz [1].

To bridge the gap from 5GHz to frequencies >10GHz, where the implementation of shunting coils makes ESD design easier [2], the parasitic ESD capacitance can be eliminated by several compensation techniques. For narrowband RF applications, cancellation or isolation can be used [3]. Broadband RF ESD protection concepts implementing a T-coil [4] or distributed protection elements have been proposed, but they suffer from large area consumption and delicate dimensioning. Alternatively bootstrapping can be applied to screen out parasitic capacitances [5]. Here, a mid node is created by arranging two ESD elements in series as exemplarily shown in Fig. 30.7.1. If an additional sense-amplifier circuit mirrors the RF signal from the RF pad to the mid node without a time shift Δt, no displacement current will flow over the ESD element connected to the pad. Thus, the parasitic ESD capacitance is compensated. For frequencies of ~10MHz as investigated in [5], a simple source follower could uphold the requirement $\Delta t \rightarrow 0$.

This work introduces a low-C ESD-protection element, referred to as dual-diode silicon-controlled rectifier (DD-SCR), with a parasitic capacitance of ~50fF, bypassing the need to cascode the ESD device for bootstrapping. The functional principle of the DD-SCR is shown in the left part of Fig. 30.7.2. It is based on a transient triggered silicon controlled rectifier (TT-SCR) as described in [1]. For a positive stress at pad 1 against V_{DD} (abbr. PAD(pos)V_{DD}), the ESD current flows along the dashed-dotted line over two forward-biased PN junctions. For a PAD(pos)V_{SS} stress, the main discharge current will flow along the dashed line. To guarantee this, the thyristor has to be turned on by an initial trigger current through the base of the first PNP transistor of the SCR. This trigger current will flow via the forward-biased D1 and the blocking capacitance C_b to ground (dotted line). The negative discharges make use of the SCR from pad1 to V_{DD} accordingly. Adding D1 to the thyristor has 2 benefits: first, the parasitic capacitance of the SCR, that is dominated by the first PN junction at the RF pad, is reduced; secondly, the required mid-node for the bootstrap concept is created without the need of cascoding the whole ESD device.

On the right side of Fig. 30.7.2, a bootstrapped version of a DD-SCR protection circuit is shown (for simplification the second thyristor is not shown). The first common-source stage of the bootstrap amplifier A1 decouples the RF signal with little additional capacitive load on the RF pad (see Fig. 30.7.3). The second stage is connected to the n-gate of the SCR and provides the major amplification. The capacitance C1 and C2 represents the RF relevant pn junctions of the DD-SCR while C3 describes the parasitic capacitance of the metallization.

For an optimum efficiency of the bootstrap concept, the amplifier has to guarantee an amplification A=1 and a time shift Δt=0. This can only be achieved by additional phase shifting elements. In this work, a parallel peaking coil L_{Boot} (760pH, 120×120µm²) is implemented to eliminate the intrinsic phase shift of the bootstrap amplifier at a center frequency of ~9GHz. The parasitics of the coil (R_{series}≈6Ω and C_{c1}≈C_{c2}≈36fF) are determined by 2.5D field simulations. For a low R_{series}, the windings are drawn in the 2 upper metal layers.

To investigate the impact of the low-C ESD protection in combination with the bootstrap amplifier on the performance of a typical RF input circuit, a 10GHz broadband amplifier was developed in a 90nm CMOS process. The employed transistors have a gate-oxide thickness of 1.5nm. As shown in Fig. 30.7.4, the amplifier consists of a first common-source transistor stage T1 (with a cascode transistor T2) and a second-stage (T3) connected via a series peaking coil, which is a copy of L_{Boot}, for bandwidth enhancement. To ensure a S_{11} <–10dB, an input matching network (R4, R5 and a matching coil) is added. The bias for T1 is provided externally by the vector network analyzer.

The unprotected amplifier has a measured gain of 10.7dB and a 3dB bandwidth of 13.2GHz (see Fig. 30.7.5). The input reflection is <-10dB up to 9.1 and 11.8GHz, before and after pad deembedding, respectively. The power consumption is 60mW at V_{DD}=1.2V. By adding the DD-SCR protection without bootstrapping, the S_{11} bandwidth is reduced by ~1.2GHz while gain and NF remain approximately constant.

Including the bootstrap circuit leads to an enhancement of the S_{11} bandwidth at the -10dB intersection of ~750MHz, therefore compensating almost 60% of the bandwidth degradation due to the ESD-protection circuit (Fig. 30.7.5). The measurement result is in good agreement with the simulated values. However, to explore the full capability of bootstrapping, the gate bias of the circuit had to be reduced from 750 (=bias#1) to 350mV (=bias#2) leading to a constant shift in S_{11} of the broadband amplifier. This measure is necessary due to a ohmic path in the DD-SCR from the bootstrapped mid-node to ground that was not considered in the design. To get the full effect of bootstrapping at the operational point of the amplifier, an isolation of the p-well of the DD-SCR, representing the mid-node, from the substrate is required. This can be achieved, for example, by a triple-well process. The power consumption of the bootstrap circuit itself is 19mW.

The ESD hardness of a fully protected version of the amplifier is shown in Fig. 30.7.6. The characterisation is done with a transmission-line pulser (TLP) setup with 10ns rise time and 100ns pulse length comparable to HBM specifications. For all important I/O stress combinations, the circuit could withstand 1.3A, which is equivalent to a level of 2kV HBM.

A broadband amplifier using a bootstrapped ESD-protection circuit achieved an ESD robustness of 2kV HBM while maintaining input matching up to 10GHz. The key parameter for this concept is the time shift of the bootstrap amplifier that is compensated with a coil in this paper. The use of low-C ESD protection elements in combination with a bootstrap circuit opens the possibility to equip multi-GHz high-speed interfaces like UWB or high-definition multimedia interface (HDMI) with significant ESD robustness. This is especially important for pins jeopardized by system-level discharges.

References:

[1] W. Soldner, M. Streibl, U. Hodel, et al., "RF ESD Protection Strategies: Codesign vs. Low-C Protection," *Proc. EOS/ESD Symp.*, pp. 33-42, Sept., 2005.
[2] S. Thijs, M. I. Natarajan, T. Daenen, et al., "ESD Protection for a 5.5 GHz LNA in 90nm RF CMOS - Implementation Concepts, Constraints and Solutions," *Proc. EOS/ESD Symp.*, pp. 40-49, Sept., 2004.
[3] S. Hyvonen, S. Joshi, E. Rosenbaum, "Comprehensive ESD Protection for RF Inputs," *Proc. EOS/ESD Symp.*, pp. 188-194, Sept., 2003.
[4] S. Galal and B. Razavi, "Broadband ESD Protection Circuits in CMOS Technology," *ISSCC Dig. Tech. Papers*, pp. 182-183, Feb., 2003
[5] I. Opris, "Bootstrapped Pad Protection Structure," *IEEE J. Solid-State Circuits*, vol. 33, pp. 300-301, Feb., 1998.

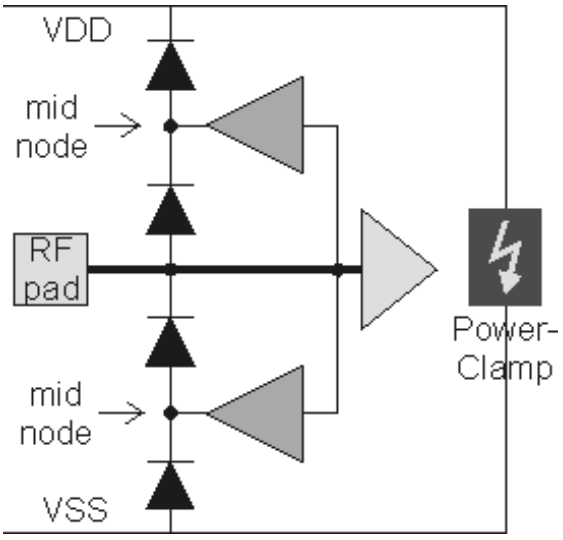

Figure 30.7.1: Conventional bootstrap concept.

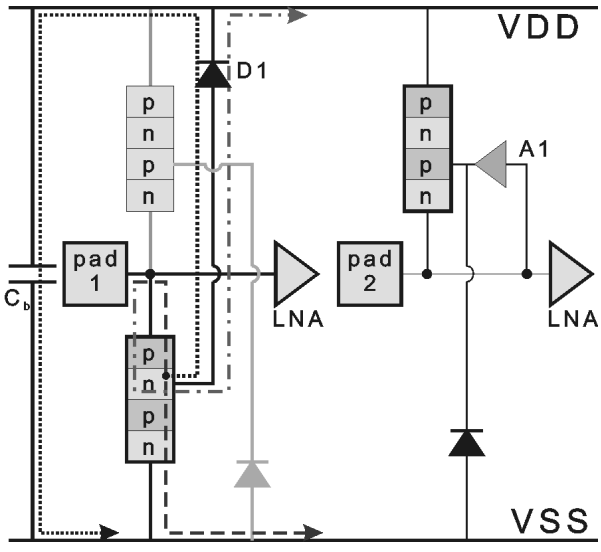

Figure 30.7.2: The DD-SCR concept (left). A bootstrapped DD-SCR (right).

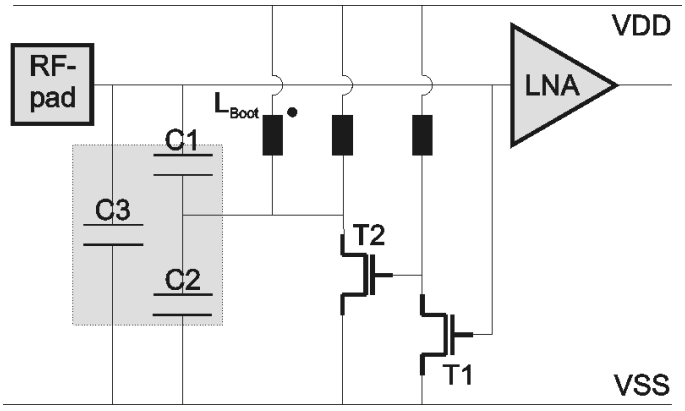

Figure 30.7.3: Implementation of a dual-stage bootstrap amplifier.

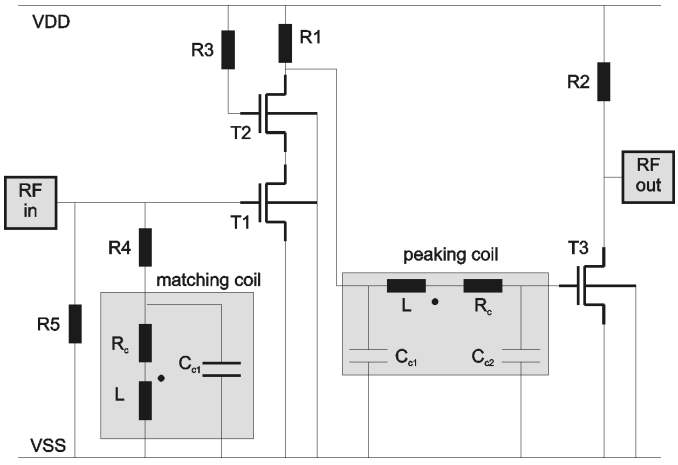

Figure 30.7.4: Schematic of the 10GHz amplifier.

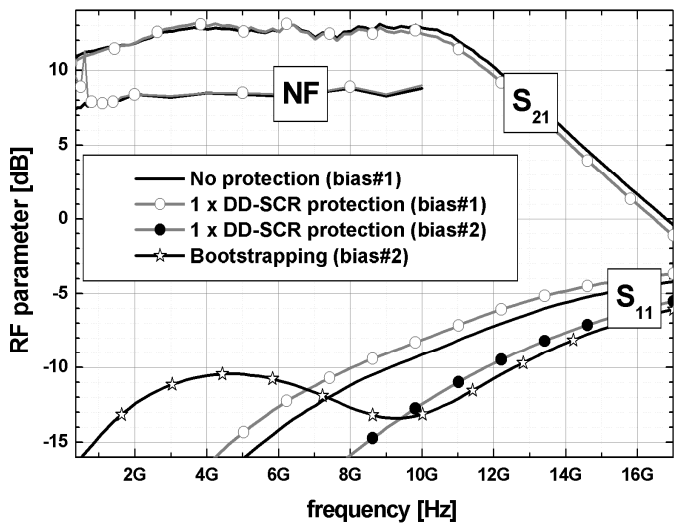

Figure 30.7.5: Measured RF parameters.

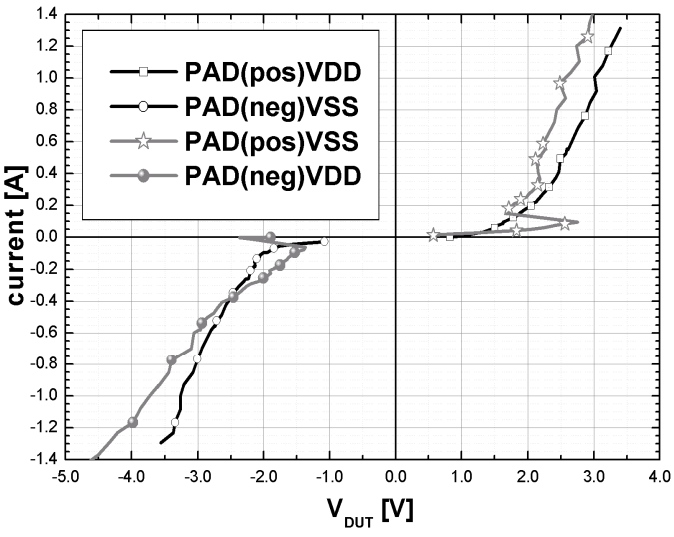

Figure 30.7.6: High-current TLP characteristics.