Automatic Phase Alignment for a Fully Integrated Cartesian Feedback Power Amplifier System

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***Abstract*—A phase-alignment system is used in the first reported IC to fully integrate a power amplifier, Cartesian feedback linearization circuitry, and a phase-alignment system. The phase-alignment system consumes 8.8 mW from a 2.5-V supply and employs a new technique for offset-free analog multiplication that enables it to function without manual trimming. Phase alignment of better than 9° is maintained for drifts as large as ±90°. We demonstrate how the phase-alignment system improves the stability margins of the fully integrated Cartesian feedback system. The power amplifier itself, integrated on the same die, operates at 2 GHz and delivers a maximum of 14.2 dBm of output power into a 50-Ω load. The IC was fabricated in a 0.25-μm CMOS process.**

***Index Terms*—Analog multipliers, Cartesian feedback, chopper stabilization, phase alignment, power amplifiers (PAs).**

I. Introduction

DESIGNERS of RF power amplifiers (PAs) for modern wireless systems are faced with a difficult tradeoff. On one hand, the PA consumes the lion's share of the power budget in most transceivers. It follows that, in a cellular phone, for example, battery lifetime is largely determined by the power efficiency of the PA. On the other hand, it may be desirable to have high *spectral* efficiency—the ability to transmit data at the highest possible rate for a given channel bandwidth. The design conflict is that, while spectral efficiency demands a highly linear PA, power efficiency is maximized when a PA is run as a constant-envelope, nonlinear element. The current state of the art is to design a moderately linear PA and employ some linearization technique. The amplifier operates as close to saturation as possible, maximizing its power efficiency, and the linearization system maximizes the spectral efficiency in this near-saturated region.

There are many different linearization techniques. Among these, Cartesian feedback is an attractive option for at least two reasons: 1) because it employs analog feedback, the requirement for a detailed nonlinear model of the PA is greatly relaxed and 2) it automatically and elegantly compensates for process variations, temperature fluctuations, and aging. Nevertheless, historically the technique has suffered the practical shortcoming of relying on synchronous downconversion, which has been difficult to realize without manual trimming. This problem, combined with the recent trend toward fully monolithic systems, has caused Cartesian feedback to languish for years as little more than an academic curiosity.

We have solved the synchronous downconversion problem with a new, nonlinear, analog phase alignment regulator [5], [6]. What this enables, for the first time, is a fully integrated Cartesian feedback system that functions with an absolute minimum of trimming. In this paper, we describe in detail the phase-alignment system of the prototype IC and present the results of its testing. The complete linearization system will be described in a separate article.

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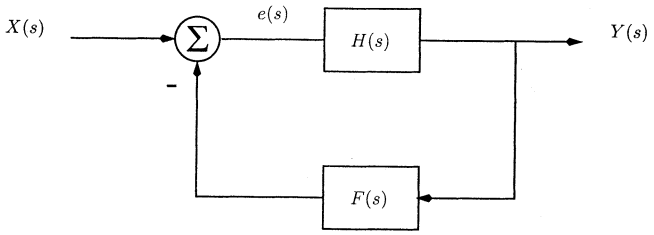

Fig. 1. Simple feedback system.

II. Terminology Convention

In this section, we identify the terminology conventions that will be used in discussing feedback systems in this paper. Fig. 1 shows an example feedback system. The signal $e(s)$ is the error or difference between the command input $X(s)$ and the feedback signal. The output of this system $Y(s)$ is related to the command input through the well-known relation

$$\frac{Y(s)}{X(s)} = \frac{H(s)}{1 + H(s)F(s)}.$$

The quantity $H(s)F(s)$ will be referred to as the loop gain, or loop transmission, of the system and will be given the symbol $L(s)$.

III. Consequences of Phase Misalignment in Cartesian Feedback Systems

Fig. 2 shows a typical Cartesian feedback system [13]. The system block $H(s)$ represents the loop driver amplifiers, which provide the loop gain as well as the dynamics introduced by the compensation strategy. The loop drivers feed the baseband inputs of the upconversion mixers, which in turn drive the PA. Some means of coupling the output of the PA to the downconversion mixers is employed, and the output of these mixers is used to close the feedback system.

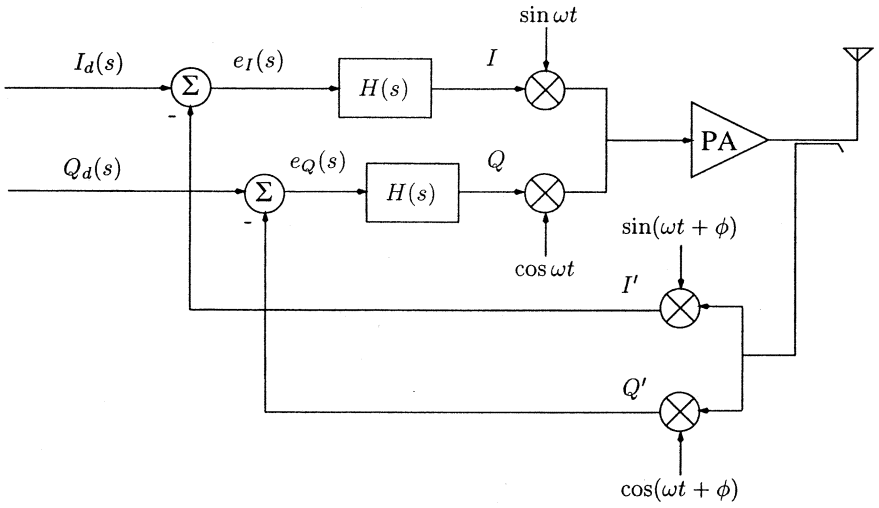

Fig. 2. Typical Cartesian feedback system.

Ideally, a Cartesian feedback system functions as two identical, decoupled feedback loops: one for the I component and one for the Q component. This corresponds to the case of $\phi = 0$ in Fig. 2. In practice, however, this state of affairs must be actively enforced. Delay through the PA, phase shifts of the RF carrier due to the reactive load of the antenna, and mismatched interconnect lengths between the local oscillator (LO) source and the two mixers all manifest as an effective nonzero ϕ. Worse, the exact value of ϕ varies with temperature, process variations, output power, and carrier frequency. A Cartesian feedback system in which ϕ is nonzero is said to have phase misalignment. In this state, the two feedback loops are coupled, and the stability of the system is compromised.

The impact of phase misalignment on system stability can be seen mathematically. We start by observing that the demodulated symbol S' is rotated relative to S by an amount equal to the phase misalignment ϕ. To see this, we write Cartesian components of the demodulated symbol

$$I' = (I\sin\omega t + Q\cos\omega t)\sin(\omega t+\phi)$$
$$Q' = (I\sin\omega t + Q\cos\omega t)\cos(\omega t+\phi)$$

where ω is the carrier frequency. Using trigonometric identities and assuming frequency components at 2ω are filtered out, we arrive at S' as

$$I' = \frac{1}{2}(I\cos\phi + Q\sin\phi) \tag{1}$$
$$Q' = \frac{1}{2}(-I\sin\phi + Q\cos\phi). \tag{2}$$

We see that, for $\phi \neq 0$, an excitation on the I input of the modulator results in a signal on the Q' downconverter output (and similarly for Q and I'). By definition, the two loops are coupled.[1]

[1]Technically, $\phi = \pi$ is also an uncoupled case. However, there is now an inversion in both loops, resulting in positive feedback instead of the desired negative feedback.

One method of stability analysis is to consider the error signals $e_I(s)$ and $e_Q(s)$ shown in Fig. 2. Recall that for the single feedback loop of Fig. 1 the error signal is written

$$e(s) = \frac{X(s)}{1+L(s)}.$$

For frequencies of interest, the hope is that $|L(s)|$ is very large. In the present case, let the phase misalignment be ϕ. Furthermore, we set $Q_d = 0$ without loss of generality.[2] The error expressions, as a function of the single input $I_d(s)$, are written

$$e_I(s) = I_d(s) - L(s)e_I(s)\cos\phi - L(s)e_Q(s)\sin\phi$$
$$e_Q(s) = L(s)e_I(s)\sin\phi - e_Q(s)L(s)\cos\phi$$

where $L(s)$ includes the dynamics of the loop compensation scheme $H(s)$ and the (linearized) dynamics introduced by the modulator, PA, and demodulator. From here, it is straightforward to show that

$$e_I(s) = \frac{X(s)}{1+L(s)\cos\phi + \frac{[L(s)\sin\phi]^2}{1+L(s)\cos\phi}}.$$

This reduction of the system to a single-input problem now yields considerable insight. We identify an effective loop transmission $L_{\text{eff}}(s,\phi)$ as follows:

$$L_{\text{eff}}(s,\phi) = L(s)\cos\phi + \frac{[L(s)\sin\phi]^2}{1+L(s)\cos\phi}. \tag{3}$$

For perfect alignment, $\phi = 0$ and L_{eff} is simply $L(s)$. The worst alignment is $\phi = \pi/2$, for which $L_{\text{eff}} = [L(s)]^2$: the loop dynamics are a cascade of the dynamics in the uncoupled case. Unless designed with this possibility in mind, most choices of $H(s)$ yield unstable behavior in this second case. Equation (3) shows that traditional measures of stability degrade continuously as ϕ sweeps from 0 to $\pi/2$, a fact demonstrated experimentally by Briffa and Faulkner [4].

[2]We do not lose generality as long as we stay with linear analysis.

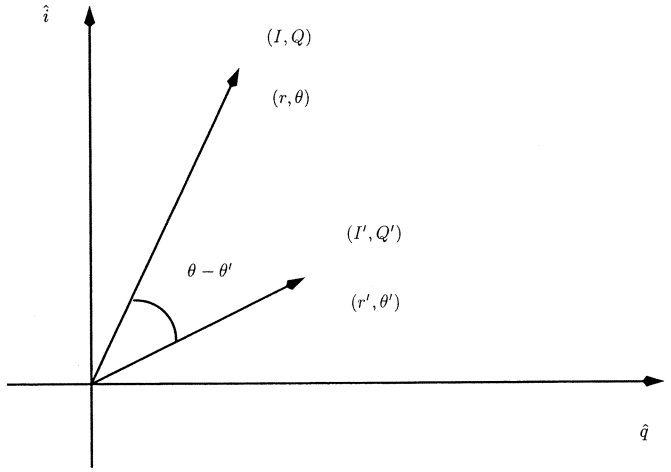

Fig. 3. Rotation of the baseband symbol due to phase misalignment.

IV. Analog Nonlinear Regulator Concept for Maintaining Phase Alignment

Occasionally, true regulation of the phase alignment is not needed, and it suffices to introduce a manually adjustable delay between the LO source and, say, the demodulator [10]. This approach is only feasible, however, if the system is not subject to variations in temperature, carrier frequency, process parameters, or, in some cases, output power. For cases in which the alignment must be regulated, various methods have been proposed in the literature [2], [3], [7], [12].

We present our control concept as a compact, truly continuous solution to the problem of LO phase alignment. It is truly continuous because it does not, for example, rely on the appearance of a specific symbol or pattern in the outgoing data stream. It is compact because it is easily implemented without digital signal processing, as presented here. This is a particularly compelling advantage, as the signals in a Cartesian feedback system are necessarily in analog form. Also, we emphasize that, because the concept is based on the processing of baseband symbols, its realization is independent of carrier frequency.

A. Nonlinear Dynamical System

Fig. 3 represents a baseband symbol at the inputs of the modulator and at the outputs of the demodulator of a Cartesian feedback system. Mathematically the vectors are described in both Cartesian and polar coordinates, with primed coordinates denoting the demodulated PA output and unprimed coordinates denoting the modulator input. In addition to undergoing a distortion in magnitude, the demodulated symbol is rotated by an amount exactly equal to the phase misalignment [see (1) and (2)].

A start to the design of a phase-alignment regulator is to observe that the signals I, Q, I', and Q', taken together, represent enough information to determine the phase misalignment. Further, they are easily accessible within the system. We seek to combine these variables such that, over a suitable range, the derived signal is monotonic in the phase misalignment.

One such combining of the variables is the sum of products $IQ' - QI'$. Recognizing that $I = r\sin\theta$ and $Q = r\cos\theta$ and using trigonometric identities, we write the key relation

$$IQ' - QI' = rr'\sin(\theta - \theta'). \tag{4}$$

We see that, using two multipliers and a subtractor—operations easily realizable in circuit form—one can derive a control signal that is indeed monotonic in the phase misalignment over the range $-(\pi/2) < \theta - \theta' < \pi/2$.

Fig. 4 details a nonlinear dynamical controller built around (4). Using the notation $\Delta\theta = \theta - \theta'$, an implementation can be understood as mechanizing the equation

$$\frac{d\theta}{dt} = -\kappa[r(t)]^2 G\sin(\Delta\theta) \tag{5}$$

where κ is a constant of proportionality and gain G is associated with the integrator.

Equation (5) presupposes the ability to correct the phase shift by changing θ. The original prototype described in [5] realizes the required rotation by directly phase shifting the modulator LO. However, substantial power savings result from doing symbol rotation at baseband, as shown in Fig. 4. Regardless, rotation should be performed in the forward path of the Cartesian feedback system, where the unavoidable artifacts of imperfect rotation are suppressed.

B. Stability Concerns

Our control solution for the phase-alignment problem is the simplest of nonlinear dynamical systems. It is seen from (5) to have two equilibrium points: the first, for which the symbols are aligned, is *stable*; the second, for which the symbols are misaligned by π radians, is unstable. For the ideal system represented by (5), this is the extent of a rigorous stability analysis.

The real-world situation can be complicated by dynamics associated with the phase shifter (and, possibly, the subtractor). If we provisionally consider a modulation scheme in which the magnitude of transmitted symbols is held constant,[3] $r(t)$ in (5) loses its time dependence. Linearizing for small phase misalignments, and including the dynamics of the phase shifter as $P(s)$, we can represent the system as shown in Fig. 5. Drawing the system this way requires some manipulation. The output of the phase shifter is not really θ, but rather an additive *part* of θ that gets combined with the polar angle of the symbol being transmitted. However, in the absence of phase distortion and drift, the symbol-by-symbol changes of the polar angle θ are tracked by identical changes in θ'. These symbol-rate changes are thus invisible to an alignment system, and it is appropriate to label the output of $P(s)$ as θ. We can then include the effects of phase distortion and phase alignment drift as the additive disturbances of Fig. 5.

One can ensure stability by choosing G such that, for the largest symbol magnitude, loop crossover occurs before nondominant poles become an issue. Fortunately, the drift disturbance will normally occur on time scales associated with tem-

[3]Unlikely when using Cartesian feedback, of course. Temporarily making this assumption, however, yields insight that is broadly relevant to the stability analysis.

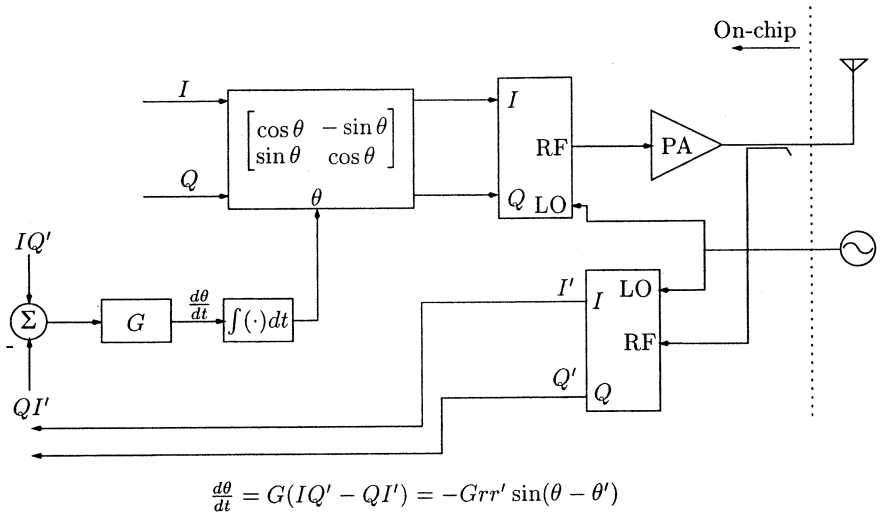

Fig. 4. Phase-alignment concept.

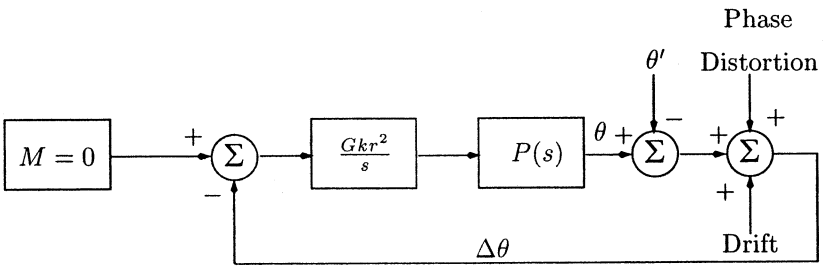

Fig. 5. Linearized phase regulation system. M is the desired misalignment, which is nominally zero.

perature drift and aging [13]. Suppression of the phase distortion is the domain of the Cartesian feedback itself. It follows that for many systems, little of the design effort need be focused on fast phase alignment.

C. Quadrature Error in the Mixers

The analysis of the phase-alignment control problem becomes complicated when one considers quadrature error in the mixers. It can be shown that, with this nonideality, no single setting of the phase shifter perfectly decouples the I and Q loops. This analytical result is independent of the phase-alignment method used. Fortunately, mixers with small quadrature errors ($\pm 5^\circ$) are easily realized. Such mixers cause no serious problems in our experiments.

V. New Technique for Offset-Free Analog Multiplication

The achieved accuracy of phase alignment is limited by errors in computing the sum of products $IQ' - QI'$ [5]. A major source of these errors is offsets in the analog multipliers. Our basic multiplier cell is shown in Fig. 6 [8]. A mathematically complete description of a multiplier's offset behavior requires at least three quantities: δ_I and δ_Q, the offsets attributable to the inputs, and δ_O, the offset introduced in the current-to-voltage conversion performed at the output of the multiplier. Minimizing these offsets is difficult: one might imagine, for example, some combination of careful, symmetrical layout and a calibration step. We introduce instead the technique shown in Fig. 6. The underlying idea is to employ chopper stabilization to eliminate (or at least greatly suppress) these multiplier offsets which produce the dominant phase alignment errors in conventional realizations. Long successfully used in precision dc amplifiers [1], [9], [14], two critical modifications are required to apply chopper stabilization to analog multiplication. The first modification is to chop the two inputs in quadrature. The second is to chop down at *twice* the original chopping frequency. To the extent that this chopping strategy is perfectly implemented, offsets δ_I, δ_Q, and δ_O are completely circumvented.

The chopping operation is equivalent to mixing a signal with a square wave of unit amplitude.[4] In the following treatment, one chopping waveform will be denoted $c_0(t)$, and the other quadrature waveform will be denoted $c_{90}(t)$. We write these two waveforms as their Fourier series decompositions

$$c_0(t) = \sum_{n=0}^{\infty} \frac{4}{(2n+1)\pi} \sin(2n+1)\omega_0 t$$

$$c_{90}(t) = \sum_{m=0}^{\infty} \frac{4}{(2m+1)\pi} (-1)^m \cos(2m+1)\omega_0 t$$

where ω_0 is the angular chopping frequency $2\pi f_0$.

[4]That is to say, a square wave that alternates between $+1$ and -1. We clarify because sometimes, particularly in single-ended systems, it is convenient to chop with a square wave that alternates between $+1$ and 0. This latter case requires a mathematical treatment that differs slightly from what we present here.

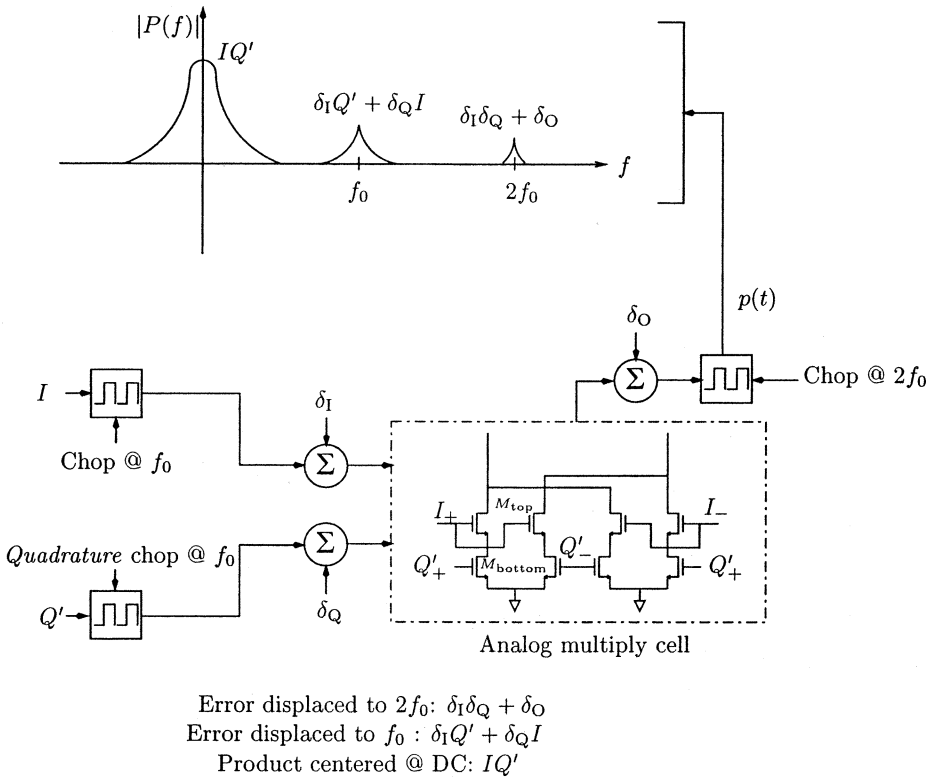

Fig. 6. New technique for offset-free analog multiplication.

Fig. 6 shows the signals applied to the inputs of the analog multiplier as

$$Ic_0(t) + \delta_I$$

and

$$Q'c_{90}(t) + \delta_Q.$$

Assuming linear multiplication, the output of the multiplier (before the down chopping operation) is written as

$$IQ'c_0(t)c_{90}(t) + \delta_I Q'c_{90}(t) + \delta_Q Ic_0(t) + \delta_I\delta_Q + \delta_O. \quad (6)$$

The second and third terms of this expression can only have spectral content centered at ω_0 and/or its odd harmonics, while the fourth and fifth terms are centered at dc. The key, then, is to demonstrate that the product $c_0(t)c_{90}(t)$ has spectral content only at even harmonics of the fundamental. A graphical analysis, as shown in Fig. 7, is by far the easiest way to accomplish this. The product $c_0(t)c_{90}(t)$ is seen to be

$$\begin{aligned} c_0(t)c_{90}(t) &= c_{2\omega_0}(t) \\ &= \sum_{n=0}^{\infty} \frac{4}{(2n+1)\pi} \sin{(2n+1)(2\omega_0)t} \end{aligned}$$

which has spectral components only at even harmonics: $2\omega_0, 6\omega_0, 10\omega_0, \ldots$. Equation (6) now becomes

$$IQ'c_{2\omega_0}(t) + \delta_I Q'c_{90}(t) + \delta_Q Ic_0(t) + \delta_I\delta_Q + \delta_O \quad (7)$$

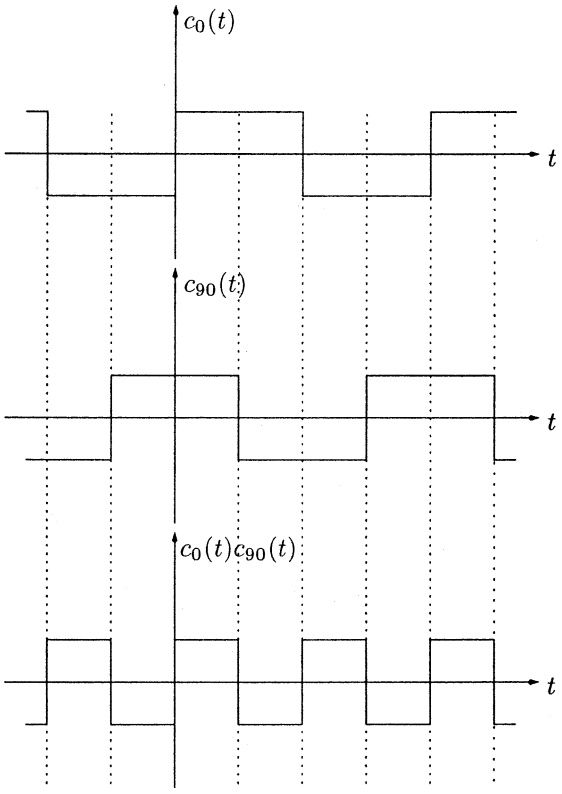

Fig. 7. Graphically computing $c_0(t)c_{90}(t)$.

and we have achieved the goal of separating, in the frequency domain, the desired product from the artifacts of dc offsets.

The last steps are to do a down-chopping operation and then to filter. For the down-chopping waveform, $c_{2\omega_0}(t)$ is the proper

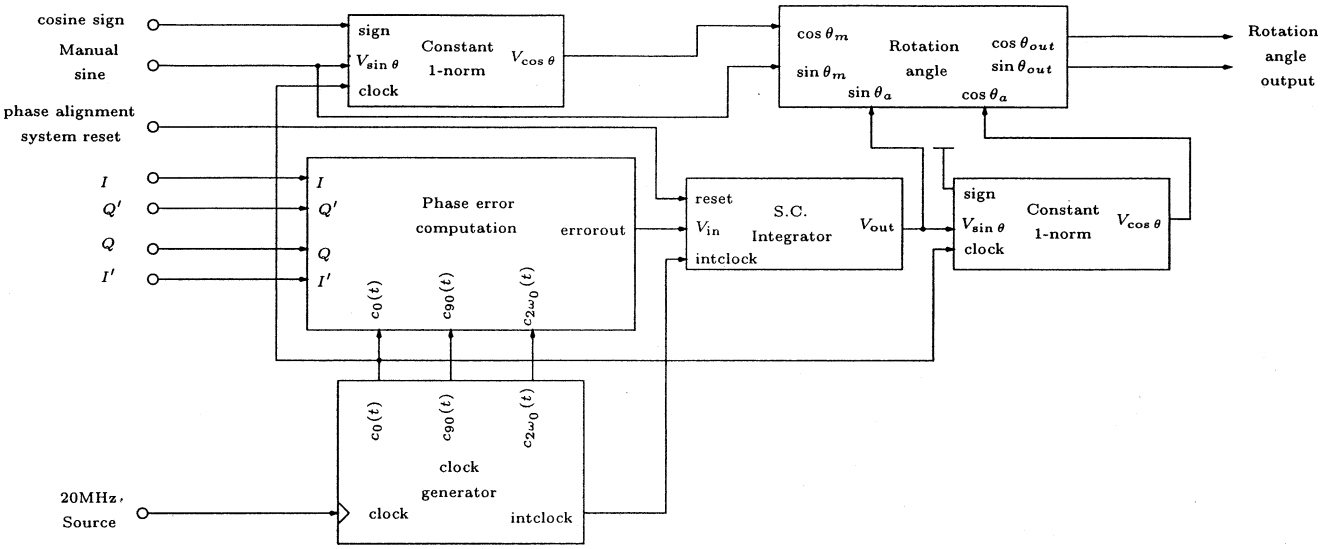

Fig. 8. Overview diagram of the phase-alignment system.

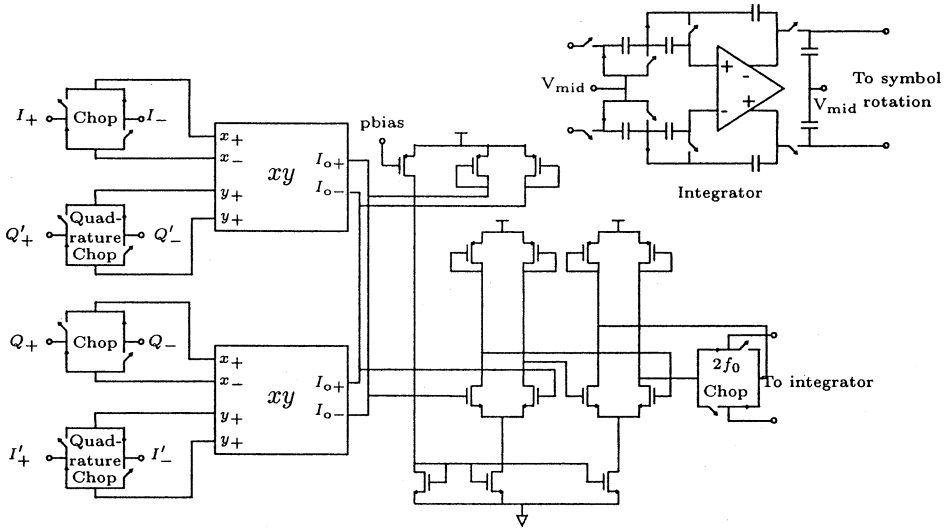

Fig. 9. Phase error computation and offset-cancelling switched-capacitor integrator.

choice. To analyze the effect of multiplying (7) by $c_{2\omega_0}(t)$, it is helpful to make use of the equalities

$$\begin{aligned} c_0(t)c_{2\omega_0}(t) &= c_{90}(t) \\ c_{90}(t)c_{2\omega_0}(t) &= c_0(t) \\ c_{2\omega_0}(t)c_{2\omega_0}(t) &= 1 \end{aligned}$$

which are readily verifiable by the kind of graphical analysis depicted in Fig. 7. Multiplying (7) by $c_{2\omega_0}$, we obtain

$$IQ' + \delta_I Q' c_0(t) + \delta_Q I c_{90}(t) + (\delta_I \delta_Q + \delta_O) c_{2\omega_0}(t). \quad (8)$$

Passing through a low-pass filter at last yields the desired product IQ'.

VI. Fully Integrated Prototype

To test the phase-alignment and chopper stabilization concepts, a prototype was implemented in National Semiconductor's 0.25-μm CMOS process. A system overview is given in Fig. 8.

A. Computing the Phase Error and Integrating

In Fig. 9, we show how the phase error calculation and integration are carried out on the fabricated IC. The chopping frequency f_0 is 2.5 MHz, down-chopping occurs at 5 MHz, and all clocks are derived from a 20-MHz off-chip crystal oscillator. As can be seen in the diagram, a switched-capacitor integrator provides the integration, and two factors motivate this choice over continuous-time methods. The first factor is that the offset removal of Fig. 6 is wasted if the integrator that follows has a large input-referred offset. Accordingly, an autozeroing switched-capacitor (SC) integrator [11] is used.[5] The second factor is that high speed in the phase-alignment system is unnecessary, as the proper phase setting typically evolves on time scales no shorter than those of temperature change, aging, and process variation.

[5]The offset of the SC integrator is further mitigated by the two preceding gain stages shown in Fig. 9.

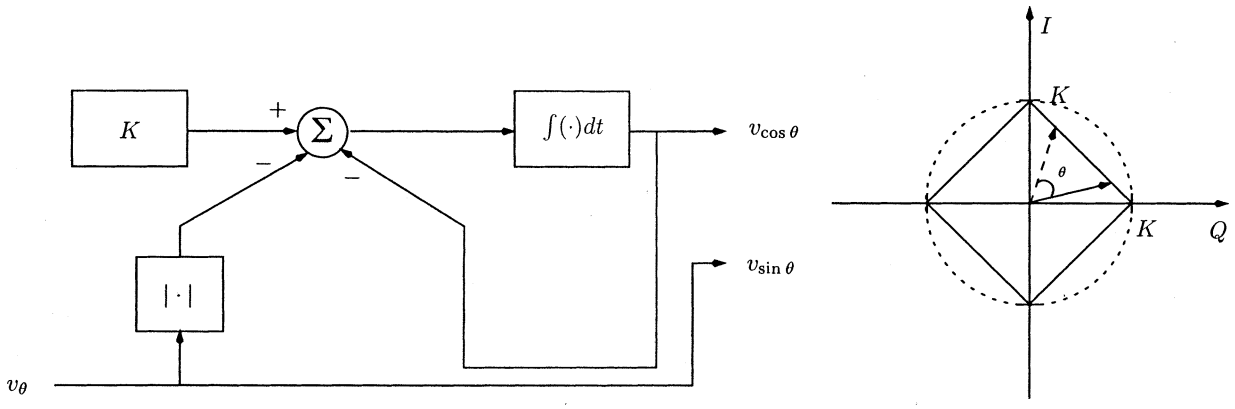

Fig. 10. Analog rotation using the 1-norm. The symbol is rotated along the contour of a square instead of a circle.

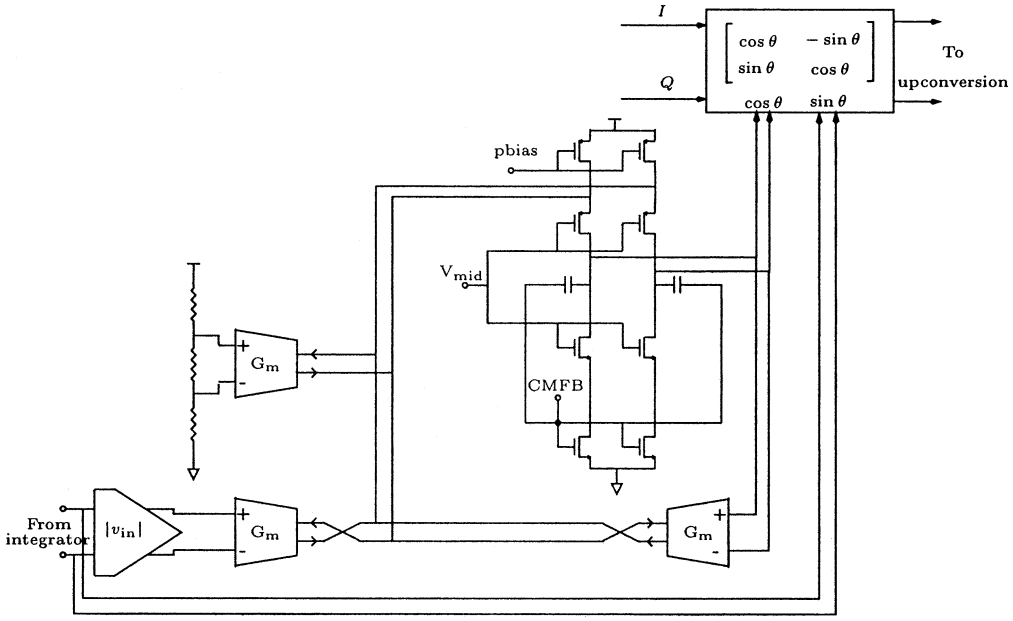

Fig. 11. Implementation of symbol rotation. Four analog multiply cells form the core of the matrix rotation block.

A slow integrator is thus appropriate and easily realized with a slowly clocked SC integrator. Its fully differential op-amp draws 524 μA and has a simulated dc gain of 115 dB. The unwanted chopping artifacts centered at 2.5 and 5 MHz are not filtered out. Instead, the integrator is clocked at 39.2 kHz, which has the property of aliasing tones at 2.5 and 5 MHz to $\pi/4$ and $\pi/2$, respectively, in the z domain.[6] As a result, aliasing of these artifacts does not result in dc errors. Chopping clocks transition on the rising edge of the 20-MHz source, while the integrator clock transitions on the falling edge. This ensures that edges of the chopping clocks do not occur at a sampling instant.

In order to test the system, it is convenient to implement the SC integrator with two modes of operation. The first mode is simply normal integration. For the second mode, the inverted output of the integrator is connected to the input, with the result that the output is driven to zero. Use of this reset mode enabled numerous experiments during the testing of the IC.

[6]Any frequency determined by $4f_0/n$, where n is an odd integer, will have this property. For this chip, n is 255.

B. Analog Symbol Rotation

For testing purposes, it is necessary to allow some way of intentionally introducing phase misalignment. Fig. 8 shows that the output of the phase-alignment system, the signal pair $(\sin\theta_a, \cos\theta_a)$ is fed to the "Rotation angle" block, which also takes as inputs the manually generated signal pair $(\sin\theta_m, \cos\theta_m)$. The output of the "Rotation angle" block is the composite signal pair $(\sin(\theta_a+\theta_m), \cos(\theta_a+\theta_m))$, which is computed using four analog multipliers. This output is then used to rotate the baseband symbol (again using analog multipliers to realize the matrix rotation) before upconversion. We are thus able to manually introduce misalignments over a 180° range and thereby confirm the regulatory behavior of the phase alignment system.

The chosen means of realizing the $(\sin\theta, \cos\theta)$ pairs is depicted in Fig. 10. The $\sin\theta$ input to the rotator block is taken directly from the integrator, while the $\cos\theta$ input is computed by an analog feedback loop. This loop acts to preserve the 1-norm of the $(v_{\sin\theta}, v_{\cos\theta})$ pair: $|v_{\sin\theta}|+|v_{\cos\theta}| = K$, where K is a reference voltage. The result is that the symbol is rotated along the contour of a square, as shown in Fig. 10,

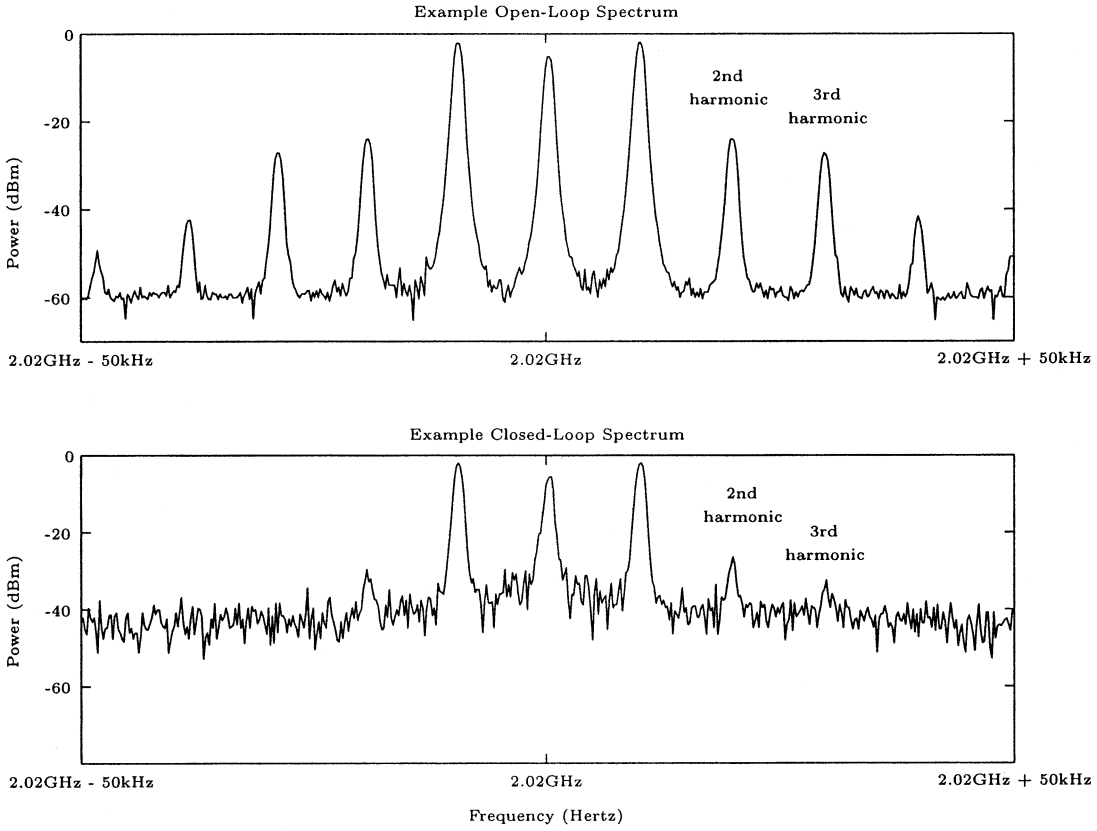

Fig. 12. Frequency-domain example of linearization behavior.

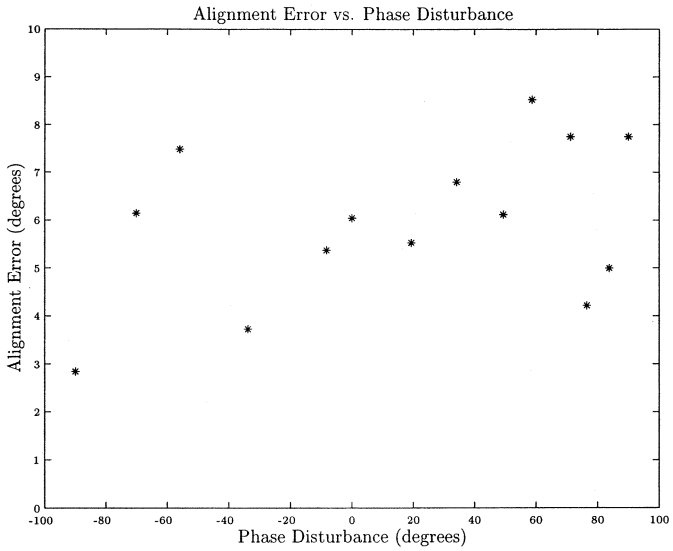

Fig. 13. Phase-alignment performance.

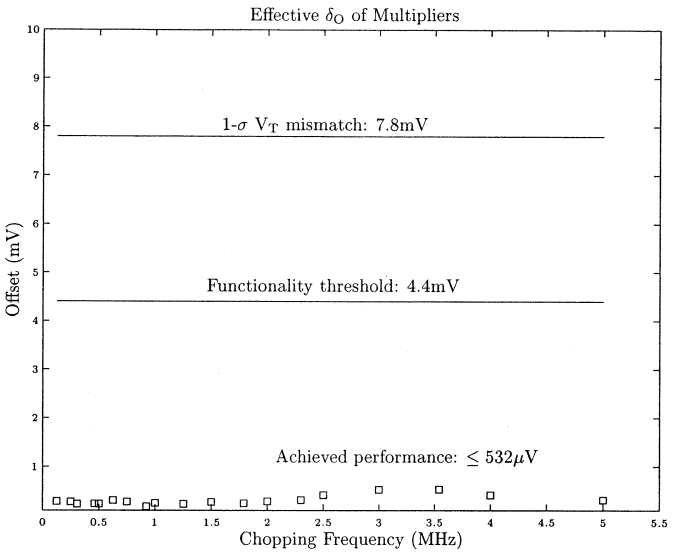

Fig. 14. Effective output offset δ_O of the chopper-stabilized multipliers of Fig. 9.

instead of a circle. This is a departure from [5], where in order to achieve pure rotation without affecting the magnitude the 2-norm $|v_{\sin\theta}|^2 + |v_{\cos\theta}|^2 = K$ was used. Use of the 1-norm is a purely simplifying decision which removes analog squarers from the system. Fortunately, the resultant warping of the symbol magnitude is rejected by the Cartesian feedback loop. For $|v_{\sin\theta}| \leq K$, the control loop of Fig. 10 enables rotations over a range of $\pm 90^\circ$.

The circuit implementation of Fig. 10 is shown in Fig. 11. The resistive voltage divider provides the voltage reference K. The capacitors serve a dual purpose. For differential signals, they set the value of the low-frequency pole to approximate the integrator of Fig. 10. For common-mode signals, they serve as the Miller compensation capacitor for the common-mode feedback loop (not shown). This circuit accounts for 3.1 mW of the overall power dissipation.

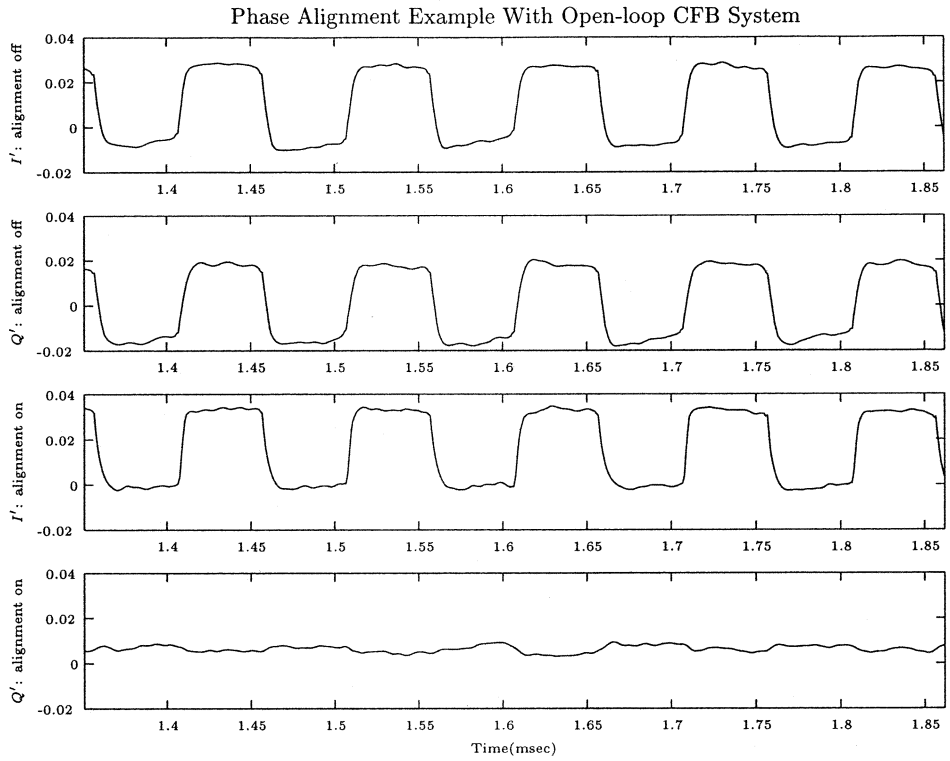

Fig. 15. Trace capture of a phase-alignment experiment. The Cartesian feedback loop is open.

VII. Prototype Results

In Fig. 12, we show a comparison of the open- and closed-loop spectra of the complete Cartesian feedback system. The top spectrum is the result of opening the CFB loop and driving a 1-kHz sine wave directly into the I channel of the upconversion mixer. The bottom spectrum shows the RF output during closed-loop operation with the phase-alignment system active. These spectra show that the Cartesian feedback system, aided by the alignment circuitry, effects a third-order harmonic reduction of 6 dB.

The reader will note that the noise floor in the closed-loop system is raised by approximately 20 dB in relation to that of the open-loop system. Furthermore, there is a peak centered at the carrier and a second harmonic centered 2 kHz away from the carrier. These are artifacts of a deficiency in the downconversion mixers, and will be discussed with the details of the full linearization system in a separate article.

Fig. 13 summarizes the phase regulation of the prototype IC. The test signal is a 500-mV-amplitude 10-kHz square wave on I, and Q is grounded. It is seen that the phase error never exceeds 9° over the full range of disturbances, which is more than adequate to keep the Cartesian feedback loop stable. Fig. 14 shows the offset of the phase-error computation circuit in Fig. 9 referred to the input of the the first gain stage. This offset for a chopping frequency of 2.5 MHz is 459 μV, and here the effectiveness of the chopping strategy is evident: the differential pair of the first gain stage alone has a $1-\sigma$ V_T mismatch of 7.8 mV. By way of comparison, complete failure of the phase-alignment system corresponds to an offset of 4.4 mV.

Fig. 15 is a trace capture of the type of experiment that yielded the data of Figs. 13 and 14. The Cartesian feedback loop is open, a 500-mV-amplitude 10-kHz square wave drives the I channel, and the Q channel is grounded.[7] The top two traces show that, initially, the misalignment has been manually set to 45°. The bottom two traces show the result of turning on the phase-alignment system (releasing it from the reset mode described in Section VI-A). Confirming its operation, we see a square wave on the I' channel only, while the Q' channel rests close to ground.[8]

Fig. 16 serves to illustrate the impact of phase misalignment on the stability margins of the closed-loop CFB system. Dominant pole compensation is used in the CFB loop, and for the upper two traces the misalignment is manually set to 74°. Overshoot and ringing is evident on these waveforms, and further misalignment causes outright oscillation. For the bottom two traces, the phase-alignment system is turned on, and one sees the classic first-order step responses that are expected when using dominant-pole compensation.

A die photo of the prototype chip is shown in Fig. 17, which was fabricated in National Semiconductor's 0.25-μm CMOS process. The maximum output power of the PA is 14.2 dBm at 2 GHz, and the complete Cartesian feedback linearization system draws 7.5 mA from a 2.5-V supply. Of that 7.5 mA, 3.5 mA is consumed by the phase-alignment regulator. All signal paths are fully differential.

[7]The voltage droop on what is normally the flat part of the square waves is due to the fact that, at the board-level, the modulator inputs have been ac coupled. There are no such ac-coupling capacitors between the loop drivers and the modulators.

[8]The dc offsets observable on I' and Q' are due in part to the board-level differential-to-single-ended converters, which are necessary in order to display the differential signals of the IC on an oscilloscope. We employ an active solution, as opposed to a balun, in order to permit testing of the system using low-frequency signals.

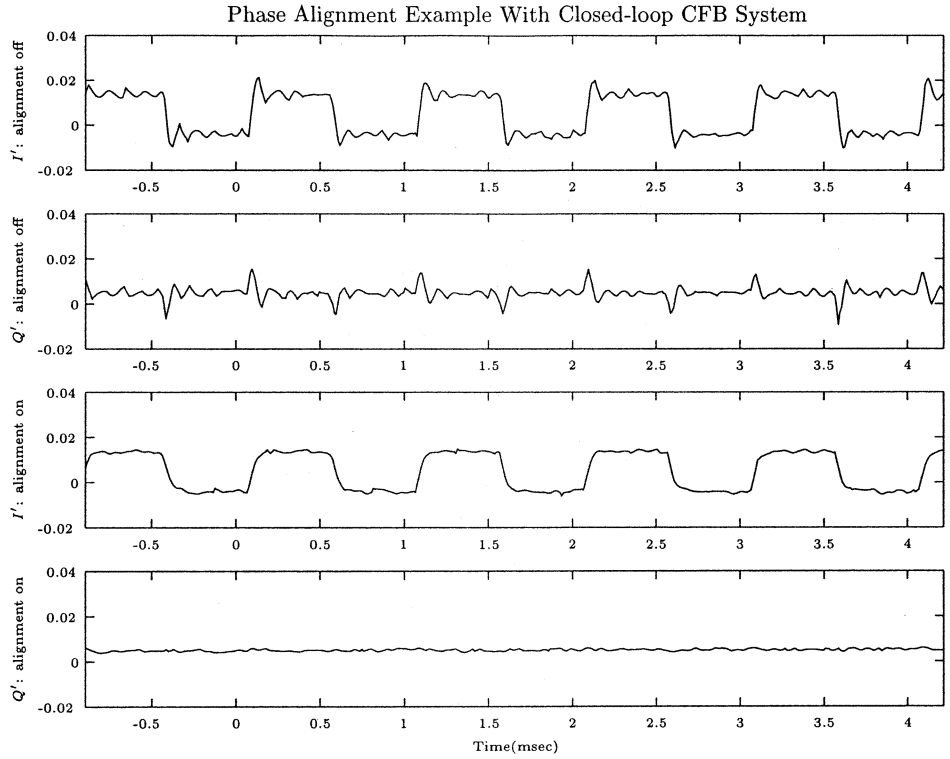

Fig. 16. Illustration of phase-alignment stabilizing the closed-loop CFB system.

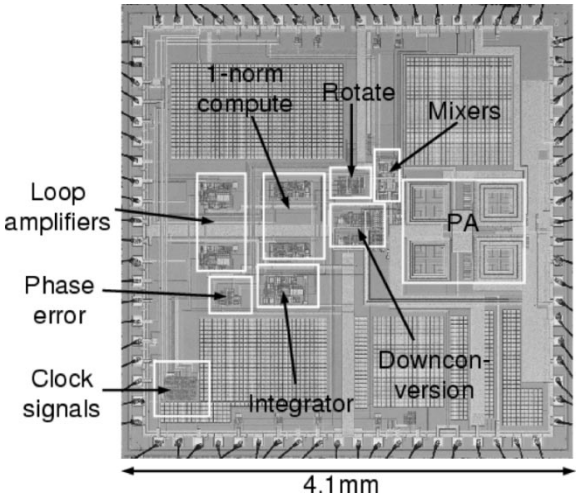

Fig. 17. Die photo.

VIII. Conclusion

This paper represents the first integrated realization of the control concept described in [5]. It was made possible in part by a new technique for analog multiplication, by which this phase-alignment system functioned without manual trimming. As a direct result of the compactness of this phase-alignment solution, we succeeded in designing, fabricating, and testing the first reported IC to have a PA, Cartesian feedback circuitry, and phase-alignment system integrated on a single die.

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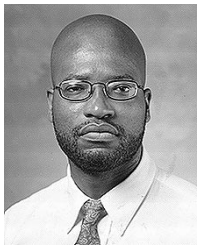

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