A 12-mW Wide Dynamic Range CMOS Front-End for a Portable GPS Receiver

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***Abstract*— This paper describes a CMOS low-noise amplifier (LNA) and mixer intended for use in the front-end of a global positioning system (GPS) receiver. The circuits were implemented in a standard 0.35-μm (drawn) CMOS process, with one poly and two metal layers. The LNA has a forward gain (S21) of 17 dB and a noise figure of 3.8 dB. The mixer has a voltage conversion gain of −3.6 dB and a third-order intermodulation intercept point (IP3) of 10 dBm, input referred. The combination draws 12 mW from a 1.5-V supply.**

***Index Terms*— Amplifier noise, CMOS analog integrated circuits, Global Positioning System, low-noise amplifiers, mixers, receivers.**

I. Introduction

THERE is large enthusiasm in the consumer market for the capabilities of the Global Positioning System (GPS). Manufacturers of cellular telephones, portable computers, and other mobile devices are looking for ways to incorporate GPS into their products. For many of these hand-held devices, one of the primary concerns is battery life. Thus, there is strong motivation to provide good performance at very low power.

The viability of a CMOS low-noise amplifier (LNA) within the context of GPS has been demonstrated previously [1]. This paper extends that work to include the mixer and also investigates a differential LNA architecture. The decision for a differential LNA was made to avoid problems caused by substrate coupling in a single-ended design.

Section II applies the results of [1] to this paper's LNA, in addition to discussing the current LNA's salient features. Section III details the mixer design and addresses the topics of conversion gain, linearity, and noise. Experimental results are presented in Section IV, followed by the authors' conclusions in Section V.

II. LNA

A. LNA Description

Fig. 1 shows a circuit-level description of the LNA. A differential architecture was selected for better rejection of on-chip interference. The penalty for such a decision is that twice the power must be consumed to achieve the same noise figure as a single-ended version.

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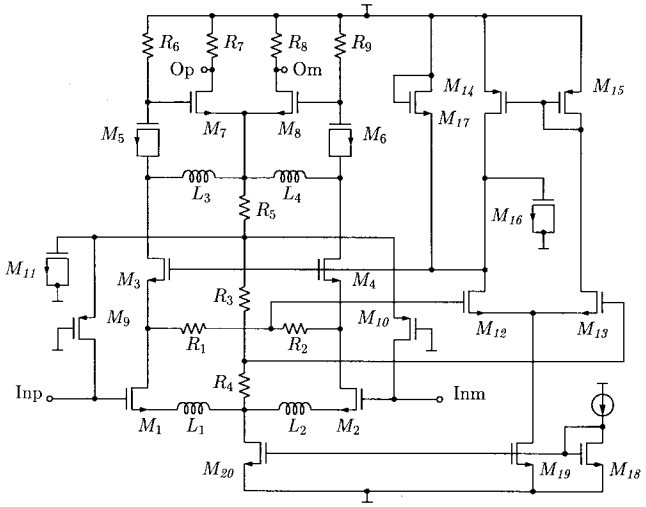

Fig. 1. LNA circuit diagram.

The LNA consists of two stages: the input stage, formed by transistors M_1 through M_4, and the output stage, formed by transistors M_7 and M_8. The input stage is cascoded for a number of reasons. The first is to reduce the influence of the gate-to-drain overlap capacitance $C_{\rm gd}$ on the LNA's input impedance. Specifically, the Miller effect tends to substantially lower the input impedance, complicating the task of matching to the input. In addition to mitigating the Miller effect, the use of a cascode improves the LNA's reverse isolation, which is important in the present application for suppressing local oscillator (LO) feedthrough from the mixer back to the LNA's RF input. Furthermore, because the output of the first stage is tuned with spiral inductors, L_3 and L_4, the LNA's stability might be compromised without the cascode, due to interaction between the inductive load and the input matching network through $C_{\rm gd}$. It should be noted, however, that a noise penalty is incurred when using a cascode. But, with proper attention to the layout of the devices, the additional noise can be minimized, as discussed in the following section.

As shown in Fig. 2, the LNA must present the proper input impedance to terminate the off-chip RF filter preceding it. For this purpose, inductive degeneration is employed in the sources of M_1 and M_2. This degeneration produces a real term in the LNA's input impedance that is used in matching to the filter.

A number of techniques are employed in dc biasing the amplifier. The bias current of the output stage is reused in the input stage, decreasing the power by a factor of two. The low threshold voltage of this process permits four devices to be stacked, provided that adequate bias control is included. The

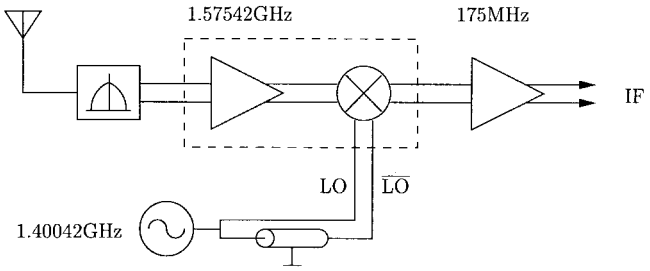

Fig. 2. Block diagram of the receiver front-end.

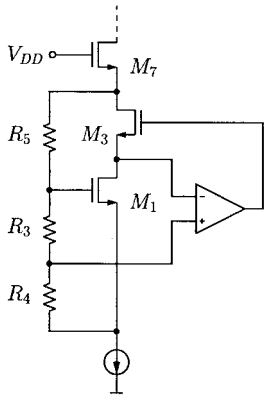

Fig. 3. Single-ended version of the dc biasing technique.

goal is to use the minimum $V_{\rm ds}$ to keep devices M_1 and M_2 in saturation, while leaving some room for signal swing.

Fig. 3 illustrates the active common-mode feedback technique that permits the amplifier to operate reliably on a 1.5-V supply, independent of process, supply, and temperature variations. Resistors R_3 and R_4 sense a fraction of the input devices' common-mode $V_{\rm gs}$ level. This fraction becomes the reference to which the input devices' common-mode $V_{\rm ds}$ level is servoed. An operational amplifier, formed by transistors M_{12} through M_{15}, is used to close the biasing loop, with adjustments to the input devices' common-mode $V_{\rm ds}$ level being made via the gate voltage on the cascode devices. Resistor R_5 permits extra headroom at the drains of M_3 and M_4 since the signal swing at these nodes can be large.

B. LNA Design

Having established the LNA's topology, we now discuss selection of inductor values and transistor sizing. The natural place to start is with the input match, since there is a fixed constraint that the real part of the LNA's input impedance equal the preceding block's output resistance. The amount of inductive source degeneration necessary to achieve this particular input resistance for the LNA is found from

$$R_{\rm in} \approx \frac{2\omega_T L_s}{1+2C_{\rm gd}/C_{\rm gs}} \tag{1}$$

where $R_{\rm in}$ is the differential input resistance and $L_s = L_1 = L_2$ is the source inductance on one side of the LNA. This formula assumes that the cascode devices are the same size as the input devices.

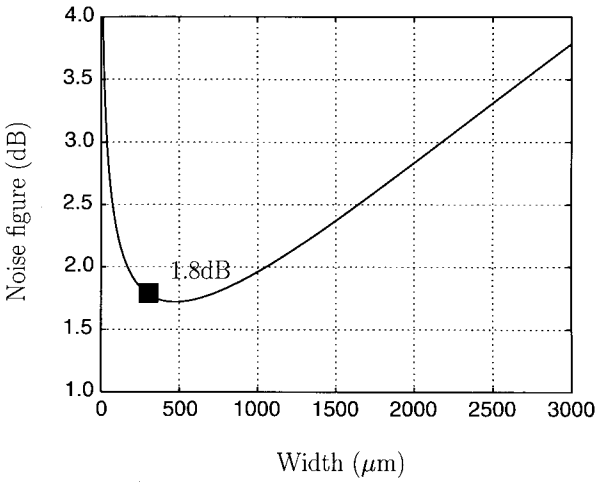

Fig. 4. Theoretical noise figure versus device width ($\gamma = 2.5$, $\delta = 5$, $L = 0.25\ \mu$m, $V_{\rm DD} = 1.5$ V, $P_D = 12$ mW, $R_{\rm in} = 100\ \Omega$).

The other fixed constraint in the design is the carrier frequency of the GPS signal. Thus, the interstage tuning inductors L_3 and L_4 are selected for resonance at the GPS carrier frequency of 1.575 42 GHz. Inductors L_3 and L_4 are implemented with on-chip spiral inductors, as are inductors L_1 and L_2. In designing L_3 and L_4, it is desirable to select spiral geometries that maximize Q, because gain will be maximized by doing so. Loss of signal energy, from mistuning or excessively narrow bandwidths, is not an issue, since the Q's of these structures are typically in the single-digits and accuracy of the inductors is within 10%.

Now we are in a position to investigate the sizing of the input stage's transistors. As hinted earlier, it is important to minimize capacitance at the sources of M_3 and M_4 to reduce their noise contribution. One expedient method is to merge the drains and sources of the bottom transistors and top transistors in the cascode, respectively, and is most readily accomplished by making the widths of M_1–M_4 equal.

The width of the input devices should be selected to optimize the LNA's noise performance. There are two dominant noise contributors in a MOS device: drain thermal noise and induced gate thermal noise [2]. The drain noise current has a power spectral density given by

$$\frac{\overline{i_d^2}}{\Delta f} = 4kT\gamma g_{d0}. \tag{2}$$

Similarly, the gate noise current has a power spectral density of

$$\frac{\overline{i_g^2}}{\Delta f} = 4kT\delta g_g \tag{3}$$

where $g_g = \omega^2 C_{\rm gs}^2/(5g_{d0})$. In these expressions, g_{d0} is the device's zero-bias drain conductance, and γ and δ are coefficients describing the magnitude of the noise powers. In addition to these noise sources, the epitaxial layer's resistance may contribute noise through the body effect. Such epi noise can be accounted for by slightly increasing γ, because this noise source is indistinguishable from drain thermal noise.

According to the theory outlined in [1], there is an optimum width for the input devices that minimizes the amplifier's noise

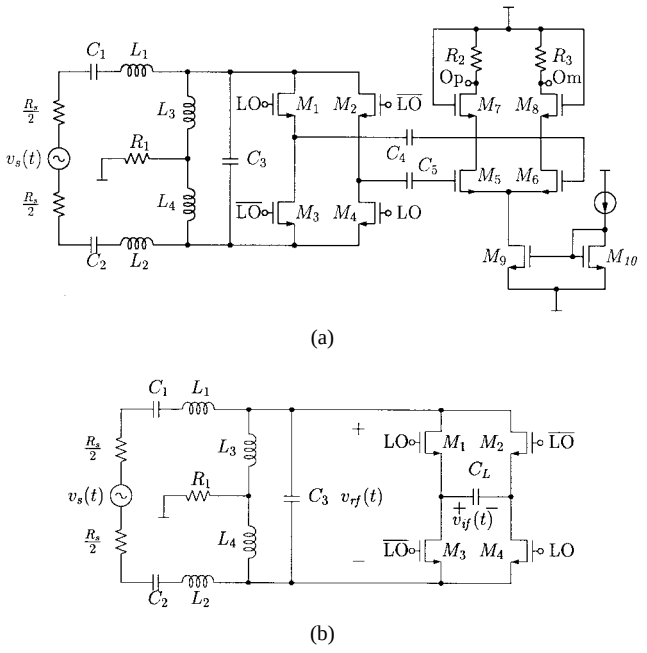

Fig. 5. Mixer circuit diagram. (a) Mixer with probe buffer and (b) mixer circuit used in analysis.

figure for a specified power consumption and input impedance. Note that this optimum exists because the gate noise and drain noise terms are not fully correlated. Fig. 4 plots noise figure as a function of input device width and clearly shows an optimum width of about 500 μm, corresponding to a noise figure of 1.8 dB. Note that this curve represents the theoretical noise contribution of the input devices only.

The implemented width is only 290 μm because the detailed nature of the gate noise was unknown to the authors when this amplifier was designed. However, the curve has a broad minimum, so the achievable noise figure is little affected by using transistors of this width, at least in principle. The discrepancy between the theoretical minimum of 1.8 dB and the measured noise figure of 3.8 dB will be addressed in Section IV.

III. Mixer

A. Mixer Description

The mixer consists of the four transistors, M_1 through M_4, in Fig. 5(a). These four transistors are grouped together into two pairs of two transistors each. Transistors M_1 and M_4 work together and are controlled by the local oscillator signal, while transistors M_2 and M_3 form a unit controlled by the inverse of the LO signal. Each pair serves the function of connecting the intermediate frequency (IF) port to the RF port of the mixer. The difference between the two pairs is the polarity with which they connect the IF port to the RF port. When M_1 and M_4 are on, the IF port is connected with a positive polarity to the RF port. But when M_2 and M_3 are on, the IF port is connected with a negative polarity to the RF port.

A probe buffer, included only for testing purposes, follows the mixer and presents a high impedance load to the mixer while interfacing to off-chip test equipment. A passive filter network precedes the mixer and can be separated into two parts for convenient analysis: an L-match and an RF tank. The L-match is formed by inductors L_1 and L_2 with part of the tank capacitance, C_3, while the RF tank is formed by inductors L_3 and L_4 with the remainder of C_3. L_1 through L_4 are implemented with bondwires, and C_3 is a metal-to-metal capacitor that incorporates lateral flux as well as vertical flux. The purpose of the L-match is to boost the signal voltage across the mixer's RF port via an impedance transformation, while the RF tank is used to filter broad-band noise at the RF port of the mixer. As will be discussed later, this filtering is important because multiple frequencies at the mixer's RF port are converted to the intermediate frequency at the mixer's IF port.

B. Mixer Conversion Gain

Fig. 5(b) shows a simplified mixer circuit that is used in the following analysis.

1) Definition: The voltage conversion gain for this mixer is found by exciting the circuit with a RF sinusoid, $v_s(t) = \cos(2\pi f_{\rm RF}t + \phi_{\rm RF})$, and determining the IF signal amplitude at the IF port. The task of determining voltage conversion gain is broken into two steps. First, the voltage gain between the source and the RF port is computed. Second, the voltage conversion gain between the RF port and the IF port is computed. The mixer's voltage conversion gain is the product of the two steps.

2) Filter Voltage Gain: The mixer's load presents a high impedance, so that during operation there is a negligible effect on the RF port's voltage, $v_{\rm rf}(t)$. Therefore, in calculating $v_{\rm rf}(t)$ it will be assumed that $C_L = 0$. The RF port response is then due to a linear time invariant (LTI) network being acted on by $v_s(t)$, which in the frequency domain is

$$V_{\rm rf}(f) = H(f)V_s(f) \tag{4}$$

where $H(f)$ is the transfer function from the source port to the RF port. Fig. 6(a) shows the passive filter network. In this figure, all parasitic resistances in the tank elements have been lumped into a single resistor, R_t. $H(f_{\rm RF})$ is computed by taking advantage of the observation that the source drives the network at resonance. First, the RF tank is eliminated, and then the L-match. This sequence of reductions is depicted in Fig. 6(b) and (c), respectively. From those simplifications, it is clear that

$$H(f_{\rm RF}) = \frac{R_t}{(Q^2+1)R_s + R_t}\sqrt{Q^2+1} \tag{5}$$

where $Q = \omega_{\rm RF}(L_1 + L_2)/R_s$. Note that if the L-match transforms the source resistance to match the tank resistance $((Q^2+1)R_s = R_t)$, $H(f_{\rm RF}) = \sqrt{Q^2+1}/2$.

In reality, C_L is a few hundred fF, but when compared to C_3, which is $\sim$5 pF, it is small. Still, the load capacitance, together with the conductance of the switches, has some effect on $v_{\rm rf}(t)$. However, the error in assuming $C_L = 0$ for calculating $v_{\rm rf}(t)$ introduces $<$1 dB of error in the voltage conversion gain.

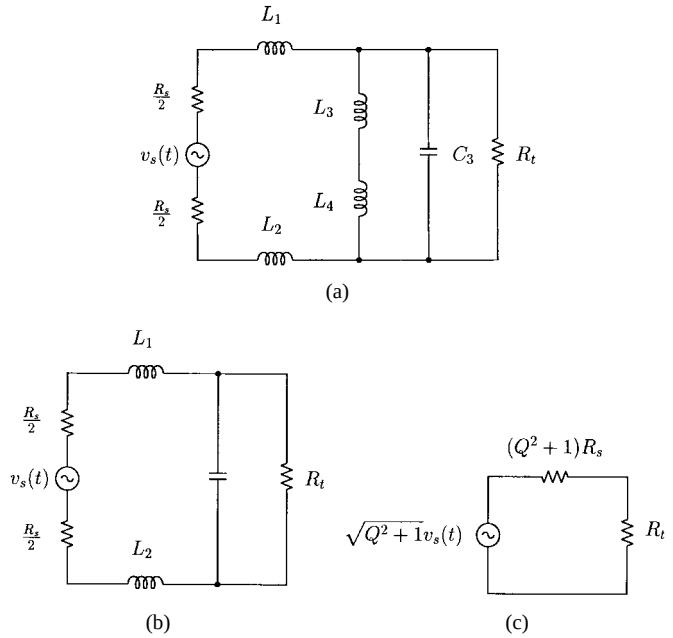

Fig. 6. Illustration of passive network reduction at resonance. (a) Unreduced network, (b) RF tank reduced, and (c) L-match reduced.

3) LO Signals: Before proceeding further, it is relevant to discuss how the mixer is driven, specifically the shapes of the LO and $\overline{\text{LO}}$ waveforms. $\overline{\text{LO}}$ is simply a time-shifted version of LO by $T_{\text{LO}}/2$.

One simple analysis treats the LO waveform as a square wave with 50% duty cycle

$$v_{\text{lo}}(t) = A_{\text{LO}}\Pi(2t/T_{\text{LO}}) * \sum_{n=-\infty}^{\infty} \delta(t - nT_{\text{LO}}) \qquad (6)$$

where $\Pi(t)$ is the rectangle function. This LO signal will be the reference to which other types of LO signals will be compared, and it is sketched in Fig. 7(a).

In practice, a square wave drive is difficult to achieve. A more practical and power-efficient method is to resonate the gate capacitances and drive the gates sinusoidally

$$v_{\text{lo}}(t) = A_{\text{LO}}\cos(2\pi f_{\text{LO}}t + \phi_{\text{LO}}) + B_{\text{LO}} \qquad (7)$$

where B_{LO} is the dc level on the gates. This type of waveform is drawn in Fig. 7(b)–(d) for three choices of B_{LO}. In Fig. 7(b), B_{LO} equals the switch threshold voltage V_{th}; in Fig. 7(c), $B_{\text{LO}} < V_{\text{th}}$ illustrating break-before-make switching action; while in Fig. 7(d), $B_{\text{LO}} > V_{\text{th}}$ which is the opposite action, make-before-break.

4) Mixer's Thévenin Equivalent: The switches in the mixer are just time varying conductances, as shown in Fig. 8(a). Therefore, it is possible to simplify the switch network with a Thévenin equivalent network, generated from C_L's point of view. This is shown in Fig. 8(b), where the open circuit voltage is

$$v_T(t) = \frac{g(t) - g(t - T_{\text{LO}}/2)}{g(t) + g(t - T_{\text{LO}}/2)} v_{\text{rf}}(t) = m(t)v_{\text{rf}}(t) \qquad (8)$$

and the Thévenin impedance, written as a conductance, is

$$g_T(t) = \frac{g(t) + g(t - T_{\text{LO}}/2)}{2}. \qquad (9)$$

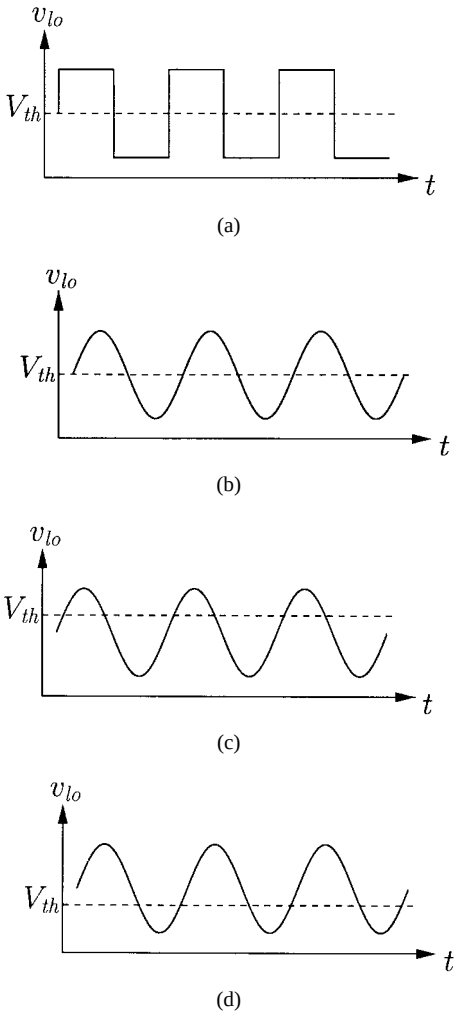

Fig. 7. Four LO signals investigated. (a) Square wave drive, (b) sinusoidal drive, (c) break-before-make, and (d) make-before-break.

The action of mixing, or frequency translation, is implicit in this transformation to a Thévenin equivalent. This is most easily seen in the reference case, when the LO drive is a square wave. The open circuit voltage is a square wave with zero dc value and unit amplitude multiplied by the RF port's voltage, and so $v_T(t)$ is a mixed version of $v_{\text{rf}}(t)$. Fig. 9 illustrates the mixing function

$$m(t) = \frac{g(t) - g(t - T_{\text{LO}}/2)}{g(t) + g(t - T_{\text{LO}}/2)} \qquad (10)$$

and $g_T(t)$, for the four cases.

Both $m(t)$ and $g_T(t)$ exhibit important properties. The mixing function $m(t)$ has no dc component, is periodic with a period of T_{LO}, and has half wave symmetry, implying that it only has odd frequency content (nf_{LO}, where n is an odd integer). The conductance $g_T(t)$ has a dc component and is periodic with a period $T_{\text{LO}}/2$.

5) Core Conversion Gain: If we return to the previous assumption that $C_L = 0$, then $v_{\text{if}}(t) = v_T(t)$. To find the conversion gain from the RF port to the IF port, the Fourier transform of the mixing function must be evaluated at f_{LO}, which has been done in Table I. It is interesting to note that $|M(f_{\text{LO}})|$ in the last two cases depends only

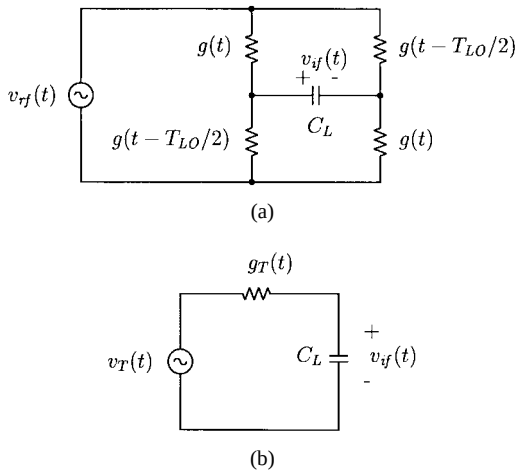

Fig. 8. Mixer core. (a) Time varying conductances and (b) Thévenin equivalent.

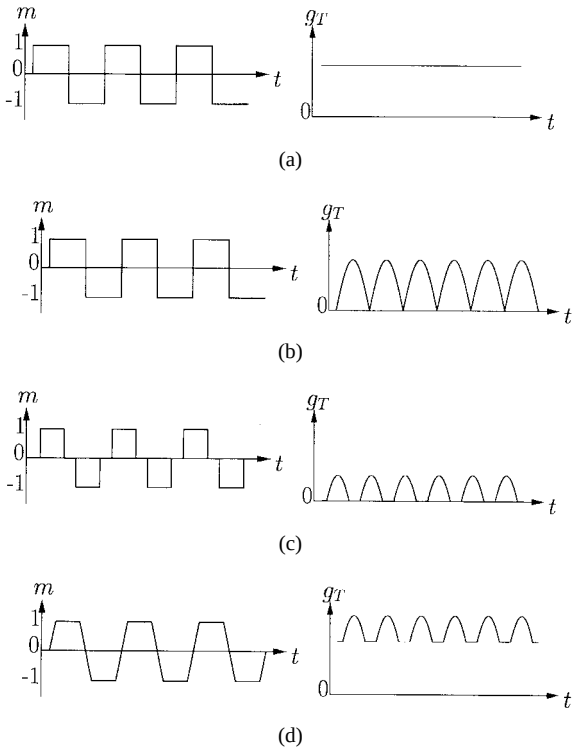

Fig. 9. Mixing function and Thévenin conductance for the four cases. (a) Square wave drive, (b) sinusoidal drive, (c) break-before-make, and (d) make-before-break.

on a single quantity that characterizes an LO waveform, r. The total voltage conversion gain follows and is equal to $|H(f_{\rm RF})||M(f_{\rm LO})|$, where $M(f)$ is the Fourier transform of $m(t)$.

In general, C_L does not equal zero. This case can be solved through a more lengthy analysis. The superposition integral is used to find $v_{\rm if}(t)$ as a function of $v_{\rm rf}(t)$, after finding the network's impulse response. The detailed derivations are contained in the Appendix, while key results are presented here. The results indicate that under certain conditions, a very simple system can be used to analyze the core conversion gain. Furthermore, the results also predict that it is theoretically possible to achieve a core conversion gain of one.

TABLE I
$|M(f_{\rm LO})|$ FOR THE FOUR CASES

Square wave drive	$2/\pi$
Sinusoidal drive	$2/\pi$
Break-before-make	$(2/\pi)\sqrt{1-r^2}$
Make-before-break	$\begin{cases} \frac{\sin^{-1}(r)/r+\sqrt{1-r^2}}{\pi} & 0 \le r \le 1 \\ 1/(2r) & 1 \le r < \infty \end{cases}$

$$r = \frac{|V_{th} - B_{LO}|}{A_{LO}}$$

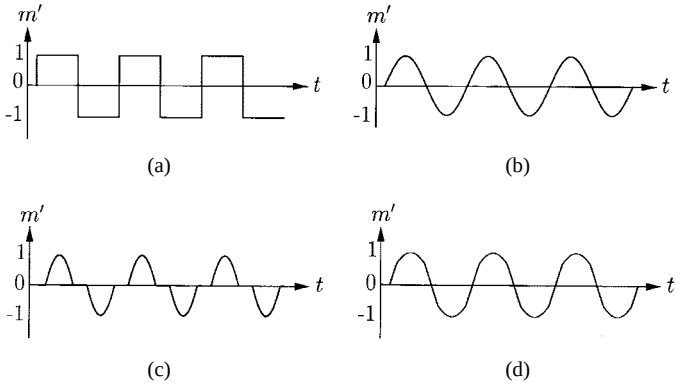

Fig. 10. Modified mixing functions for the four cases. (a) Square wave drive, (b) sinusoidal drive, (c) break-before-make, and (d) make-before-break.

The following discussion applies if $\overline{g_T}/(2\omega_{\rm LO}C_L) \ll 1$, where $\overline{g_T}$ is the dc level of $g_T(t)$. For this case, the superposition integral reduces to

$$v_{\rm if}(t) = \int_{-\infty}^{t} \frac{\overline{g_T}}{C_L} e^{-\frac{\overline{g_T}}{C_L}(t-\tau)} \frac{g_T(\tau)}{\overline{g_T}} m(\tau) v_{\rm rf}(\tau)\, d\tau. \quad (11)$$

This equation provides insight into the mixer's behavior. The RF port's voltage is evidently multiplied by a modified mixing function, which we will define as

$$m'(t) = \frac{g_T(t)}{g_{T\max}} m(t) \quad (12)$$

where $g_{T\max}$ is the peak conductance of $g_T(t)$, normalizing $m'(t)$ to vary between -1 and 1. This modified mixing function appears in Fig. 10 for the four cases, and governs how frequencies are translated. $g_{T\max}$ is also introduced to highlight a gain term

$$A = \frac{g_{T\max}}{\overline{g_T}} \quad (13)$$

which is the ratio of the peak conductance to the average conductance. With these definitions, (11) can be expressed as

$$v_{\rm if}(t) = \int_{-\infty}^{t} \frac{\overline{g_T}}{C_L} e^{-\frac{\overline{g_T}}{C_L}(t-\tau)} A m'(\tau) v_{\rm rf}(\tau)\, d\tau. \quad (14)$$

The remaining terms implement a very familiar component. A simple single-pole low-pass filter is shown in Fig. 11. The superposition integral, which reduces to a convolution integral, for this case is

$$v_{\rm out}(t) = \int_{-\infty}^{t} \frac{g}{C} e^{-\frac{g}{C}(t-\tau)} v_{\rm in}(\tau)\, d\tau. \quad (15)$$

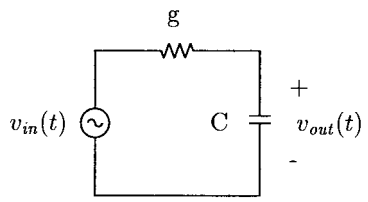

Fig. 11. Single-pole low-pass filter.

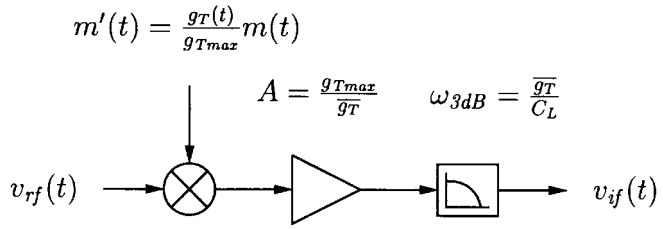

Fig. 12. Equivalent block diagram for core conversion gain.

By comparing (15) to (14), we see that (14) has the same form as (15), except g is replaced by the average conductance, $\overline{g_T}$. Now, (14) can be expressed as

$$v_{\rm if}(t) = \int_{-\infty}^{t} h_{\rm lpf}(t-\tau) A m'(\tau) v_{\rm rf}(\tau)\, d\tau. \qquad (16)$$

In words, this equation indicates that the RF port's voltage is multiplied, gained, and then filtered by a single-pole low-pass filter, as diagrammed in Fig. 12. The total voltage conversion gain is just $A|H(f_{\rm RF})||M'(f_{\rm LO})||H_{\rm lpf}(f_{\rm IF})|$.

It is very intriguing to discover that $Am'(t)$ for a sine wave with $B_{\rm LO} = V_{\rm th}$ gives rise to a *better* conversion gain, by a factor of $\pi^2/8$, than $Am'(t)$ for the reference square wave drive. For a sinusoidal drive, $|M'(f_{\rm LO})| = 1/2$, whereas for a square wave drive, $|M'(f_{\rm LO})| = 2/\pi$. But notice in the square wave case, the peak-to-average conductance is unity, while in the sinusoidal case, the gain A is $\pi/2$. When we take the product $A|M'(f_{\rm LO})|$ the total multiplication factor for a sinusoidal drive is $\pi/4$ (-2.1 dB), which *exceeds* the $2/\pi$ (-3.9 dB) value for a square wave drive.

Observing that the conversion gain of a sinusoidal drive is better than that for a square wave drive motivates examination of the conversion gain for the specific case of a break-before-make drive. It is possible, though slightly involved, to express conversion gain as a function of r once again

$$A|M'(f_{\rm LO})| = \frac{\cos^{-1}(r) - r\sqrt{1-r^2}}{2[\sqrt{1-r^2} - r\cos^{-1}(r)]} \approx \left(1 - \frac{\pi}{4}\right) r + \frac{\pi}{4} \qquad (17)$$

where $r = (V_{\rm th} - B_{\rm LO})/A_{\rm LO}$. Fig. 13 plots (17) as a function of r. The voltage conversion gain actually improves as $r \to 1$, contrary to widely held beliefs. $r = 0$ corresponds to a sine wave with $B_{\rm LO} = V_{\rm th}$. $r = 1$ is the extreme of break-before-make action where each switch is on for just one instant of a LO cycle. Although the conversion gain is higher for $r = 1$, linearity suffers, so this drive is not a practical one.

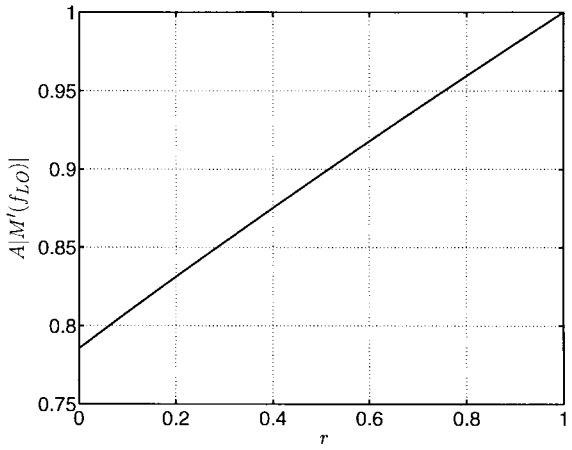

Fig. 13. $A|M'(f_{\rm LO})|$ versus r for break-before-make.

C. Mixer Linearity

There are two major sources of distortion in the mixer: device nonlinearities and phase modulation of the switching instants.

To improve the linearity of the transistors, it is most important to keep the current through the switches small to reduce nonlinear voltage drops across the devices [3]. This criterion is satisfied with the use of a small capacitive load, which presents a high impedance to the output. The remaining nonlinearities consist of parasitic junction capacitances, which are weak nonlinearities. Furthermore, at the RF port, the parasitic junction capacitances are insignificant compared with the large, linear tank capacitance C_3.

A second source of distortion arises from phase modulation of the mixing function by the RF voltage, just as in diode ring mixers [4]. Borrowing from the research on diode rings, we may expect this type of distortion to diminish if larger LO drive levels are used to steepen the LO waveform's slope as it passes through zero. A corollary is that square wave drives will lead to improved linearity over sinusoid drives if this is the dominant source of nonlinearity. References [3] and [4] contain more detailed treatments of this type of distortion.

D. Mixer Noise Figure

In an LTI system, a single frequency excitation produces responses in the system at only that frequency. In contrast, in a linear periodically time varying (LPTV) system, a single frequency excitation produces responses at a number of different frequencies [5]. A corollary is that the response at a particular frequency can be due to a number of different single frequency inputs.

The modified mixing function is capable of translating frequencies at the RF port by odd multiples of $f_{\rm LO}$. Thus the frequencies in the set, $f_{\rm IF} + nf_{\rm LO}$, where n is an odd integer, can all translate to the IF port's IF frequency from the RF port. The RF tank placed across the RF port suppresses the conversion of the undesirable frequencies to the output.

The dominant source of noise is from the switches. In general, it is desirable for the switches to be very wide, to reduce their on resistance and associated thermal noise.

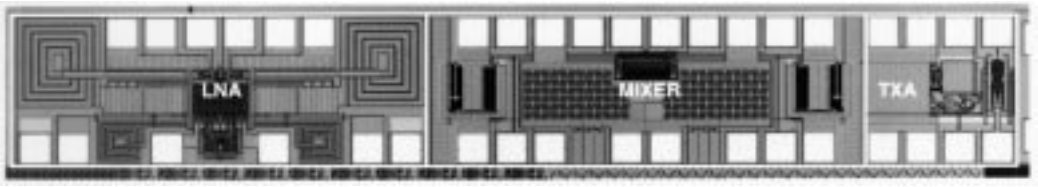

Fig. 14. Die photo.

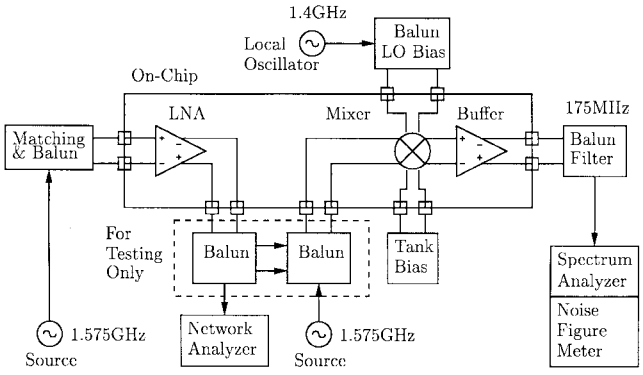

Fig. 15. Block diagram of the GPS front-end test setup.

However, making the switches very wide increases their contribution to the load capacitance, which eventually reduces conversion gain. Also, LO power increases as the switches are made wider because a smaller inductance must be used to resonate the gates. For a fixed Q, this results in a smaller parallel resistance. Thus, in sizing the switches for a given LO drive, one should increase switch width until conversion gain starts to drop, and then stop.

There is one additional point regarding the passive mixer structure that warrants special attention. Since there is no dc current through the switches, there is no $1/f$ noise. This consideration is particularly important in direct conversion architectures.

For a more thorough treatment of the general subject of noise in mixers, the interested reader can refer to [5].

IV. Experimental Results

The LNA and mixer were integrated in a 0.35-μm CMOS technology with only two metal layers. A die photograph is shown in Fig. 14. The aspect ratio of the silicon is somewhat unusual because this project was designed to fit in the scribe lane of a wafer that was primarily devoted to other dice. Accordingly, the dimensions are 350 μm $\times$ 2.4 mm.

Fig. 15 shows how the die was packaged for testing, and important comments regarding testing follow. First, the interface between the LNA and the mixer was taken off-chip to facilitate testing only. By doing so, each block could be tested individually. In a real chip, the LNA would interface on-chip directly to the mixer. Second, the probe buffer, following the mixer, is used to measure the mixer's output. It was designed so that its linearity does not interfere with the mixer linearity measurement. In a real chip, an IF amplifier would replace the probe buffer, and since test equipment no longer needs to be driven, design of the IF amplifier can proceed without having to drive a 50-Ω load. Finally, because the circuits are differential, baluns were required to interface to the single-ended test instrumentation. By using surface mount hybrid baluns, the insertion loss may be on the order of 0.8 dB or less per balun. In a complete integrated receiver system, only one balun would be required to transform the single-ended signal from the antenna and RF filter into differential form. Particular surface acoustic wave (SAW) filters naturally provide a differential output in which case a balun is not necessary.

TABLE II
GPS Front-End Performance Summary

Low-Noise Amplifier	
Frequency	1.57542GHz
Noise Figure	3.8dB
S21	17.0dB
S12	$\leq$ -52dB
IP3 (Input)	-6dBm
1dB Compression (Input)	-20dBm
Power Dissipation	12mW
Mixer	
LO Frequency	1.40042GHz
LO Amplitude	300mV ($\approx$-3.5dBm in 100Ω)
Voltage Conversion Gain	-3.6dB
IP3 (Input)	10dBm
1dB Compression (Input)	-5dBm
Noise Figure (SSB)	10dB
Supply Voltage	1.5V
Technology	0.35μm CMOS
Die Area	0.84mm^2

The results of experimental measurements are summarized in Table II and discussed in detail below. In the discussion that follows, "dBm" is used in its original, rigorous sense: the signal power referenced to 1 mW and expressed in dB. In cases where the impedance is not well known (and hence, the power difficult to quantify), voltage units are used explicitly to avoid confusion.

A. LNA

The test board for the LNA used a low-loss dielectric and contained auxiliary test structures to permit measurement of the insertion loss of board traces, baluns, and connectors. As a result, the noise figure of the LNA could be measured with a precision of $\sim\pm$0.2 dB.

As noted previously, the measured noise figure diverges from the theoretical minimum of 1.8 dB predicted in Section II. In part, this difference is due to the fact that

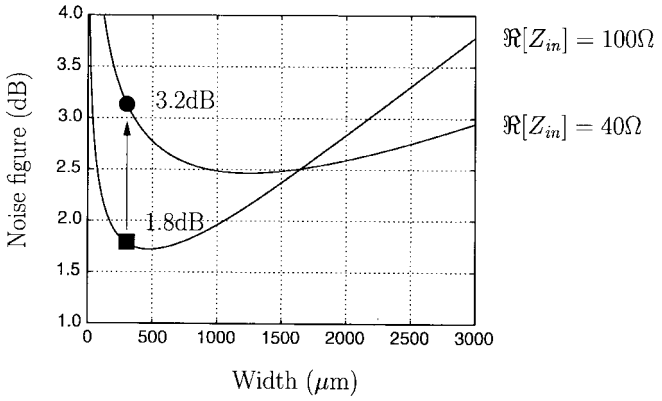

Fig. 16. Noise figure versus device width for $R_{\text{in}} = 100\ \Omega$ and $R_{\text{in}} = 40\ \Omega$.

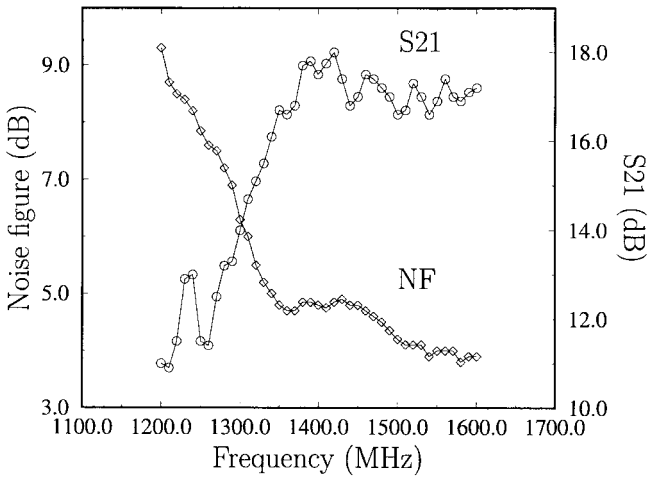

Fig. 17. LNA noise figure/S21 measurement.

the complete amplifier has more than one noise contributor; however this is not sufficient to account for the discrepancy.

A measurement of the input impedance of the LNA revealed the primary reason for the difference. The real part of the input impedance was found to be only 40-Ω differential, rather than the desired 100-Ω differential. This gross difference is partially due to the influence of the overlap capacitance of the input devices, which lowers the impedance seen at the gates of those devices. This behavior was observed in simulations of the LNA's input impedance, but unfortunately, the impact of the reduced impedance on the noise figure was not fully appreciated at the time. Furthermore, increasing the inductance of the source spiral inductors L_1 and L_2, which is necessary to combat this effect, would reduce the LNA's gain, leading to an increase in the mixer's relative noise contribution.

The noise figure curve of the earlier section can be replotted in light of this information. Because we are matching to a lower impedance, one might expect the noise contribution of the input devices to be more significant relative to this reduced impedance. Indeed, this is the case, as is evident in the plot of Fig. 16. Both noise figure plots represent predictions for the performance of an isolated device of the stated width, assuming 12 mW power consumption in the final amplifier. As can be seen, the chosen width of 290 μm is substantially removed from the optimum point on the 40-Ω curve. Also, the optimum point on this new curve is itself 0.7 dB higher than on the 100-Ω curve. These compounding effects illustrate the penalty in undershooting the desired input impedance.

The revised prediction anticipates a 3.2-dB noise figure from the input pair alone. Thus, the observed total noise figure of 3.8 dB is reasonable, given that other devices in the circuit contribute noise in a second-order fashion. For example, the cascode devices, the load inductors, and the output stage transistors all have noise, which contributes some small amount to the noise figure. The forward gain (S21) and noise figure are plotted in Fig. 17.

One salient feature of the differential LNA architecture that merits discussion is its reverse gain (S12), which was measured to be less than -52 dB between 1 and 2 GHz. Good reverse isolation is required to attenuate local oscillator leakage from the mixer back to the RF input of the LNA. The use of a cascode structure in the LNA's input stage helps to reduce reverse feedthrough, and this good reverse isolation is augmented by the fact that the substrate appears as an incremental ground, to first order, for differential signals.

B. Mixer

The mixer was measured separately from the LNA to determine its characteristics. The voltage conversion gain, as defined in an earlier section, is -3.6 dB. The measurement was performed with the input port of the mixer impedance matched to 100-Ω differential. Note that, without the impedance transformation of the L-match network, the expected voltage conversion gain should be close to -10 dB. This value includes -6 dB for the voltage attenuation from matching the input port and -4 dB for the mixer core conversion gain. We may infer that the Q of the L-match is approximately 1.8, resulting in a factor of 2.1 step up in voltage before the mixer. The RF tank thus presents an equivalent parallel resistance of about 440 Ω at resonance, corresponding to a total network Q of about 11.

The linearity of the mixer was measured with a two-tone IP3 test with tones at 1.575 and 1.585 GHz. The result is plotted in Fig. 18. The fundamental output amplitude is extrapolated along a line of unity slope, while the third-order intermodulation products (IM3) are extrapolated along a line with a slope of three, using the products at higher source power as a reference. The IP3 is about 10 dBm, input-referred, for a differential LO amplitude of 300 mV. This LO amplitude is equivalent to -3.5 dBm in a 100-Ω impedance. Note, however, that the terminating impedance for the LO port need not be 100 Ω if the LO were integrated with the mixer. Indeed, a higher impedance could be achieved with spiral inductor tuning of the LO port to further reduce LO power.

The single-sideband (SSB) noise figure of the mixer is estimated to be 10 dB based on noise figure measurements of the mixer/buffer combination. Given the gain of the preceding LNA, the mixer contributes 0.3 dB to the noise figure of the LNA/mixer combination. The IP3 of the combination is approximately -11.1 dBm, input-referred. Using these two numbers, we can calculate that the peak dynamic range is 61 dB at a source power level of -43 dBm.

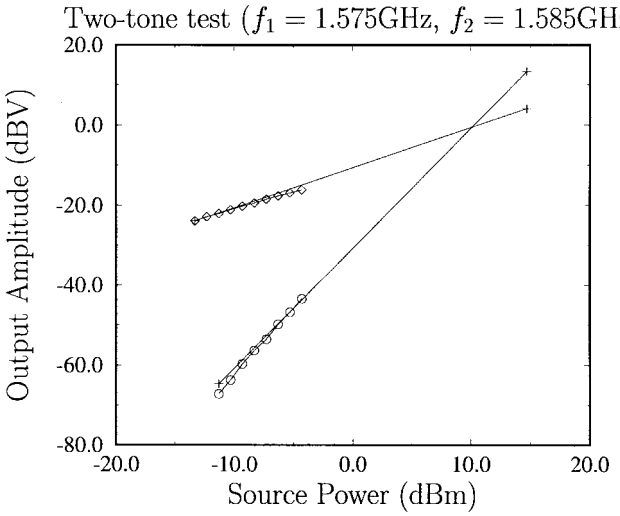

Fig. 18. Mixer two-tone IP3 measurement.

V. Conclusion

A functional LNA/mixer combination for a CMOS GPS receiver has been presented. The LNA's measured reverse gain (S12) of -52 dB indicates that the differential configuration will greatly outperform a single-ended version in the presence of on-chip interference, justifying the power penalty. The passive mixer also presents a suitable balance between linearity and noise figure, at a very low power cost. The discussion presented in the section on mixer conversion gain provides guidance in the design of this type of mixer and establishes a foundation for exploring other topics relevant to mixers.

Appendix
Impulse Response and Superposition Integral for Mixer Core

An impulse is applied to the circuit in Fig. 8(b) at time τ, $v_T(t) = \delta(t-\tau)$. To determine the initial voltage produced on C_L, the Thévenin equivalent circuit is transformed into a Norton equivalent circuit with the following short circuit current:

$$i_N(t) = g_T(t)v_T(t) = g_T(\tau)\delta(t-\tau). \tag{18}$$

The total charge delivered to the capacitor as a result of the impulse in voltage is $g_T(\tau)$ coulombs. This charge produces an initial voltage of $g_T(\tau)/C_L$ V on C_L at time τ. Then, the following differential equation describes the circuit's response to this initial condition:

$$C_L\frac{dv_{\rm if}(t)}{dt} = -g_T(t)v_{\rm if}(t). \tag{19}$$

The solution has the form $h(t) = Ae^{-f(t)}$. Combining the initial condition with this solution, and noting that the system is causal, yields

$$h(t,\tau) = \frac{g_T(\tau)}{C_L}e^{-\int_\tau^t \frac{g_T(s)}{C_L}ds}u(t-\tau) \tag{20}$$

where $u(t)$ is the unit step function. Finally, using (20) in the superposition integral produces

$$v_{\rm if}(t) = \int_{-\infty}^{t}\frac{g_T(\tau)}{C_L}e^{-\int_\tau^t \frac{g_T(s)}{C_L}ds}m(\tau)v_{\rm rf}(\tau)\,d\tau. \tag{21}$$

Some useful manipulations are enabled if $g_T(t)$ is written as

$$g_T(t) = \overline{g_T} + \sum_{n=1}^{\infty}a_n\cos(n2\omega_{\rm LO}t+\phi_n) = \overline{g_T} + \widetilde{g_T}(t) \tag{22}$$

where $\overline{g_T}$ is the dc level of $g_T(t)$. Furthermore, the integral of $\widetilde{g_T}(t)$ will be called $\widetilde{f_T}(t)$

$$\widetilde{f_T}(t) = \frac{\overline{g_T}}{2\omega_{\rm LO}}\sum_{n=1}^{\infty}\frac{a_n\sin(n2\omega_{\rm LO}t+\phi_n)}{n\overline{g_T}} + K \tag{23}$$

where K is an arbitrary constant. These modifications allow us to write

$$v_{\rm if}(t) = e^{\frac{\widetilde{f_T}(t)}{C_L}}\int_{-\infty}^{t}\frac{\overline{g_T}}{C_L}e^{-\frac{\overline{g_T}}{C_L}(t-\tau)}e^{-\frac{\widetilde{f_T}(\tau)}{C_L}} \times\frac{g_T(\tau)}{\overline{g_T}}m(\tau)v_{\rm rf}(\tau)\,d\tau. \tag{24}$$

This last result warrants close attention. The exponentials involving $\widetilde{f_T}$ have a coefficient that multiplies a series of normalized sinusoids. This coefficient is equal to

$$\frac{\overline{g_T}}{2\omega_{\rm LO}C_L} \tag{25}$$

and gives rise to three cases: if it is much less than one, the exponentials involving $\widetilde{f_T}$ reduce to one; if it is much greater than one, the result for $C_L = 0$ should be used; or if it is between these two extremes, the impact of the two exponential terms involving $\widetilde{f_T}$ is ambiguous.

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References

[1] D. K. Shaeffer and T. H. Lee, "A 1.5 V, 1.5 GHz CMOS low noise amplifier," *IEEE J. Solid-State Circuits*, vol. 32, pp. 745–759, May 1997.
[2] A. van der Ziel, *Noise in Solid State Devices and Circuits*. New York: Wiley, 1986.
[3] H. P. Walker, "Sources of intermodulation in diode-ring mixers," *Radio Electron. Eng.*, vol. 46, no. 5, pp. 247–255, May 1976.
[4] J. G. Gardiner, "The relationship between cross-modulation and intermodulation distortions in the double-balanced modulator," *Proc. IEEE*, vol. 56, pp. 2069–2071, Nov. 1968.
[5] C. D. Hull and R. G. Meyer, "A systematic approach to the analysis of noise in mixers," *IEEE Trans. Circuits Syst. I*, vol. 40, pp. 909–919, Dec. 1993.

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Derek K. Shaeffer (S'90), for a photograph and biography, see p. 759 of the May 1997 issue of this JOURNAL.

Thomas H. Lee (S'87–M'87), for a photograph and biography, see this issue, p. 1857.