Jitter and Phase Noise in Ring Oscillators

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***Abstract*—A companion analysis of clock jitter and phase noise of single-ended and differential ring oscillators is presented. The impulse sensitivity functions are used to derive expressions for the jitter and phase noise of ring oscillators. The effect of the number of stages, power dissipation, frequency of oscillation, and short-channel effects on the jitter and phase noise of ring oscillators is analyzed. Jitter and phase noise due to substrate and supply noise is discussed, and the effect of symmetry on the upconversion of $1/f$ noise is demonstrated. Several new design insights are given for low jitter/phase-noise design. Good agreement between theory and measurements is observed.**

***Index Terms*—Design methodology, jitter, noise measurement, oscillator noise, oscillator stability, phase jitter, phase-locked loops, phase noise, ring oscillators, voltage-controlled oscillators.**

I. Introduction

DUE to their integrated nature, ring oscillators have become an essential building block in many digital and communication systems. They are used as voltage-controlled oscillators (VCO's) in applications such as clock recovery circuits for serial data communications [1]–[4], disk-drive read channels [5], [6], on-chip clock distribution [7]–[10], and integrated frequency synthesizers [10], [11]. Although they have not found many applications in radio frequency (RF), they can be used for some low-tier RF systems.

Recently, there has been some work on modeling jitter and phase noise in ring oscillators. References [12] and [13] develop models for the clock jitter based on time-domain treatments for MOS and bipolar differential ring oscillators, respectively. Reference [14] proposes a frequency-domain approach to find the phase noise based on an linear time-invariant model for differential ring oscillators with a small number of stages.

In this paper, we develop a parallel treatment of frequency-domain phase noise [15] and time-domain clock jitter for ring oscillators. We apply the phase-noise model presented in [16] to obtain general expressions for jitter and phase noise of the ring oscillators.

The next section briefly reviews the phase-noise model presented in [16]. In Section III, we apply the model to timing jitter and develop an expression for the timing jitter of oscillators, while Section IV provides the derivation of a closed-form expression to calculate the rms value of the impulse sensitivity function (ISF). Section V introduces expressions for jitter and phase noise in single-ended and differential ring oscillators in long- and short-channel regimes of operation. Section VI describes the effect of substrate and supply noise as well as the noise due to the tail-current source in differential structures. Section VII explains the design insights obtained from this treatment for low jitter/phase-noise design. Section VIII summarizes the measurement results.

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II. Phase Noise

The output of a practical oscillator can be written as

$$V_{\text{out}}(t) = A(t) \cdot f[\omega_0 t + \phi(t)] \tag{1}$$

where the function f is periodic in 2π and $\phi(t)$ and $A(t)$ model fluctuations in amplitude and phase due to internal and external noise sources. The amplitude fluctuations are significantly attenuated by the amplitude limiting mechanism, which is present in any practical stable oscillator and is particularly strong in ring oscillators. Therefore, we will focus on phase variations, which are not quenched by such a restoring mechanism.

As an example, consider the single-ended ring oscillator with a single current source on one of the nodes shown in Fig. 1. Suppose that the current source consists of an impulse of current with area Δq (in coulombs) occurring at time $t = \tau$. This will cause an instantaneous change in the voltage of that node, given by

$$\Delta V = \frac{\Delta q}{C_{\text{node}}} \tag{2}$$

where C_{node} is the effective capacitance on that node at the time of charge injection. This produces a shift in the transition time. For small ΔV, the change in the phase $\phi(t)$ is proportional to the injected charge

$$\Delta\phi = \Gamma(\omega_0 t)\frac{\Delta V}{V_{\text{swing}}} = \Gamma(\omega_0 t)\frac{\Delta q}{q_{\text{swing}}} \tag{3}$$

where V_{swing} is the voltage swing across the capacitor and $q_{\text{swing}} = C_{\text{node}} V_{\text{swing}}$. The dimensionless function $\Gamma(\omega_0 t)$ is the time-varying proportionality constant and is periodic in 2π. It is large when a given perturbation causes a large phase shift and small where it has a small effect [16]. Since $\Gamma(x)$ thus represents the sensitivity of every point of the waveform to a perturbation, $\Gamma(x)$ is called the *impulse sensitivity function*.

The time dependence of the ISF can be demonstrated by considering two extreme cases. The first is when the impulse is injected during a transition; this will result in a large phase shift. As the other case, consider injecting an impulse while the output is saturated to either the supply or the ground. This impulse will have a minimal effect on the phase of the oscillator, as shown in Fig. 2.

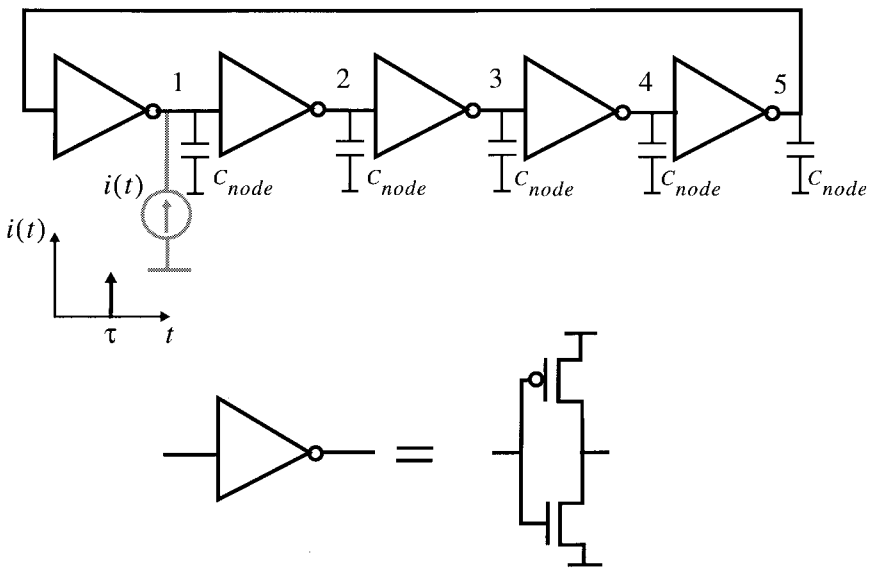

Fig. 1. Five-stage inverter-chain ring oscillator.

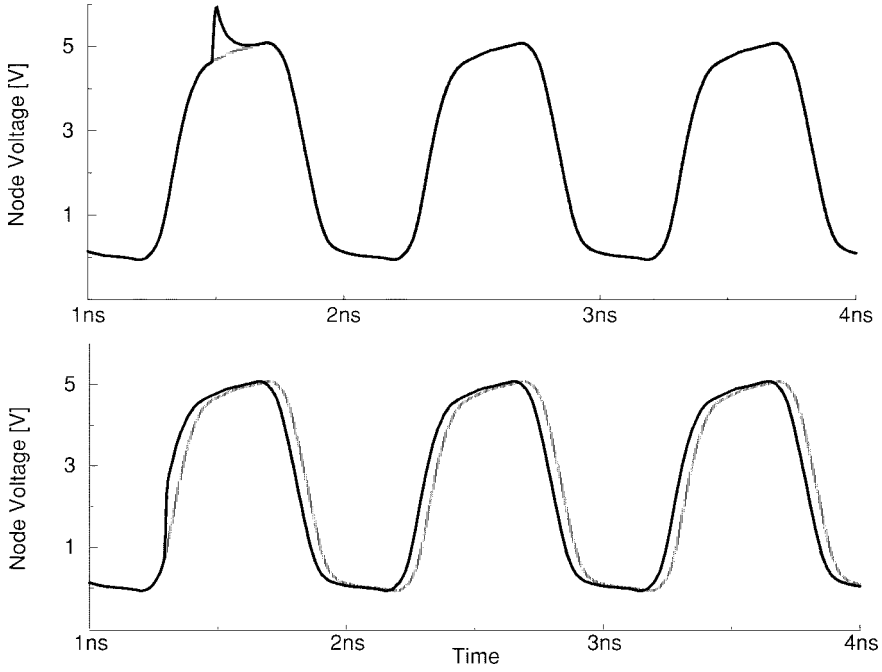

Fig. 2. Effect of impulses injected during transition and peak.

Being interested in its phase $\phi(t)$, we can treat an oscillator as a system that converts voltages and currents to phase. As is evident from the discussion leading to (3), this system is linear for small perturbations. It is also time variant, no matter how small the perturbations are.

Unlike amplitude changes, phase shifts persist indefinitely, since subsequent transitions are shifted by the same amount. Thus, the phase impulse response of an oscillator is a time-varying step. Also note that as long as the introduced change in the voltage due to the current impulse is small, the resultant phase shift is linearly proportional to the injected charge, and hence the transfer function from current to phase is linear.

The unit impulse response of the system is defined as the amount of phase shift per unit current impulse [16]. Based on the foregoing argument, we obtain the following time-dependent impulse response:

$$h_\phi(t,\tau) = \frac{\Gamma(\omega_0\tau)}{q_{\max}} u(t-\tau) \tag{4}$$

where $u(t)$ is a unit step.

Knowing the response to an impulse, we can calculate $\phi(t)$ in response to any injected current using the superposition integral

$$\begin{aligned}\phi(t) &= \int_{-\infty}^{\infty} h_\phi(t,\tau) i(\tau)\, d\tau \\ &= \int_{-\infty}^{t} \frac{\Gamma(\omega_0\tau)}{q_{\max}} i(\tau)\, d\tau \end{aligned} \tag{5}$$

where $i(t)$ represents the noise current injected into the node of interest. Note that the integration arises from the closed-loop nature of the oscillator. The single-sideband phase-noise spectrum due to a white-noise current source is given by [16][1]

$$L\{f_{\rm off}\} = \frac{\Gamma_{\rm rms}^2}{8\pi^2 f_{\rm off}^2} \cdot \frac{\overline{i_n^2}/\Delta f}{q_{\max}^2} \tag{6}$$

where $\Gamma_{\rm rms}$ is the rms value of the ISF, $\overline{i_n^2}/\Delta f$ is the single-sideband power spectral density of the noise current source, and $f_{\rm off}$ is the frequency offset from the carrier. In the case of multiple noise sources injecting into the same node, $\overline{i_n^2}/\Delta f$ represents the total current noise due to all the sources and is given by the sum of individual noise power spectral densities [17]. If the noise sources on different nodes are uncorrelated, the waveform (and hence the ISF) of all the nodes are the same except for a phase shift, assuming identical stages. Therefore, the total phase noise due to all N noise sources is N times the value given by (6) (or $2N$ times for a differential ring oscillator).

From (5), it follows that the upconversion of low-frequency noise, such as $1/f$ noise, is governed by the dc value of the ISF. The corner frequency between $1/f^2$ and $1/f^3$ regions in the spectrum of the phase noise is called f_{1/f^3} and is related to the $1/f$ noise corner $f_{1/f}$ through the following equation [16]:

$$f_{1/f^3} = f_{1/f} \cdot \frac{\Gamma_{\rm dc}^2}{\Gamma_{\rm rms}^2} \tag{7}$$

where $\Gamma_{\rm dc}$ is the dc value of the ISF. Since the height of the positive and negative lobes of the ISF is determined by the slope of the rising and falling edges of the output waveform, respectively, symmetry of the rising and falling edges can reduce $\Gamma_{\rm dc}$ and hence the upconversion of $1/f$ noise.

III. Jitter

In an ideal oscillator, the spacing between transitions is constant. In practice, however, the transition spacing will be variable. This uncertainty is known as clock jitter and increases with measurement interval ΔT (i.e., the time delay between the reference and the observed transitions), as illustrated in Fig. 3. This variability accumulation (i.e., "jitter accumulation") occurs because any uncertainty in an earlier transition affects all the following transitions, and its effect persists indefinitely. Therefore, the timing uncertainty when ΔT seconds have elapsed is the sum of the uncertainties associated with each transition.

The statistics of the timing jitter depend on the correlations among the noise sources involved. The case of each transition's being affected by independent noise sources has been considered in [12] and [13]. The jitter introduced by each stage is assumed to be totally independent of the jitter introduced by other stages, and therefore the total variance of the jitter is given by the sum of the variances introduced at each stage. For ring oscillators with identical stages, the variance will be given by $m\sigma_s^2$, where m is the number of transitions during ΔT and

[1] A more accurate treatment [17] shows that the phase noise does not grow without bound as $f_{\rm off}$ approaches zero (it becomes flat for small values of $f_{\rm off}$). However, this makes no practical difference in this discussion.

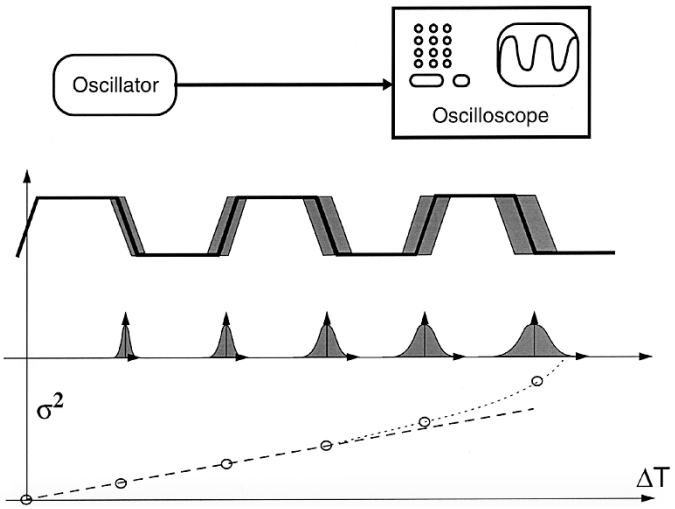

Fig. 3. Clock jitter increasing with time.

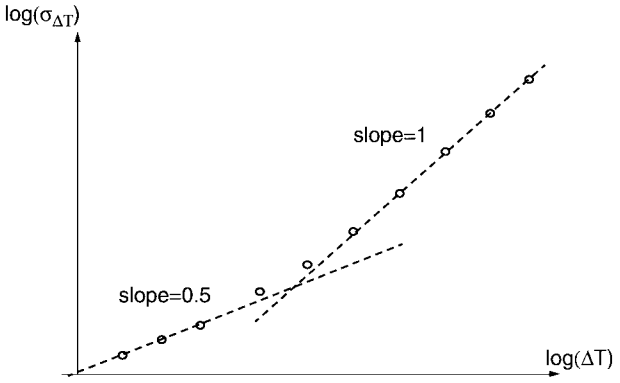

Fig. 4. RMS jitter versus measurement time on a log–log plot.

σ_s^2 is the variance of the uncertainty introduced by one stage during one transition. Noting that m is proportional to ΔT, the standard deviation of the jitter after ΔT seconds is [13]

$$\sigma_{\Delta T} = \kappa\sqrt{\Delta T} \tag{8}$$

where κ is a proportionality constant determined by circuit parameters.

Another instructive special case that is not usually considered is when the noise sources are totally correlated with one another. Substrate and supply noise are examples of such noise sources. Low-frequency noise sources, such as $1/f$ noise, can also result in a correlation between induced jitter on transitions over multiple cycles. In this case, the standard deviations rather than the variances add. Therefore, the standard deviation of the jitter after ΔT seconds is proportional to ΔT

$$\sigma_{\Delta T} = \zeta\Delta T \tag{9}$$

where ζ is another proportionality constant. Noise sources such as thermal noise of devices are usually modeled as uncorrelated, while substrate and supply-noise sources, as well as low-frequency noise, are approximated as partially or fully correlated sources. In practice, both correlated and uncorrelated sources exist in a circuit, and hence a *log–log* plot of the timing jitter $\sigma_{\Delta T}$ versus the measurement delay ΔT for an open-loop oscillator will demonstrate regions with slopes of 1/2 and 1, as shown in Fig. 4.

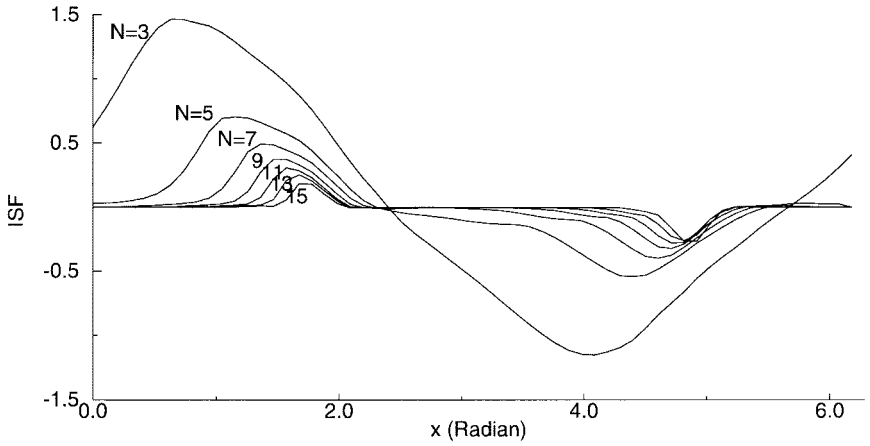

Fig. 5. ISF for ring oscillators of the same frequency with different number of stages.

In most digital applications, it is desirable for $\sigma_{\Delta T}$ to decrease at the same rate as the period T. In practice, we wish to keep constant the ratio of the timing jitter to the period. Therefore, in many applications, phase jitter, defined as

$$\sigma_{\Delta\phi} = 2\pi \frac{\sigma_{\Delta T}}{T} = \omega_0 \sigma_{\Delta T} \tag{10}$$

is a more useful measure.

An expression for $\sigma_{\Delta\phi}$ can be obtained using (5). As shown in Appendix A, for $\Delta T \gg T$ or $\Delta T = nT$ where n is an integer, the phase jitter due to a single white noise source is given by

$$\sigma^2_{\Delta\phi} = \frac{\Gamma^2_{\rm rms} \cdot \overline{i_n^2}/\Delta f}{2q^2_{\max}} \Delta T. \tag{11}$$

Using (10) and (11), the proportionality constant κ in (8) is calculated to be

$$\kappa = \frac{\Gamma_{\rm rms}}{q_{\max}\omega_0} \sqrt{\frac{1}{2}\frac{\overline{i_n^2}}{\Delta f}}. \tag{12}$$

IV. Calculation of the ISF for Ring Oscillators

To calculate phase noise and jitter using (6) and (12), one needs to know the rms value of the ISF. Although one can always find the ISF through simulation, we obtain a closed-form approximate equation for the rms value of the ISF of ring oscillators, which usually makes such simulations unnecessary.

It is instructive to look at the actual ISF of ring oscillators to gain insight into what constitutes a good approximation. Fig. 5 shows the shape of the ISF for a group of single-ended CMOS ring oscillators. The frequency of oscillation is kept constant (through adjustment of channel length), while the number of stages is varied from 3 to 15 (in odd numbers). To calculate the ISF, a narrow current pulse is injected into one of the nodes of the oscillator, and the resulting phase shift is measured a few cycles later in simulation.

As can be seen, increasing the number of stages reduces the peak value of the ISF. The reason is that the transitions of the normalized waveform become faster for larger N. Since the sensitivity during the transition is inversely proportional to the slope, the peak of the ISF drops. It should be noted that only the peak of the ISF is inversely proportional to the slope, and this relation should not be generalized to other points in time. Also, the widths of the lobes of the ISF decrease as N becomes larger, since each transition occupies a smaller fraction of the period. Based on these observations, we approximate the ISF as triangular in shape and with symmetric rising and falling edges, as shown in Fig. 6. The case of nonsymmetric rising and falling edges is considered in Appendix B.

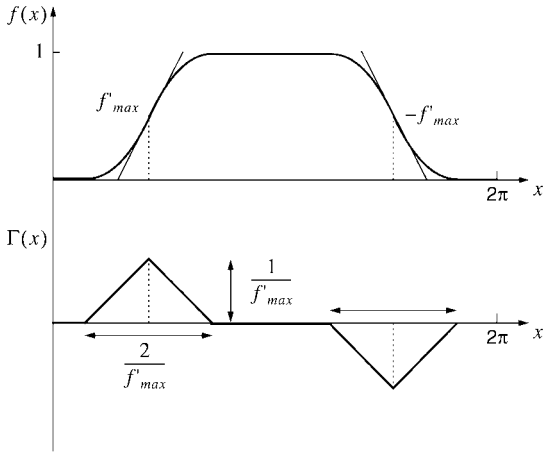

Fig. 6. Approximate waveform and ISF for ring oscillator.

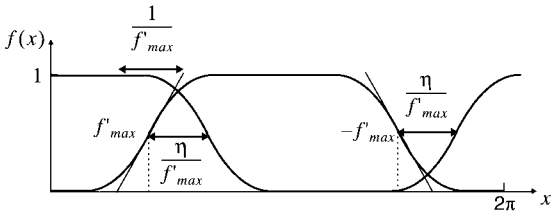

Fig. 7. Relationship between rise time and delay.

The ISF has a maximum of $1/f'_{\max}$, where $f'_{\max}$ is the maximum slope of the normalized waveform f in (1). Also, the width of the triangles is approximately $2/f'_{\max}$, and hence the slopes of the sides of the triangles are ± 1. Therefore, assuming equality of rise and fall times, $\Gamma_{\rm rms}$ can be estimated as

$$\Gamma^2_{\rm rms} = \frac{1}{2\pi}\int_0^{2\pi} \Gamma^2(x)\,dx = \frac{4}{2\pi}\int_0^{1/f'} x^2\,dx = \frac{2}{3\pi}\left(\frac{1}{f'_{\max}}\right)^3. \tag{13}$$

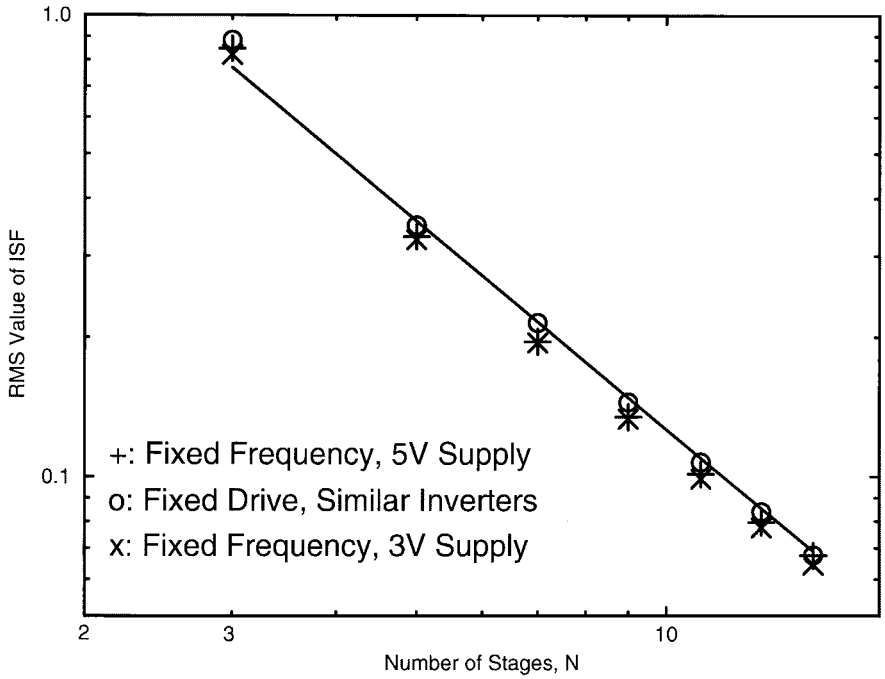

Fig. 8. RMS values of the ISF's for various single-ended ring oscillators versus number of stages.

On the other hand, stage delay is proportional to the rise time

$$\hat{t}_D = \frac{\eta}{f'_{\max}} \tag{14}$$

where $\hat{t}_D$ is the normalized stage delay and η is a proportionality constant, which is typically close to one, as can be seen in Fig. 7.

The period is $2N$ times longer than a single stage delay

$$2\pi = 2N\hat{t}_D = \frac{2N\eta}{f'_{\max}}. \tag{15}$$

Using (13) and (15), the following approximate expression for $\Gamma_{\rm rms}$ is obtained:

$$\Gamma_{\rm rms} = \sqrt{\frac{2\pi^2}{3\eta^3}}\frac{1}{N^{1.5}}. \tag{16}$$

Note that the $1/N^{1.5}$ dependence of $\Gamma_{\rm rms}$ is independent of the value of η. Fig. 8 illustrates $\Gamma_{\rm rms}$ for the ISF shown in Fig. 5 with plus signs on *log–log* axes. The solid line shows the line of $\Gamma_{\rm rms} \approx 4/N^{1.5}$, which is obtained from (16) for $\eta = 0.75$. To verify the generality of (16), we maintain a fixed channel length for all the devices in the inverters while varying the number of stages to allow different frequencies of oscillation. Again, $\Gamma_{\rm rms}$ is calculated, and is shown in Fig. 8 with circles. We also repeat the first experiment with a different supply voltage (3 V as opposed to 5 V), and the result is shown with crosses. As can be seen, the values of $\Gamma_{\rm rms}$ are almost identical for these three cases.

It should not be surprising that $\Gamma_{\rm rms}$ is primarily a function of N because the effect of variations in other parameters, such as $q_{\max}$ and device noise, have already been decoupled from $\Gamma(x)$, and thus the ISF is a unitless, frequency- and amplitude-independent function.

Equation (16) is valid for differential ring oscillators as well, since in its derivation no assumption specific to single-ended oscillators was made. Fig. 9 shows the $\Gamma_{\rm rms}$ for three sets of differential ring oscillators, with a varying number of stages (4–16). The data shown with plus signs correspond to oscillators in which the total power dissipation and the drain voltage swing are kept constant by scaling the tail-current sources and load resistors as N changes. Members of the second set of oscillators have a fixed total power dissipation and fixed load resistors, which result in variable swings and for whom data are shown with circles. The third case is that of a fixed tail current for each stage and constant load resistors, whose data are illustrated using crosses. Again, in spite of the diverse variations of the frequency and other circuit parameters, the $1/N^{1.5}$ dependency of $\Gamma_{\rm rms}$ and its independence from other circuit parameters still holds. In the case of a differential ring oscillator, $\Gamma_{\rm rms} \approx 3/N^{1.5}$, which corresponds to $\eta = 0.9$, is the best fit approximation for $\Gamma_{\rm rms}$. This is shown with the solid line in Fig. 9. A similar result can be obtained for bipolar differential ring oscillators.

Although $\Gamma_{\rm rms}$ decreases as the number of stages increases, one should not prematurely conclude that the phase noise can be reduced using a larger number of stages because the number of noise sources, as well as their magnitudes, also increases for a given total power dissipation and frequency of oscillation.

In the case of asymmetric rising and falling edges, both $\Gamma_{\rm rms}$ and $\Gamma_{\rm dc}$ will change. As shown in Appendix B, the $1/f^3$ corner of the phase-noise spectrum is inversely proportional to the number of stages. Therefore, the $1/f^3$ corner can be reduced either by making the transitions more symmetric in terms of rise and fall times or by increasing the number of stages. Although the former always helps, the latter has other implications on the phase noise in the $1/f^2$ region, as will be shown in the following section.

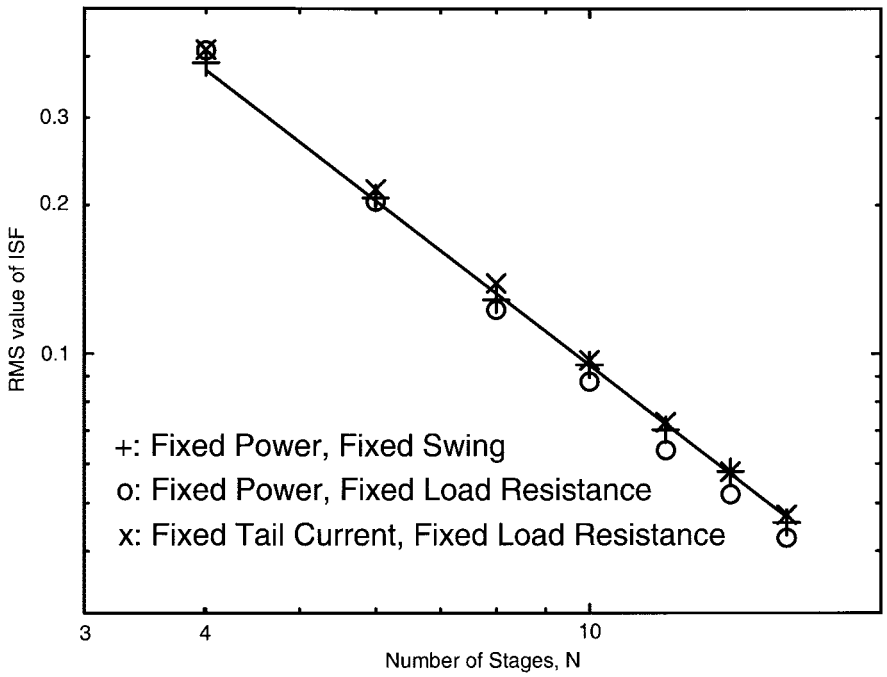

Fig. 9. RMS values of the ISF's for various differential ring oscillators versus number of stages.

V. Expressions for Jitter and Phase Noise in Ring Oscillators

In this section, we derive expressions for the phase noise and jitter of different types of ring oscillators. Throughout this section, we assume that the symmetry criteria required to minimize $\Gamma_{\rm dc}$ (and hence the upconversion of $1/f$ noise) are already met and that the jitter and phase noise of the oscillator are dominated by white noise. For CMOS transistors, the drain current noise spectral density is given by

$$\frac{\overline{i_n^2}}{\Delta f} = 4kT\gamma g_{d0} = 4kT\gamma\mu C_{\rm ox}\frac{W}{L}\Delta V \tag{17}$$

where g_{d0} is the zero-bias drain source conductance, μ is the mobility, $C_{\rm ox}$ is the gate-oxide capacitance per unit area, W and L are the channel width and length of the device, respectively, and ΔV is the gate voltage overdrive. The coefficient γ is 2/3 for long-channel devices in the saturation region and typically two to three times greater for short-channel devices [18]. Equation (17) is valid in both short- and long-channel regimes as long as an appropriate value for γ is used.

A. Single-Ended CMOS Ring Oscillators

We start with a single-ended CMOS ring oscillator with equal-length NMOS and PMOS transistors. Assuming that $V_{\rm TN} = |V_{\rm TP}|$, the maximum total channel noise from NMOS and PMOS devices, when both the input and output are at $V_{\rm DD}/2$, is given by

$$\frac{\overline{i_n^2}}{\Delta f} = \left(\frac{\overline{i_n^2}}{\Delta}\right)_N + \left(\frac{\overline{i_n^2}}{\Delta f}\right)_N = 4kT\gamma\mu_{\rm eff}C_{\rm ox}\frac{W_{\rm eff}}{L}\Delta V \tag{18}$$

where

$$W_{\rm eff} = W_n + W_p \tag{19}$$

and

$$\mu_{\rm eff} = \frac{\mu_n W_n + \mu_p W_p}{W_n + W_p} \tag{20}$$

and ΔV is the gate overdrive in the middle of transition, i.e., $\Delta V = (V_{\rm DD}/2) - V_T$.

During one period, each node is charged to $q_{\max}$ and then discharged to zero. In an N-stage single-ended ring oscillator, the power dissipation associated with this process is $Nq_{\max}V_{\rm DD}f_0$. However, during the transitions, some extra current, known as crowbar current, is drawn from the supply, which does not contribute to charging and discharging the capacitors and goes directly from supply to ground through both transistors. In a symmetric ring oscillator, these two components are approximately equal, and their difference will depend on the ratio of the rise time and stage delay. Therefore, the total power dissipation is approximately given by

$$P = 2\eta N V_{\rm DD} q_{\max} f_0. \tag{21}$$

Assuming $\mu_n W_n = \mu_p W_p$ to make the waveforms symmetric to the first order, we have

$$f_0 = \frac{1}{2Nt_D} = \frac{1}{\eta N(t_r + t_f)} \approx \frac{\mu_{\rm eff}W_{\rm eff}C_{\rm ox}\Delta V^2}{8\eta N L q_{\max}} \tag{22}$$

where t_D is the delay of each stage and t_r and t_f are the rise and fall time, respectively, associated with the maximum slope during a transition.

Assuming that the thermal noise sources of the different devices are uncorrelated, and assuming that the waveforms (and hence the ISF) of all the nodes are the same except for a phase shift, the total phase noise due to all N noise sources is

N times the value given by (6). Taking only these inevitable noise sources into account, (6), (16), (18), (21), and (22) result in the following expressions for phase noise and jitter:

$$L\{\Delta f\} \approx \frac{8}{3\eta} \cdot \frac{kT}{P} \cdot \frac{V_{\rm DD}}{V_{\rm char}} \cdot \frac{f_0^2}{\Delta f^2} \tag{23}$$

$$\kappa \approx \sqrt{\frac{8}{3\eta}} \cdot \sqrt{\frac{kT}{P} \cdot \frac{V_{\rm DD}}{V_{\rm char}}} \tag{24}$$

where $V_{\rm char}$ is the *characteristic voltage* of the device. For long-channel mode of operation, it is defined as $V_{\rm char} = \Delta V/\gamma$. Any extra disturbance, such as substrate and supply noise, or noise contributed by extra circuitry or asymmetry in the waveform will result in a larger number than (23) and (24). Note that lowering threshold voltages reduces the phase noise, in agreement with [12]. Therefore, the minimum achievable phase noise and jitter for a single-ended CMOS ring oscillator, assuming that all symmetry criteria are met, occurs for zero threshold voltage

$$L\{\Delta f\} > \frac{16\gamma}{3\eta} \cdot \frac{kT}{P} \cdot \frac{f_0^2}{\Delta f^2} \tag{25}$$

$$\kappa > \sqrt{\frac{16\gamma}{3\eta}} \cdot \sqrt{\frac{kT}{P}}. \tag{26}$$

As can be seen, the minimum phase noise is inversely proportional to the power dissipation and grows quadratically with the oscillation frequency. Further, note the lack of dependence on the number of stages (for a given power dissipation and oscillation frequency). Evidently, the increase in the number of noise sources (and in the maximum power due to the higher transition currents required to run at the same frequency) essentially cancels the effect of decreasing $\Gamma_{\rm rms}$ as N increases, leading to no net dependence of phase noise on N. This somewhat surprising result may explain the confusion that exists regarding the optimum N, since there is not a strong dependence on the number of stages for single-ended CMOS ring oscillators. Note that (25) and (26) establish the lower bound and therefore should not be used to calculate the phase noise and jitter of an arbitrary oscillator, for which (6) and (12) should be used, respectively.

We may carry out a similar calculation for the short-channel case. For such devices, the drain current may be expressed as

$$I_D = \frac{\mu C_{\rm ox}}{2} W E_c \Delta V \tag{27}$$

where E_c is the critical electric field and is defined as the value of electric field resulting in half the carrier velocity expected from low field mobility. Combining (17) with (27), we obtain the following expression for the drain current noise of a MOS device in short channel:

$$\frac{\overline{i_n^2}}{\Delta f} = 8kT\frac{\gamma I_D}{E_C L}. \tag{28}$$

The frequency of oscillation can be approximated by

$$f_0 = \frac{1}{2Nt_D} = \frac{1}{\eta N(t_r + t_f)} = \frac{\mu_{\rm eff} W_{\rm eff} C_{\rm ox} \Delta V^2}{8\eta N L q_{\max}}. \tag{29}$$

Using (28) and (29), we obtain the same expressions for phase noise and jitter as given by (23) and (24), except for a new $V_{\rm char}$

$$V_{\rm char} = \frac{E_c L}{\gamma} \tag{30}$$

which results in a larger phase noise and jitter than the long-channel case by a factor of $\gamma\Delta V/E_c L$. Again, note the absence of any dependency on the number of stages.

B. Differential CMOS Ring Oscillators

Now consider a differential MOS ring oscillator with resistive load. The total power dissipation is

$$P = NI_{\rm tail}V_{\rm DD} \tag{31}$$

where N is the number of stages, $I_{\rm tail}$ is the tail bias current of the differential pair, and $V_{\rm DD}$ is the supply voltage. The frequency of oscillation can be approximated by

$$f_0 = \frac{1}{2Nt_D} \approx \frac{1}{2\eta N t_r} \approx \frac{I_{\rm tail}}{2\eta N q_{\max}}. \tag{32}$$

Surprisingly, tail-current source noise in the vicinity of f_0 does not affect the phase noise. Rather, its low-frequency noise as well as its noise in the vicinity of *even* multiples of the oscillation frequency affect the phase noise. Tail noise in the vicinity of even harmonics can be significantly reduced by a variety of means, such as with a series inductor or a parallel capacitor. As before, the effect of low-frequency noise can be minimized by exploiting symmetry. Therefore, only the noise of the differential transistors and the load are taken into account. The total current noise on each single-ended node is given by

$$\begin{aligned}\frac{\overline{i_n^2}}{\Delta f} &= \left(\frac{\overline{i_n^2}}{\Delta f}\right)_N + \left(\frac{\overline{i_n^2}}{\Delta f}\right)_{\rm Load} \\ &= 4kTI_{\rm tail}\left(\frac{1}{V_{\rm char}} + \frac{1}{R_L I_{\rm tail}}\right)\end{aligned} \tag{33}$$

where R_L is the load resistor, $V_{\rm char} = (V_{\rm GS} - V_T)/\gamma$ for a balanced stage in the long-channel limit and $V_{\rm char} = E_c L/\gamma$ in the short-channel regime. The phase noise and jitter due to all $2N$ noise sources is $2N$ times the value given by (6) and (12). Using (16), the expression for the phase noise of the differential MOS ring oscillator is

$$L_{\min}\{\Delta f\} = \frac{8}{3\eta} \cdot N \cdot \frac{kT}{P} \cdot \left(\frac{V_{\rm DD}}{V_{\rm char}} + \frac{V_{\rm DD}}{R_L I_{\rm tail}}\right) \cdot \frac{f_0^2}{\Delta f^2} \tag{34}$$

and is given by

$$\kappa_{\min} = \sqrt{\frac{8}{3\eta}} \cdot \sqrt{N \cdot \frac{kT}{P} \cdot \left(\frac{V_{\rm DD}}{V_{\rm char}} + \frac{V_{\rm DD}}{R_L I_{\rm tail}}\right)}. \tag{35}$$

Equations (34) and (35) are valid in both long- and short-channel regimes of operation with the right choice of $V_{\rm char}$.

Note that, in contrast with the single-ended ring oscillator, a differential oscillator does exhibit a phase noise and jitter dependency on the number of stages, with the phase noise

degrading as the number of stages increases for a given frequency and power dissipation. This result may be understood as a consequence of the necessary reduction in the charge swing that is required to accommodate a constant frequency of oscillation at a fixed power level as N increases. At the same time, increasing the number of stages at a fixed total power dissipation demands a proportional reduction of tail-current sources, which will reduce the swing, and hence $q_{\max}$, by a factor of $1/N^2$.

C. Bipolar Differential Ring Oscillator

A similar approach allows us to derive the corresponding results for a bipolar differential ring oscillator. In this case, the power dissipation is given by (31) and the oscillation frequency by (32). The total noise current is given by the sum of collector shot noise and load resistor noise

$$\frac{\overline{i_n^2}}{\Delta f} = 2q_e I_C + \frac{4kT}{R} = 4kTI_{\text{tail}}\left(\frac{1}{V_{\text{char}}} + \frac{1}{R_L I_{\text{tail}}}\right) \quad (36)$$

where q_e is the electron charge, $I_C = I_{\text{tail}}/2$ is the collector current during the transition, and $V_{\text{char}} = 4kT/q_e$. Using these relations, the phase noise and jitter of a bipolar ring oscillator are again given by (34) and (35) with the appropriate choice of V_{char}.

VI. Other Noise Sources

Other noise sources, such as tail-current source noise in a differential structure, or substrate and supply noise sources, may play an important role in the jitter and phase noise of ring oscillators. The low-frequency noise of the tail-current source affects phase noise if the symmetry criteria mentioned in Section II are not met by each half circuit. In such cases, the ISF for the tail-current source has a large dc value, which increases the upconversion of low-frequency noise to phase noise. This upconversion is particularly prominent if the tail device has a large $1/f$ noise corner.

Substrate and supply noise are among other important sources of noise. There are two major differences between these noise sources and internal device noise. First, the power spectral density of these sources is usually nonwhite and often demonstrates strong peaks at various frequencies. Even more important is that the substrate and supply noise on different nodes of the ring oscillator have a very strong correlation. This property changes the response of the oscillator to these sources.

To understand the effect of this correlation, let us consider the special case of having equal noise sources on all the nodes of the oscillator. If all the inverters in the oscillator are the same, the ISF for different nodes will only differ in phase by multiples of $2\pi/N$, as shown in Fig. 10. Therefore, the total phase due to all the sources is given by superposition of (5)

$$\begin{aligned}\phi(t) &= \frac{1}{q_{\max}}\sum_{n=0}^{N-1}\int_{-\infty}^{t} i(\tau)\Gamma\left(\omega_0\tau + \frac{2\pi n}{N}\right)d\tau \\ &= \frac{1}{q_{\max}}\int_{-\infty}^{t} i(\tau)\left[\sum_{n=0}^{N-1}\Gamma\left(\omega_0\tau + \frac{2\pi n}{N}\right)\right]d\tau. \quad (37)\end{aligned}$$

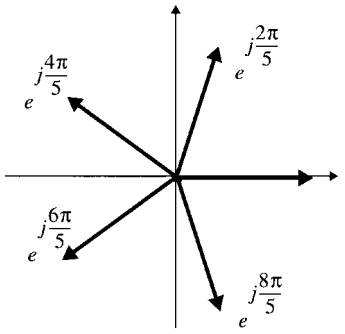

Fig. 10. Phasors for noise contributions from each source.

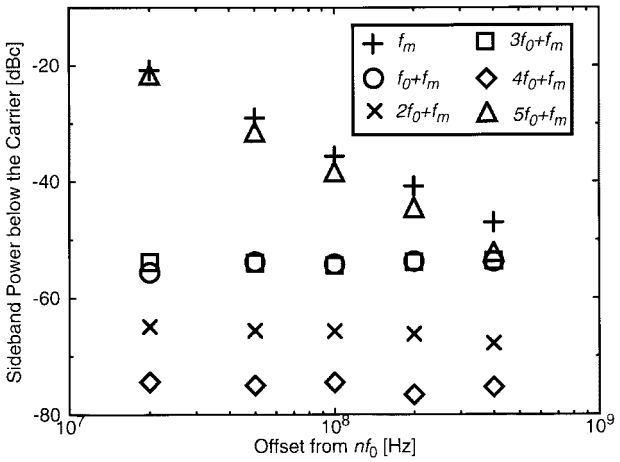

Fig. 11. Sideband power below carrier for equal sources on all five nodes at $nf_0 + f_m$.

Expanding the term in brackets in a Fourier series, we can show that it is zero except at dc and multiples of $N\omega_0$, i.e.,

$$\phi(t) = \frac{N}{q_{\max}}\sum_{n=0}^{\infty} c_{(nN)}\int_{-\infty}^{t} i(\tau)\cos(nN\omega_0\tau)\,d\tau \quad (38)$$

where c_i is the ith Fourier coefficient of the ISF. Equation (38) means that for identical sources, only noise in the vicinity of integer multiples of $N\omega_0$ affects the phase.

To verify this effect, sinusoidal currents with an amplitude of 10 μA were injected into all five nodes of the five-stage ring oscillator of Fig. 1 at different offsets from integer multiples of the frequency of oscillation, and the induced sidebands were measured. The measured sideband power with respect to the carrier is plotted in Fig. 11.

As can be seen in Fig. 11, only injection at low frequency and in the vicinity of the fifth harmonic are integrated, and show a -20 dB/dec slope. The effect of injection in the vicinity of harmonics that are not integer multiples of N is much smaller than at the integer ones. Ideally, there should be no sideband induced by the injection in the vicinity of harmonics that are not integer multiples of N; however, as can be seen in Fig. 11, there is some sideband power due to the amplitude response.

Low-frequency noise can also result in correlation between uncertainties introduced during different cycles, as its value does not change significantly over a small number of periods.

Therefore, the uncertainties add up in amplitude rather than power, resulting in a region with a slope of one in the *log–log* plot of jitter even in the absence of external noise sources such as substrate and supply noise.

VII. Design Implications

One can use (23) and (34) to compare the phase-noise performance of single-ended and differential MOS ring oscillators. As can be seen for N stages, the phase noise of the differential ring oscillator is approximately $N[1 + V_{\rm char}/(R_L I_{\rm tail})]$ times larger than the phase noise of a single-ended oscillator of equal $N, P_{\rm tot}$ and f_0. Since the minimum N for a regular ring oscillator is three, even a properly designed differential CMOS ring oscillator underperforms its single-ended counterpart, especially for a larger number of stages. This difference is even more pronounced if proper precautions to reduce the noise of the tail current are not taken. However, the differential ring oscillator may still be preferred in IC's because of the lower sensitivity to substrate and supply noise, as well as lower noise injection into other circuits on the same chip. The decision to use differential versus single-ended ring oscillators should be based on both of these considerations.

The common-mode sensitivity problem in a single-ended ring oscillator can be mitigated to some extent by using two identical ring oscillators laid out close to each other that oscillate out of phase because of small coupling inverters [19]. Single-ended configurations may be used in a less noisy environment to achieve better phase-noise performance for a given power dissipation.

As shown in Appendix B, asymmetry of the rising and falling edges degrades phase noise and jitter by increasing the $1/f^3$ corner frequency. Thus, every effort should be taken to make the rising and falling edges symmetric. By properly adjusting the symmetry properties, one can suppress or even eliminate low-frequency-noise upconversion [16]. As shown in [16], differential symmetry is insufficient, and the symmetry of each half circuit is important. One practical method to achieve this symmetry is to use more linear loads, such as resistors or linearized MOS devices. This method reduces the $1/f$ noise upconversion and substrate and supply coupling [20]. Another revealing implication, shown in Appendix A, is the reduction of the $1/f^3$ corner frequency as N increases. Hence for a process with large $1/f$ noise, a larger number of stages may be helpful.

One question that frequently arises in the design of ring oscillators is the optimum number of stages for minimum jitter and phase noise. As seen in (23), for single-ended oscillators, the phase noise and jitter in the $1/f^2$ region is not a strong function of the number of stages for single-ended CMOS ring oscillators. However, if the symmetry criteria are not well satisfied and/or the process has a large $1/f$ noise, a larger N will reduce the jitter. In general, the choice of the number of stages must be made on the basis of several design criteria, such as $1/f$ noise effect, the desired maximum frequency of oscillation, and the influence of external noise sources, such as supply and substrate noise, that may not scale with N.

The jitter and phase noise behavior are different for differential ring oscillators. As (34) suggests, jitter and phase noise increase with an increasing number of stages. Hence if the $1/f$ noise corner is not large, and/or proper symmetry measures have been taken, the minimum number of stages (three or four) should be used to give the best performance. This recommendation holds even if the power dissipation is not a primary issue. It is not fair to argue that burning more power in a larger number of stages allows the achievement of better phase noise, since dissipating the same total power in a smaller number of stages results in better jitter/phase noise as long as it is possible to maximize the total charge swing.

Another insight one can obtain from (34) and (35) is that the jitter of a MOS differential ring oscillator at a given $V_{\rm DD}, P, N$, and f_0 is smaller than that of a differential bipolar ring oscillator, at least for today's range of circuit and process parameters. As we go to shorter channel lengths, the characteristic voltage for the MOS devices given by (30) becomes smaller, and thus phase noise degrades with scaling. Bipolar ring oscillators do not suffer from this problem.

LC oscillators generally have better phase noise and jitter compared to ring oscillators for two reasons. First, a ring oscillator stores a certain amount of energy in the capacitors during every cycle and then dissipates all the stored energy during the same cycle, while an LC resonator dissipates only $2\pi/Q$ of the total energy stored during one cycle. Thus, for a given power dissipation in steady state, a ring oscillator suffers from a smaller maximum charge swing $q_{\rm max}$. Second, in a ring oscillator, the device noise is maximum during the transitions, which is the time where the sensitivity, and hence the ISF, is the largest [16].

VIII. Experimental Results

The phase-noise measurements in this section were performed using three different systems: an HP 8563E spectrum analyzer with phase-noise measurement capability, an RDL NTS-1000A phase-noise measurement system, and an HP E5500 phase-noise measurement system. The jitter measurements were performed using a Tektronix CSA 803A communication signal analyzer.

Tables I–III summarize the phase-noise measurements. All the reported phase-noise values are at a 1-MHz offset from the carrier, chosen to achieve the largest dynamic range in the measurement. Table I shows the measurement results for three different inverter-chain ring oscillators. These oscillators are made of the CMOS inverters shown in Fig. 12(a), with no frequency tuning mechanism. The output is taken from one node of the ring through a few stages of tapered inverters. Oscillators number 1 and 2 are fabricated in a 2-μm, 5-V CMOS process, and oscillator number 3 is fabricated in a 0.25-μm, 2.5-V process. The second column shows the number of stages in each of the oscillators. The W/L ratios of the NMOS and PMOS devices, as well as the supply voltages, the total measured supply currents, and the frequencies of oscillation are shown next. The phase-noise prediction using (23) and (6), together with the measured phase noise, are shown in the last three columns.

TABLE I
INVERTER-CHAIN RING OSCILLATORS

Index	N	*NMOS W/L* µm/µm	*PMOS W/L* µm/µm	V_{DD}	I_{sup} *mA*	f_o	Pred. (23) *dBc/Hz*	Pred. (6) *dBc/Hz*	Meas. PN *dBc/Hz*
1	5	3/2	5/2	5.0	0.3	232MHz	-119.9	-117.7	-118.5
2	11	4/2	6/2	5.0	0.5	115MHz	-127.2	-126.4	-126.0
3	19	10/0.25	20/0.25	2.5	10	1.33GHz	-111.8	-113.0	-111.5

TABLE II
CURRENT-STARVED INVERTER-CHAIN RING OSCILLATORS

Index	N	*Ninv W/L* µm/µm	*Pinv W/L* µm/µm	*Ntail W/L* µm/µm	*Ptail W/L* µm/µm	I_{sup} *mA*	f_o *MHz*	Pred. (23) *dBc/Hz*	Pred. (6) *dBc/Hz*	Meas. PN *dBc/Hz*
4	3	35/ 0.53	70/ 0.53	28/ 0.53	56/ 0.53	2.34	751	-113.8	-116.6	-114.0
5	5	21/ 0.39	42/ 0.39	23/ 0.39	46/ 0.39	2.51	850	-111.7	-111.9	-112.6
6	7	14/ 0.36	28/ 0.36	36.8/ 0.36	73.5/ 0.36	2.49	931	-110.5	-110.4	-111.7
7	9	12.6/ 0.32	25.2/ 0.32	28/ 0.32	56/ 0.32	2.73	932	-110.4	-113.5	-112.5
8	11	10.5/ 0.32	21/ 0.32	146/ 0.32	291/ 0.32	2.65	869	-110.9	-110.1	-112.2
9	15	9.1/ 0.28	18.2/ 0.28	146/ 0.28	291/ 0.28	2.8	929	-110.0	-110.7	-112.3
10	17	7.4/ 0.25	12.6/ 0.25	25.2/ 0.28	50.4/ 0.28	3.8	898	-111.2	-109.4	-112.0
11	19	6.3/ 0.25	12.6/ 0.25	56/ 0.25	112/ 0.25	3.9	959	-110.6	-110.1	-110.9

As an illustrative example, we will show the details of phase-noise calculations for oscillator number 3. Using (16) to calculate $\Gamma_{\rm rms}$, the phase noise can be obtained from (6). We calculate the noise power when the stage is halfway through a transition. At this point, the drain current is simulated to be 3.47 mA. An E_c of 4×10^6 V/m and a γ of 2.5 is used in (28) to obtain a noise power of $\overline{i^2}/\Delta f = 2.87 \times 10^{-22}\,\mathrm{A}^2/\mathrm{Hz}$. The total capacitance on each node is $C_{\rm total} = 71.8$ fF, and hence $q_{\rm max} = 179.5$ fC. There is one such noise source on each node; therefore, the phase noise is N times the value given by (6), which results in $\mathcal{L}\{1\,\mathrm{MHz}\} = -113.0$ dBc/Hz.

Table II summarizes the data obtained for current-starved ring oscillators with the cell structure shown in Fig. 12(b), all implemented in the same 0.25-μm, 2.5-V process. Ring oscillators with a different number of stages were designed with roughly constant oscillation frequency and total power dissipation. Frequency adjustment is achieved by changing the channel length, while total power dissipation control is performed by changing device width. The W/L ratios of the inverter and the tail NMOS and PMOS devices are shown in Table II. The node $Nbias$ is kept at $V_{\rm DD}$, while node $Pbias$ is at 0 V. The measured total current dissipation and the frequency of oscillation can be found in columns 7 and 8. Phase-noise calculations based on (23) and (6) are in good agreement with the measured results. The die photo of the chip containing these oscillators is shown in Fig. 13. The slightly superior phase noise of the three-stage ring oscillator (number 4) can be attributed to lower oscillation frequency and longer channel length (and hence smaller γ).

Table III summarizes the results obtained for differential ring oscillators of various sizes and lengths with the inverter topology shown in Fig. 12(c), covering a large span of frequencies up to 5.5 GHz. All these ring oscillators are implemented in the same 0.25-μm, 2.5-V process, and all the oscillators, except the one marked with N/A, have the tuning circuit shown. The resistors are implemented using an unsilicided polysilicon layer. The main reason to use poly resistors is to reduce $1/f$ noise upconversion by making the waveform on each node closer to the step response of an RC network, which is more symmetrical. The value of these load resistors and the W/L ratios of the differential pair are shown in Table III. A fixed 2.5-V power supply is used, resulting in different total power dissipations. As before, the measured phase noise is in good agreement with the predicted phase noise using (34) and (6). The die photo of oscillator number 26 can be found in Fig. 14.

To illustrate further how one obtains the phase-noise predictions shown in Table III, we elaborate on the phase-noise

TABLE III
DIFFERENTIAL RING OSCILLATORS

Index	N	W/L µm/µm	R_L Ω	I_{tail} mA	P_{tot} mW	f_{max}	Tuning range	Pred. (34) dBc/Hz	Pred. (6) dBc/Hz	Meas. PN dBc/Hz
12	4	4.2/0.25	2k	1	10	2.81GHz	34%	-95.4	-95.5	-95.2
13	4	8.4/0.25	1k	2	20	4.47GHz	42%	-95.1	-94.0	-94.3
14	4	16.8/0.25	500	4	40	3.89GHz	44%	-98.5	-97.2	-97.4
15	4	33.6/0.25	250	8	80	5.43GHz	25%	-98.7	-99.6	-98.5
16	4	8.4/0.25	2k	1	10	2.87GHz	37%	-95.2	-96.6	-93.8
17	4	16.8/0.25	1k	2	20	3.39GHz	45%	-96.7	-97.9	-96.8
18	4	33.6/0.25	500	4	40	5.33GHz	32%	-95.8	-97.2	-95.3
19	4	16.8/0.25	2k	1	10	1.75GHz	73%	-99.5	-97.5	-95.2
20	4	33.6/0.25	1k	2	20	2.24GHz	58%	-100.3	-100.3	-99.0
21	4	33.6/0.25	2k	1	10	1.27GHz	67%	-104.4	-101.8	-100.2
22	4	67.2/0.25	1k	2	20	1.19GHz	76%	-105.8	-102.6	-100.2
23	4	33.6/0.25	2k	1	10	1.53GHz	N/A	-100.6	-98.9	-97.3
24	6	13.4/0.25	3k	0.67	10	859MHz	58%	-103.9	-106.0	-104.3
25	8	6.7/0.25	4k	0.5	10	731MHz	74%	-104.1	-106.3	-106.2
26	12	4.2/0.25	6k	0.33	10	447MHz	52%	-106.6	-110.4	-109.5

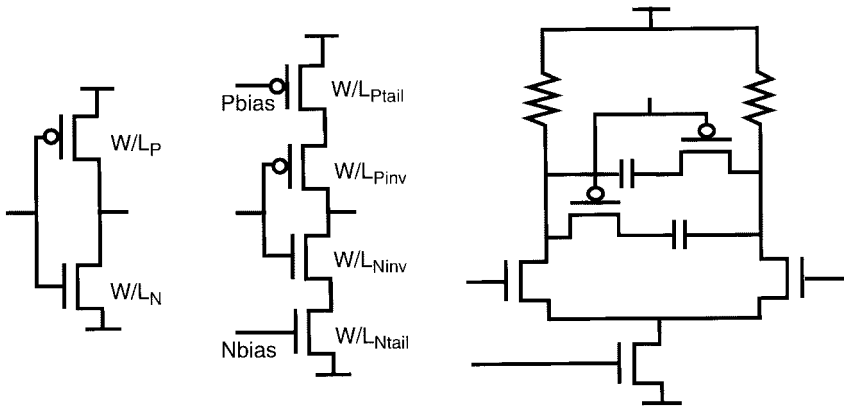

Fig. 12. Inverter stages for (a) inverter-chain ring oscillators, (b) current-starved inverter-chain ring oscillators, and (c) differential ring oscillators.

calculations for oscillator number 12. The noise current due to one of differential pair NMOS devices is given by (28). The total capacitance on each node in the balanced case is $C_{\text{total}} = 41.6$ fF, and the simulated voltage swing is 1.208 V; therefore, $q_{\max} = 50.3$ fC. In the balanced case, this current is half of the tail current, i.e., $I_D = 0.5$ mA, and therefore the noise current of the NMOS device has a single-sideband spectral density of $\overline{i^2}/\Delta f = 4.14\times10^{-23}\,\text{A}^2/\text{Hz}$. The thermal noise due to the load resistor is $\overline{i^2}/\Delta f = 8.28\times10^{-24}\,\text{A}^2/\text{Hz}$; therefore, the total current noise density is given by $\overline{i^2}/\Delta f = 4.97 \times 10^{-23}\,\text{A}^2/\text{Hz}$. For a differential ring oscillator with N stages, there is one such noise source on each node; therefore, the phase noise is $2N$ times the value given by (6), which results in $\mathcal{L}\{1\,\text{MHz}\} = -95.5\,\text{dBc/Hz}$. The total power dissipation is $NV_{\text{DD}}I_{\text{tail}} = 10$ mW, and $R_L = 2\,\text{k}\Omega$. Therefore, with an η of 0.9, (34) predicts a phase noise of $\mathcal{L}\{1\,\text{MHz}\} = -95.4\,\text{dBc/Hz}$.

Timing jitter for oscillator number 12 can be measured using the setup shown in Fig. 15. The oscillator output is divided into two equal-power outputs using a power splitter. The CSA 803A is not capable of showing the edge it uses to trigger, as there is a 21-ns minimum delay between the triggering transition and the first acquired sample. To be able to look at the triggering edge and perhaps the edges before that, a delay line of approximately 25 ns is inserted in the signal path in front of the sampling head. This way, one may look at the exact edge used to trigger the signal. If the sampling head and the power splitter were noiseless, this edge would show no jitter. However, the power splitter and the sampling head introduce noise onto the signal, which cannot be easily

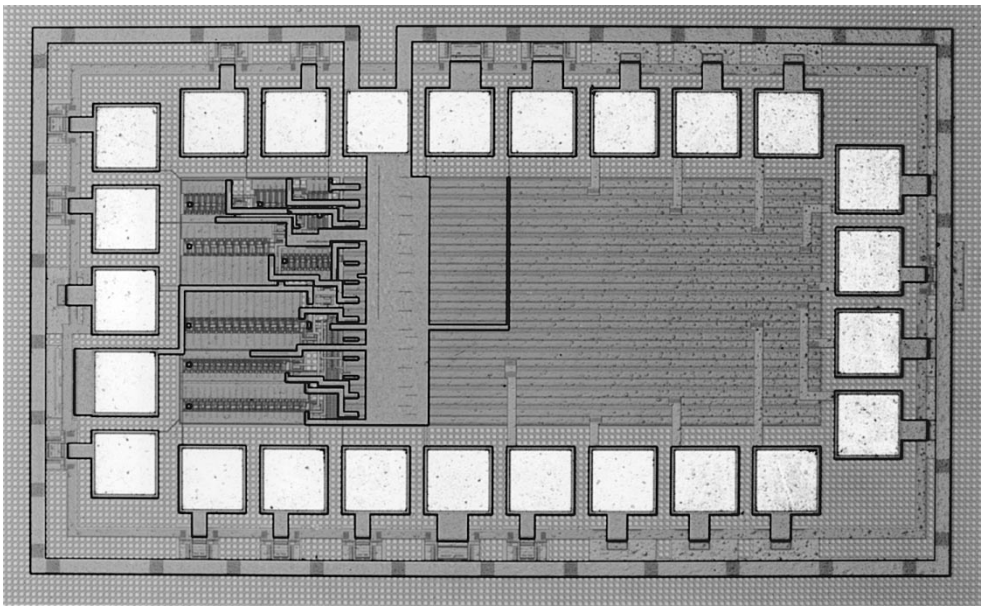

Fig. 13. Die photograph of the current-starved single-ended oscillators.

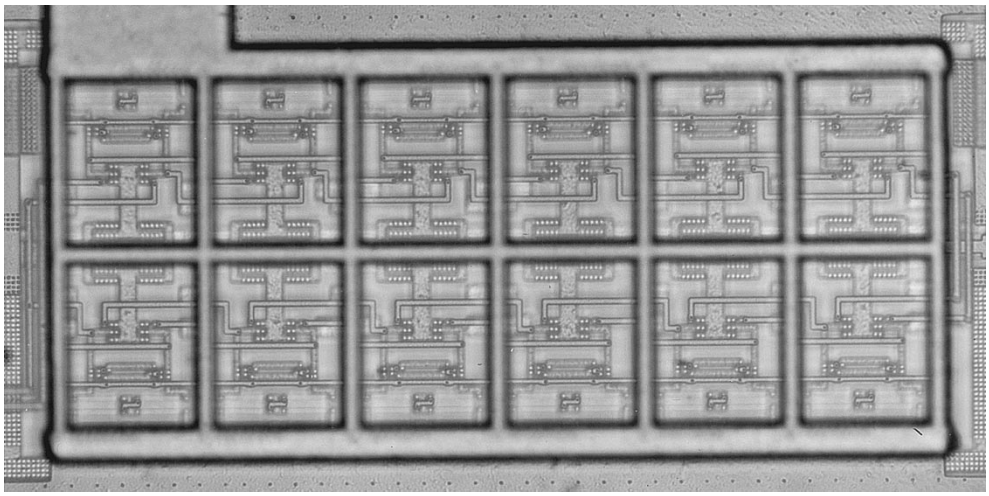

Fig. 14. Die photograph of the 12-stage differential ring oscillator.

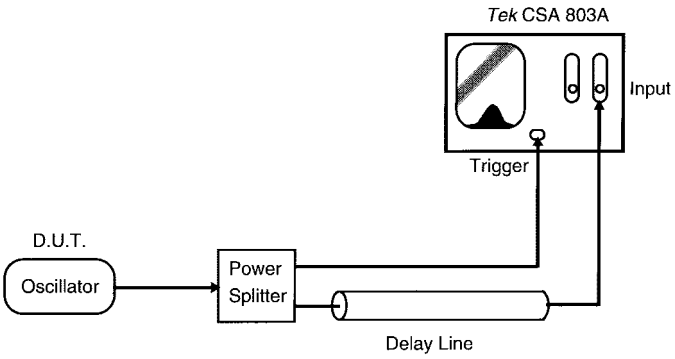

Fig. 15. Timing jitter measurement setup using CSA803A.

distinguished from the device under test (DUT)'s jitter. This extra jitter can be directly measured by looking at the jitter on the triggering edge. This edge can be readily identified since it has lower rms jitter than the transitions before and after it. The effect of this excess jitter should be subtracted from the jitter due to the DUT. Assuming no correlation between the jitter of the DUT and the sampling head, the equivalent jitter due to the DUT can be estimated by

$$\sigma_{\Delta T,\text{eff}} = \sqrt{\sigma^2_{\Delta T,\text{meas}} - \sigma^2_{\Delta T,\text{min}}} \tag{39}$$

where $\sigma_{\Delta T,\text{eff}}$ is the effective rms timing jitter, $\sigma_{\Delta T,\text{meas}}$ is the measured rms jitter at a delay ΔT after the triggering edge, and $\sigma_{\Delta T,\text{min}}$ is the jitter on the triggering edge.

Fig. 16 shows the rms jitter versus the measurement delay for oscillator number 12 on a *log–log* plot. The best fit κ for the data shown in Fig. 16 is $\kappa = 6.18 \times 10^{-9}\sqrt{s}$. Equations (12) and (35) result in $\kappa = 5.95 \times 10^{-9}\sqrt{s}$ and $\kappa = 6.07 \times 10^{-9}\sqrt{s}$, respectively. The region of the jitter plot with the slope of one can be attributed to the $1/f$ noise of the devices, as discussed at the end of Section VI.

In a separate experiment, the phase noise of oscillator number 7 is measured for different values of $Nbias$ and

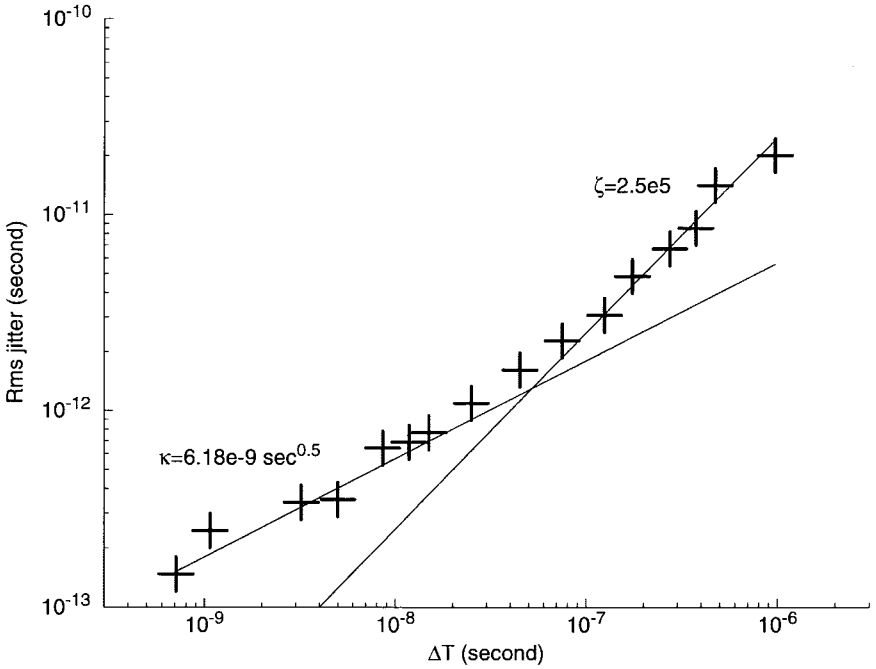

Fig. 16. RMS jitter versus measurement interval for the four-stage, 2.8-GHz differential ring oscillator (oscillator number 12).

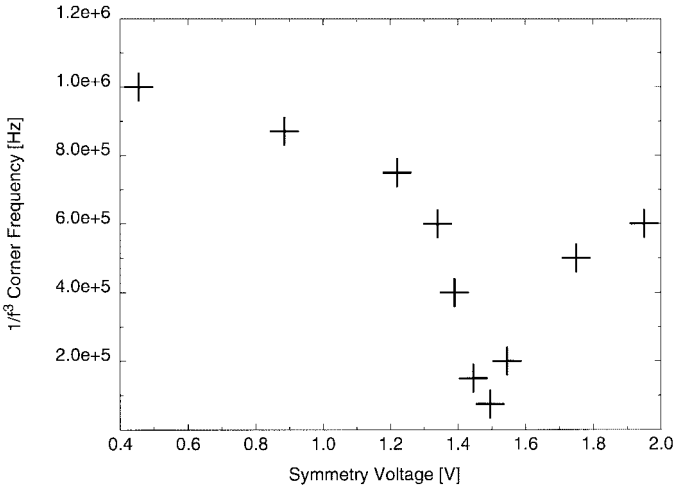

Fig. 17. Phase noise versus symmetry voltage for oscillator number 7.

$PBias$. These bias voltages are chosen in such a way as to keep a constant oscillation frequency while changing only the ratio of rise time to fall time. The $1/f^3$ corner of the phase noise is measured for different ratios of the pullup and pulldown currents while keeping the frequency constant. One can observe a sharp reduction in the corner frequency at the point of symmetry in Fig. 17.

IX. Conclusion

An analysis of the jitter and phase noise of single-ended and differential ring oscillators was presented. The general noise model, based on the ISF, was applied to the case of ring oscillators, resulting in a closed-form expression for the phase noise and jitter of ring oscillators [(6), (23), (34)]. The model was used to perform a parallel analysis of jitter and phase noise for ring oscillators. The effect of the number of stages on the phase noise and jitter at a given total power dissipation and frequency of oscillation was shown for single-ended and differential ring oscillators using the general expression for the rms value of the ISF. The upconversion of low-frequency $1/f$ was analyzed showing the effect of waveform asymmetry and the number of stages. New design insights arising from this approach were introduced, and good agreement between theory and measurements was obtained.

Appendix A
Relationship Between Jitter and Phase Noise

The phase jitter is

$$\sigma^2_{\Delta\phi} = E\{\Delta\phi^2\} = E\{[\phi(t+\Delta T) - \phi(t)]^2\} \tag{40}$$

where

$$\Delta\phi = \int_0^{\Delta T} \frac{\Gamma(\omega_0\tau)}{q_{\max}} i(\tau)\, d\tau. \tag{41}$$

Therefore

$$\sigma^2_{\Delta\phi} = \frac{1}{q^2_{\max}} \int_0^{\Delta T}\int_0^{\Delta T} \Gamma(\omega_0\tau_1)\Gamma(\omega_0\tau_2) \cdot E[i(\tau_1)i(\tau_2)]\, d\tau_1\, d\tau_2. \tag{42}$$

For a white-noise current source, the autocorrelation function is $R_{ii}(t_1,t_2) = (1/2)(\overline{i_n^2}/\Delta f)\delta(t_1 - t_2)$; therefore

$$\sigma^2_{\Delta\phi} = \frac{1}{2}\frac{\overline{i_n^2}/\Delta f}{q^2_{\max}} \int_0^{\Delta T} \Gamma^2(\omega_0\tau)\, d\tau \tag{43}$$

which is

$$\sigma^2_{\Delta\phi} = \frac{1}{2}\frac{\overline{i_n^2}/\Delta f}{q^2_{\max}}\Gamma^2_{\rm rms}\Delta T \quad \text{for} \quad \begin{matrix}\Delta T \gg T \\ \text{or} \\ \Delta T = mT.\end{matrix} \tag{44}$$

Analog and digital designers prefer using phase noise and timing jitter, respectively. The relationship between these two parameters can be obtained by noting that timing jitter is the standard deviation of the timing uncertainty

$$\sigma^2_{\Delta\phi} = \frac{1}{\omega_0^2} E\{[\phi(t+\Delta T) - \phi(t)]^2\} = \frac{E[\phi^2(t)]}{\omega_0^2} + \frac{[\phi^2(t+\Delta T)]}{\omega_0^2} - \frac{E[\phi(t)\phi(t+\Delta T)]}{\omega_0^2} \tag{45}$$

where $E[\cdot]$ represents the expected value. Since the autocorrelation function of $\phi(t), R_\phi(\Delta T)$, is defined as

$$R_\phi(\tau) = E[\phi(t)\phi(t+\Delta T)] \tag{46}$$

the timing jitter in (45) can be written as

$$\sigma^2_{\Delta\phi} = \frac{2}{\omega_0^2}[R_\phi(0) - R_\phi(\Delta T)]. \tag{47}$$

The relation between the autocorrelation and the power spectrum is given by the Khinchin theorem [21], i.e.,

$$R_\phi(\tau) = \int_{-\infty}^{\infty} S_\phi(f) e^{j2\pi f\tau}\, df \tag{48}$$

where $S_\phi(f)$ represents the power spectrum of $\phi(t)$. Therefore, (47) results in the following relationship between clock jitter and phase noise:

$$\sigma^2_{\Delta\phi} = \frac{8}{\omega_0^2}\int_0^{\infty} S_\phi(f)\sin^2(\pi f\tau)\, df. \tag{49}$$

It may be useful to know that $S_\phi(f)$ can be approximated by $\mathcal{L}\{\Delta f\}$ for large offsets [22]. As can be seen from the foregoing, the rms timing jitter has less information than the phase-noise spectrum and can be calculated from phase noise using (49). However, unless extra information about the shape of the phase-noise spectrum is known, the inverse is not possible in general.

In the special case where the phase noise is dominated by white noise, $\mathcal{L}\{\Delta f\}$ and κ are given by (6) and (12). Therefore, κ can be expressed in terms of phase noise in the $1/f^2$ region as

$$\kappa = \frac{\Delta f}{f_0}\cdot 10^{-\mathcal{L}\{\Delta f\}/20} \tag{50}$$

where $\mathcal{L}\{\Delta f\}$ is the phase noise measured in the $1/f^2$ region at an offset frequency of Δf and f_0 is the oscillation frequency. Therefore, based on (8), the rms cycle-to-cycle jitter will be given by

$$\sigma_{\rm CTC} = \frac{f}{f_0^{1.5}}\cdot 10^{-\mathcal{L}\{\Delta f\}/20}. \tag{51}$$

Note that for (50) and (51) to be valid, the phase noise at Δf should be in the $1/f^2$ region.

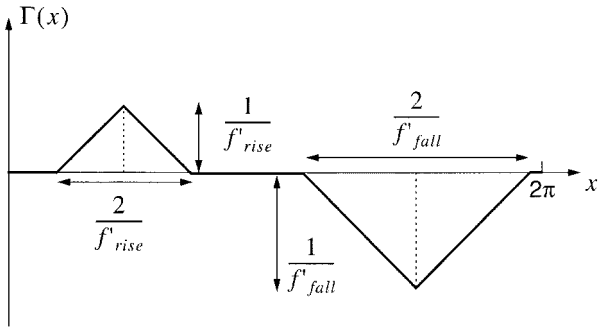

Fig. 18. Approximate waveform and the ISF for asymmetric rising and falling edges.

Appendix B
Nonsymmetric Rising and Falling Edges

We approximate the ISF in this Appendix by the function depicted in Fig. 18. The rms value of the ISF is

$$\Gamma^2_{\rm rms} = \frac{1}{2\pi}\int_0^{2\pi}\Gamma^2(x)\,dx = \frac{1}{\pi}\left[\int_0^{1/f'_{\rm rise}} x^2\,dx + \int_0^{1/f'_{\rm fall}} x^2\,dx\right] = \frac{1}{3\pi}\left(\frac{1}{f'_{\rm rise}}\right)^3(1+A^3) \tag{52}$$

where $f'_{\rm rise}$ and $f'_{\rm fall}$ are the maximum slope during the rising and falling edge, respectively, and A represents the asymmetry of the waveform and is defined as

$$A \equiv \frac{f'_{\rm rise}}{f'_{\rm fall}} \tag{53}$$

noting that

$$2\pi = \eta N\left(\frac{1}{f'_{\rm rise}} + \frac{1}{f'_{\rm fall}}\right) = \frac{\eta N}{f'_{\rm rise}}(1+A). \tag{54}$$

Combining (52) and (54) results in the following:

$$\Gamma^2_{\rm rms} = \frac{2\pi^2}{3\eta^3}\frac{1}{N^3}\left[4\frac{1+A^3}{(1+A)^3}\right] \tag{55}$$

which reduces to (16) in the special case of $A = 1$, i.e., symmetric rising and falling edges. The dc value of the ISF, $\Gamma_{\rm dc}$, can be calculated from Fig. 18 in a similar manner and is given by

$$\Gamma_{\rm dc} = \frac{2\pi}{\eta^2}\frac{1}{N^2}\left(\frac{1-A}{1+A}\right). \tag{56}$$

Using (7), the $1/f^3$ corner is given by

$$f_{1/f^3} = f_{1/f}\cdot\frac{3}{2\eta N}\cdot\frac{(1-A)^2}{(1-A+A^2)}. \tag{57}$$

As can be seen for a constant rise-to-fall ratio, the $1/f^3$ corner decreases inversely with the number of stages; therefore, ring oscillators with a smaller number of stages will have a larger $1/f^3$ noise corner. As a special case, if the rise and fall time are symmetric, $A = 1$, and the $1/f^3$ corner approaches zero.

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