Superharmonic Injection-Locked Frequency Dividers

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***Abstract*—Injection-locked oscillators (ILO's) are investigated in a new theoretical approach. A first-order differential equation is derived for the noise dynamics of ILO's. A single-ended injection-locked frequency divider (SILFD) is designed in a 0.5-μm CMOS technology operating at 1.8 GHz with more than 190 MHz locking range while consuming 3 mW of power. A differential injection-locked frequency divider (DILFD) is designed in a 0.5-μm CMOS technology operating at 3 GHz and consuming 0.45 mW, with a 190 MHz locking range. A locking range of 370 MHz is achieved for the DILFD when the power consumption is increased to 1.2 mW.**

***Index Terms*—Analog and digital frequency dividers, injection-locked oscillators, radio-frequency integrated circuits.**

I. Introduction

CONVENTIONAL phase-locked loops (PLL's) use frequency dividers in their feedback path to achieve frequency multiplication. Most PLL's designed for wireless systems use flip-flop-based digital frequency dividers. These dividers are wide band and their power consumption increases with the frequency of operation. In frequency synthesizers used in modern wireless systems, frequency dividers consume a large percentage of the total power [2], [8]. Most often, off-chip frequency dividers are used as the first stage in a stack of dividers in high-frequency PLL's [8]. The limitation on power and maximum frequency of operation of conventional digital frequency dividers is associated with the wide-band nature of these dividers. However, since most wireless systems are themselves narrow band, narrow-band analog frequency dividers may be used to reduce power and increase the maximum frequency of operation.

Regenerative frequency dividers [Fig. 1(a)] are the most widely used analog frequency dividers [5]–[7]. Frequency division in such a divider results from combining frequency multiplication in the feedback path with mixing at the input. Regenerative dividers can operate at frequencies higher than flip-flop-based dividers [13]. However, they require many functional blocks to guarantee frequency division [7]. As a result, regenerative frequency dividers are not the best solution for low-power systems.

Parametric frequency dividers [Fig. 1(b)] are another group of analog frequency dividers used in microwave systems [3], [5], [15]. The frequency division principle of a parametric frequency divider relies on exciting a varactor at frequency f and realizing a negative resistance that sustains a loop gain of unity at $f/2$. High Q varactors and inductors are key

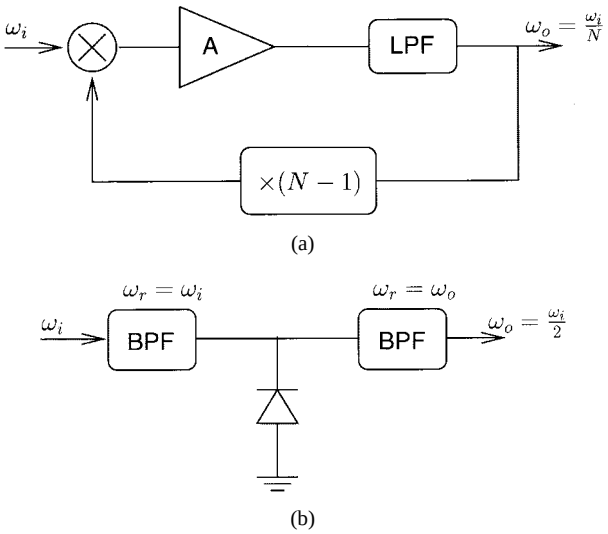

Fig. 1. Analog frequency dividers: (a) regenerative frequency divider and (b) parametric frequency divider.

elements in parametric frequency dividers [15]. Since high Q passive elements cannot be implemented in contemporary silicon technologies, parametric dividers are not amenable to integration.

The third group, injection-locked frequency dividers (ILFD's), work by synchronizing an oscillator with an incident signal. Depending upon the ratio of the incident frequency to the oscillation frequency, three classes of injection-locked oscillators (ILO's) may be defined: first-harmonic, subharmonic, and superharmonic ILO's. In a first-harmonic ILO, the oscillation frequency is the same as the fundamental frequency of the incident signal [1], while in a subharmonic ILO, the incident frequency is a subharmonic of the oscillation frequency [4], [9], [14], [20]. Likewise, in a superharmonic ILO, the incident frequency is a harmonic of the oscillation frequency. Uzunoglu *et al.* [16], [17] used synchronous oscillators (SO's) as frequency dividers, without providing a physical model for the frequency division functionality of SO's. The SO proposed in [17] is a nonlinear oscillator with a very large internal gain and a saturated output amplitude (voltage limited). High bias currents are required to provide the large gain and to operate SO's in a voltage-limited amplitude regime. Therefore, SO's are not appropriate for low-power systems. Unlike SO's, superharmonic ILO's can be designed as very low-power frequency dividers [10].

In this paper, we present a new method to calculate the locking range of ILO's. We also introduce two different mechanisms for failure of injection locking. A differential equation is derived that models the noise dynamics of ILO's.

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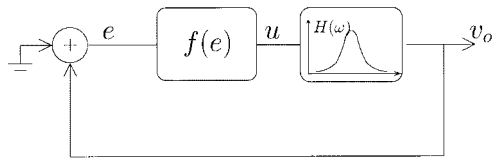

Fig. 2. Model for a free-running *LC* oscillator.

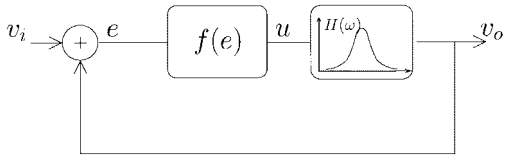

Fig. 3. Model for an injection-locked oscillator.

Measurements on a single-ended ILFD (SILFD) are compared with simulations. The simulation results of a differential ILFD (DILFD) are reported as well.

II. Model for Injection-Locked Oscillators

An *LC* oscillator can be modeled as a nonlinear block $f(e)$, followed by a frequency selective block (e.g., an *RLC* tank) $H(\omega)$, in a positive feedback loop as shown in Fig. 2. The nonlinear block models all the nonlinearities in the oscillator, including any amplitude-limiting mechanism. To have a steady-state oscillation, a loop gain of unity should be maintained. We would like to express the oscillation condition in terms of gain and phase criteria for reasons that will be clear later. The gain condition is satisfied if the output amplitude V_o is the same as the amplitude of $e(t)$ in an open-loop excitation of the system at the oscillation frequency ω_o. The phase condition requires that the excess phase introduced in the loop at $\omega = \omega_o$ be zero.

With an additional external signal (i.e., the incident signal), this same model can be used to model an ILO. This model is shown in Fig. 3. To investigate the injection-locking phenomenon in an ILO, we define

$$v_i(t) = V_i \cos(\omega_i t + \varphi) \tag{1}$$

$$v_o(t) = V_o \cos(\omega_o t) \tag{2}$$

$$u(t) = f(e(t)) = f(v_o(t) + v_i(t)) \tag{3}$$

$$H(\omega) = \frac{H_0}{1 + j2Q\frac{\omega - \omega_r}{\omega_r}} \tag{4}$$

where $v_i(t)$ is the incident signal, $v_o(t)$ is the output signal, φ is the phase difference between those two signals, and ω_r and Q are the resonant frequency and quality factor of the *RLC* tank, respectively. The output of the nonlinear block $u(t)$ may contain various harmonic and intermodulation terms of $v_i(t)$ and $v_o(t)$. As shown in Appendix A, we can write $u(t)$ as

$$\begin{aligned} u(t) &= f(v_i + v_o) \\ &= \sum_{m=0}^{\infty}\sum_{n=0}^{\infty} K_{m,n}\cos(m\omega_i t + m\varphi)\cos(n\omega_o t) \end{aligned} \tag{5}$$

where each $K_{m,n}$ is an intermodulation coefficient of $f(v_i + v_o)$.

We assume that all frequency components of $u(t)$ far from the resonant frequency of the tank are filtered out, so the frequency of the output signal can be written as $\omega_o = \omega_r + \Delta\omega$. Thus, we need only consider intermodulation terms with frequency ω_o, that is, $|m\omega_i - n\omega_o| = \omega_o$. For an Nth-order superharmonic ILO (i.e., $\omega_o = (1/N)\omega_i$), the intermodulation terms with $n = Nm \pm 1$ possess a frequency equal to $1/N$ of the incident frequency. The signal $u_{\omega_o}(t)$, which is the component of $u(t)$ with frequency ω_o, can be written as

$$u_{\omega_o}(t) = K_{0,1}\cos(\omega_o t) + \frac{1}{2}\sum_{m=1}^{\infty} K_{m,Nm\pm1}\cos(\omega_o t + m\varphi). \tag{6}$$

Using a complex exponential to replace sines and cosines, and applying the oscillation condition, the output signal can be written as

$$v_o = V_o e^{j\omega_o t} = \frac{H_0 e^{j\omega_o t}}{1 + j2Q\frac{\Delta\omega}{\omega_r}}\left[K_{0,1} + \frac{1}{2}\sum_{m=1}^{\infty} K_{m,Nm\pm1}e^{jm\varphi}\right] \tag{7}$$

or

$$V_o\left(1 + j2Q\frac{\Delta\omega}{\omega_r}\right) = H_0\left[K_{0,1} + \frac{1}{2}\sum_{m=1}^{\infty} K_{m,Nm\pm1}e^{jm\varphi}\right]. \tag{8}$$

The real and imaginary parts of (8) can be separated as

$$V_o = H_o\left[K_{0,1} + \frac{1}{2}\sum_{m=1}^{\infty} K_{m,Nm\pm1}\cos(m\varphi)\right] \tag{9}$$

$$2V_o Q\frac{\Delta\omega}{\omega_r} = \frac{H_0}{2}\sum_{m=1}^{\infty} K_{m,Nm\pm1}\sin(m\varphi). \tag{10}$$

Equations (9) and (10) are the fundamental equations for a superharmonic injection-locked oscillator. The simultaneous solution of these two equations specifies V_o and φ for any incident amplitude V_i and any incident frequency ω_i or, equivalently, for any offset frequency $\Delta\omega = (\omega_i/N) - \omega_r$. Equation (10) can be rearranged as

$$\Delta\omega = \Delta\omega_A\left[\frac{H_0}{2V_i}\sum_{m=1}^{\infty} K_{m,Nm\pm1}\sin(m\varphi)\right] \tag{11}$$

where $\Delta\omega_A = (\omega_r/2Q)(V_i/V_o)$ is Adler's *locking range* figure of merit [1]. The fundamental equations, (9) and (10), are very general but provide limited intuition. However, as shown in the next section, for the special case of $N = 2$ (i.e., divide-by-two) and a third-order nonlinearity (i.e., $f(e) = a_0 + a_1 e + a_2 e^2 + a_3 e^3$), (9) and (10) can be solved analytically, which allows the development of design insight.

A. Special Case ($N = 2$ and $f(e)$ Is a Third-Order Nonlinear Function)

For the special case of $N = 2$ and $f(e) = a_0 + a_1 e + a_2 e^2 + a_3 e^3$, the only unknown in (10) is the input–output

phase difference φ, which means the phase condition can be satisfied independently of the gain condition

$$\sin(\varphi) = \frac{2Q}{H_o a_2 V_i}\frac{\Delta\omega}{\omega_r}$$
$$|\sin(\varphi)| < 1 \Rightarrow \left|\frac{\Delta\omega}{\omega_r}\right| < \left|\frac{H_0 a_2 V_i}{2Q}\right|. \tag{12}$$

On the other hand, satisfying the gain condition and solving (9) results in an expression for the oscillation amplitude

$$V_o = \sqrt{\frac{4}{3}\frac{1}{a_3 H_0}\left[1 - H_0\left(a_1 + \frac{3}{2}a_3 V_i^2 + a_2 V_i\cos(\varphi)\right)\right]}. \tag{13}$$

As (12) suggests, the locking range can be increased by increasing either H_0/Q or the incident amplitude V_i. Increasing H_0/Q in an *LC* oscillator is equivalent to using an inductor with a larger value ($H_0/Q = \omega L$). The self-resonant frequency of the inductor puts a limit on the maximum inductor size and effectively limits the locking range by failing to satisfy the phase condition. The increase of the locking range with the incident amplitude is also limited. When the term under the square root in (13) becomes negative, the gain condition fails and limits the locking range. As a result, injection locking fails and the locking range is limited by failure of either the phase condition (phase limited) or the gain condition (gain limited). The effect of each limiting mechanism on the noise performance of an ILO is discussed in more detail in Section V-A.

As mentioned before, the locking range in an ILO is a function of the incident amplitude. So, by injecting the incident signal into a high-impedance node, the required incident power can be reduced significantly. Due to the high impedance of the gate of MOS transistors, MOS transistors are a good candidate for injection-locked oscillators.

The underlying assumption in the derivation of (9) and (10) is that the resonant frequency of the *LC* tank does not change as the incident frequency changes. However, to achieve a larger tuning range, the free-running oscillation frequency of the ILO can be modified such that it tracks the incident frequency [11], [12].

III. Noise in ILO's

To investigate the phase noise performance of an ILO, we first consider the response of a first-harmonic ILO to a deterministic sinusoidal noise. For convenience, the model for an ILO is repeated in Fig. 4 with the noise v_n added to the summing junction. The noise can be either from the incident signal or from the ILO itself. The incident signal, output signal, and sinusoidal noise are represented by their equivalent phasors in Fig. 5 and mathematically defined as

$$v_i(t) = V_i\cos(\omega_o t) \tag{14}$$
$$v_o(t) = V_o\cos(\omega_o t + \varphi) \tag{15}$$
$$v_n(t) = V_n\cos((\omega_o + \omega_n)t + \varphi_n). \tag{16}$$

When the output signal is injection locked to the incident signal in the absence of noise, the input–output phase difference is constant ($\varphi = \varphi_o$). However, when sinusoidal noise

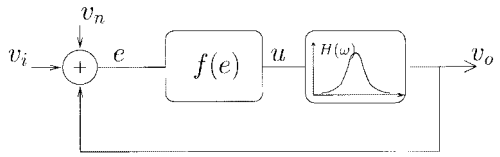

Fig. 4. ILO model used for noise analysis.

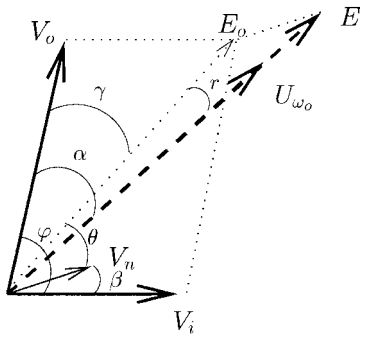

Fig. 5. Phasor representation of signals in Fig. 4.

with an offset frequency ω_n is added to the system, φ is no longer constant and the instantaneous output frequency ω is defined as

$$\omega = \omega_o + \frac{d\varphi}{dt}. \tag{17}$$

It is the variation of φ that generates phase noise in the output signal. As shown in Appendix B, $\frac{d\varphi}{dt}$ can be approximated as

$$\frac{d\varphi}{dt} \simeq -\Delta\omega_o - \frac{1}{A}\left[\frac{V_i}{V_o}\sin(\varphi) - \frac{V_n}{V_o}\cos(\varphi)\sin(\beta)\right] \tag{18}$$

where $\Delta\omega_0$ is the difference between the incident frequency and the free-running frequency, $A = (2Q)/\omega_r$, and $\beta = \omega_n t + \varphi_n$.

The input–output phase difference can be written as

$$\varphi = \varphi_o + \varphi_\epsilon \tag{19}$$

where φ_o is the input–output phase difference in the absence of noise and is a constant [$\Delta\omega_o = -V_i/(AV_o)\sin(\varphi_o)$ from (45)] and φ_ϵ is the time-variant portion of φ. $\varphi_\epsilon \ll 1$ because $V_n \ll V_i \ll V_o$. Hence (18) can be simplified to

$$\frac{d\varphi_\epsilon}{dt} + K\varphi_\epsilon = \frac{V_n}{AV_o}\cos(\varphi_o)\sin(\beta) \tag{20}$$

where

$$K = \frac{V_i}{AV_o}\cos(\varphi_o) - \frac{V_n}{AV_o}\sin(\varphi_o)\sin(\beta). \tag{21}$$

If $\tan(\varphi_o) \ll V_i/V_n$, meaning that the incident frequency is not at the edge of a phase-limited locking range, K can be approximated as

$$K \simeq \frac{V_i}{AV_o}\cos(\varphi_o) \tag{22}$$

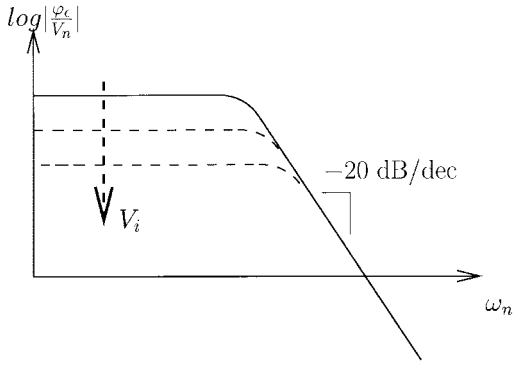

Fig. 6. Noise transfer function of an ILO.

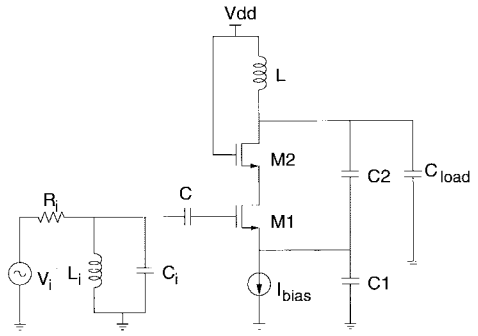

Fig. 7. Schematic of the single-ended injection-locked frequency divider.

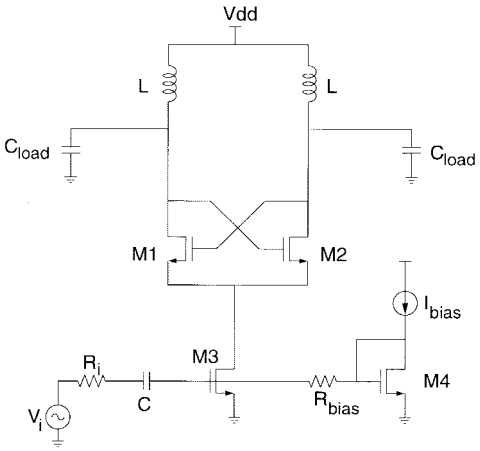

Fig. 8. Schematic of the differential injection-locked frequency divider.

which allows simplification of (20) to a first-order differential equation

$$\frac{d\varphi_\epsilon}{dt} + \left[\frac{V_i}{AV_o}\cos(\varphi_o)\right]\varphi_\epsilon = \left[\frac{V_n}{AV_o}\cos(\varphi_o)\right]\sin(\omega_n t + \varphi_n). \tag{23}$$

The noise transfer function from v_n to the output phase (23) is shown in Fig. 6. From (23) and Fig. 6, it is clear that an ILO has the same noise transfer function as a first-order PLL. The noise from the incident signal is shaped by the low-pass characteristic of the noise transfer function, and the output signal tracks the phase variations of the incident signal within the loop bandwidth $(V_i/(AV_o)\cos(\varphi_o))$. However, unlike a first-order PLL, the loop bandwidth of an ILO is a function of the incident amplitude and is larger for a larger incident amplitude.

The interpretation of the noise transfer function is a little different if the noise comes from the ILO itself. Within the loop bandwidth, the noise from the ILO is suppressed by the ratio of the noise power to the incident power. Outside the loop bandwidth, the noise suppression increases by 20 dB per decade of offset frequency, and a $1/f^2$ phase noise region is observed.

The noise dynamics in a superharmonic ILO are the same as those of a first-harmonic ILO, except $(d\varphi_\epsilon)/(dt)$ is $1/N$ of that in a first-harmonic ILO due to the frequency division operation. So (23) for an Nth-order ILFD can be modified as

$$\frac{d\varphi_\epsilon}{dt} + \left[\frac{V_i}{AV_o}\cos(\varphi_o)\right]\varphi_\epsilon = \frac{1}{N}\left[\frac{V_n}{AV_o}\cos(\varphi_o)\right]\sin(\omega_n t + \varphi_n) \tag{24}$$

where φ_o is no longer a simple function of $\Delta\omega_0$ but is determined by solving the superharmonic ILO's fundamental equations, (9) and (10). As the division ratio N increases, the noise rejection increases proportionally. So in a divide-by-two ILFD, the output close-in phase noise is $20\log(2) = 6$ dB lower than that of the incident signal.

IV. Circuit Implementation

In this paper, we propose two different architectures for ILFD's. Fig. 7 shows the schematic of an SILFD. For simplicity, the biasing circuitry is not shown in this figure. A Colpitts oscillator forms the core of the SILFD. The incident signal is injected into the gate of M1. Transistors M1 and M2 are used in cascode, mainly to provide more isolation between the input and output. Transistor M2 is sized to be smaller than M1 by almost a factor of three to reduce the parasitic capacitance at the output node (drain of M2). As a result, a larger inductor can be used to resonate this reduced capacitance. As discussed in Section II-A, using a larger inductor increases the locking range. The power consumption is also reduced due to the increased effective parallel impedance of the *LC* tank, assuming that tank losses are mainly from the inductor. Last, Li and Ci in the gate of M1 are used to model the *LC* tank of the preceding *LC* oscillator. The analogy of this circuit with the model in Fig. 3 can be realized by observing that transistor M1 functions as the summing element for the incident and output signals.

The schematic of a DILFD is shown in Fig. 8. The incident signal is injected into the gate of M3, which delivers the incident signal to the common source connection of M1 and M2. The output signal is fed back to the gates of M1 and M2. The output and incident signals are thus summed across the gates and sources of M1 and M2. The common source connection of M1 and M2, even in the absence of the incident signal, oscillates at twice the frequency of the output signal, which makes this node an appropriate injection node for a divide-by-two operation.

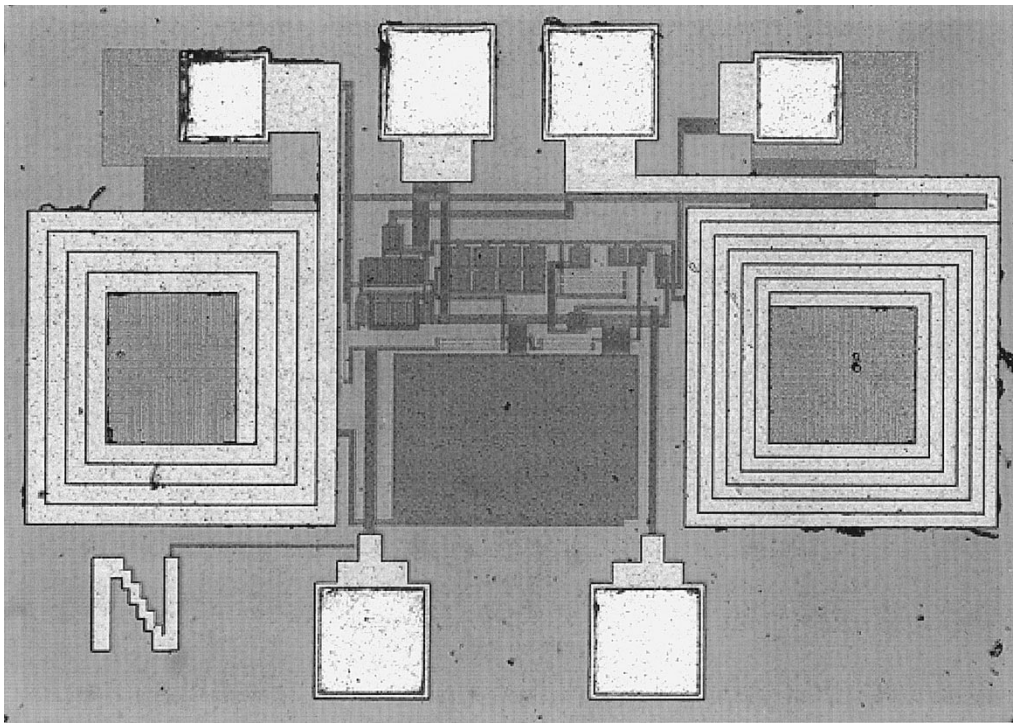

Fig. 9. Die micrograph of the SILFD (0.7×1 mm^2).

V. Simulation and Measurement Results

A. Single-Ended ILFD

The SILFD shown in Fig. 7 is designed in a 0.5-μm CMOS technology and operates on 2.5 V and a bias current of 1.2 mA. The free-running frequency of oscillation is 920 MHz, and the incident frequency is around 1840 MHz. Both inductors are on-chip spiral inductors with patterned ground shields [18], [19]. The die micrograph of the SILFD is shown in Fig. 9. The total area of the die is 0.7 mm^2 (0.7×1 mm^2).

The oscillation amplitude of the SILFD is plotted in Fig. 10 as a function of the incident frequency for different incident amplitudes. The locking range is determined by the frequency difference between the two ends of each curve. At small incident amplitudes, the locking range is phase limited, as explained in Section II-A, and increases with the incident amplitude. However, for incident amplitudes beyond 300 mV, the locking range is gain limited and shrinks as the incident amplitude increases. Simulated and measured locking range as a function of incident amplitude are shown in Fig. 11. A locking range of more than 190 MHz (11% of the center frequency) is achieved when consuming 3 mW of power. The maximum locking range as a function of bias current is shown in Fig. 12. A locking range of more than 135 MHz is achieved with a bias current as low as 600 μA.

Phase noise measurement results are shown in Fig. 13. The thin solid line in this figure shows the phase noise of the free-running SILFD. The thick solid line is the phase noise of the HP8664A signal generator used as the incident signal. The nonsolid lines are the phase noise measurement of the SILFD when locked to three different incident frequencies, referred to as middle-frequency, phase-limited, and gain-limited curves.

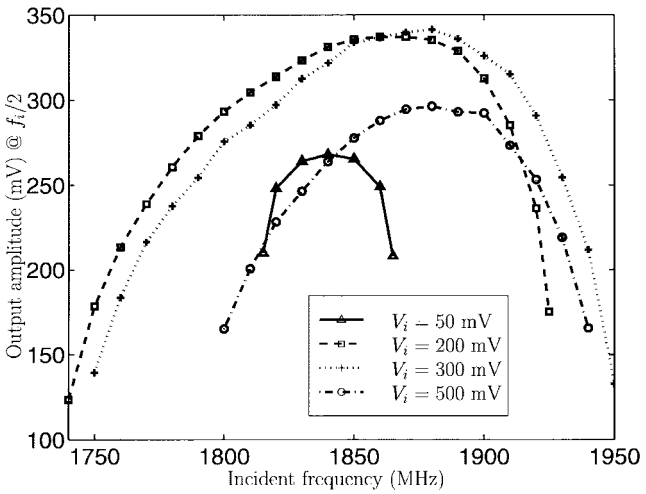

Fig. 10. Oscillation amplitude in the SILFD.

The middle-frequency curve is the output phase noise measured at an incident frequency in the middle of the locking range. The phase- and gain-limited curves are measured when the incident frequency is at the edge of a phase- and gain-limited locking range, respectively.

At low offset frequencies, the divider output phase noise is almost 6 dB lower than the incident phase noise, as is expected from the divide-by-two operation and predicted by (24). However, at higher offset frequencies, the excess noise from the divider increases the output phase noise. The far-out phase noise at the edge of a gain-limited locking range is even worse than the phase noise of the free-running oscillator. The small oscillation amplitude at the edge of a gain-limited

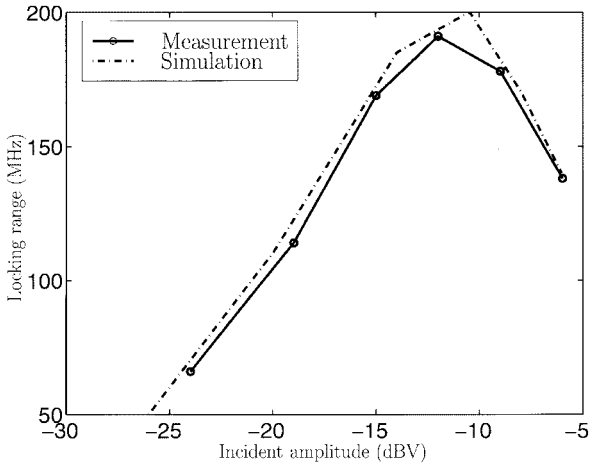

Fig. 11. Locking range for the SILFD.

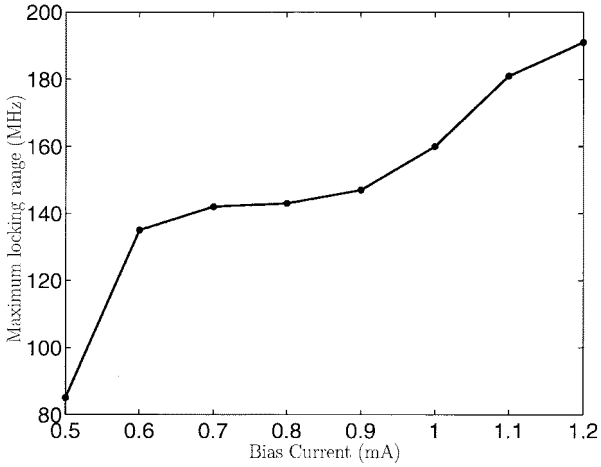

Fig. 12. Locking range as a function of the bias current in the SILFD.

locking range explains this higher phase noise of the ILFD at large offset frequencies.

Despite the large close-in phase noise of the free-running ILFD, the divider phase noise tracks the phase noise of the incident signal for offset frequencies up to 100 kHz. As a result, the ILFD can be designed for very low-power operation without sacrificing the noise performance of the system. Also, very low Q on-chip spiral inductors, with small physical dimensions, can be used in ILFD's.

B. Differential ILFD

A DILFD (Fig. 8) is designed in a 0.5-μm CMOS technology. The supply voltage is 1.5 V and the tail current is nominally 300 μA. The DILFD oscillates at 1.6 GHz in free-running operation, and the incident frequency is in the vicinity of 3.2 GHz. On-chip spiral inductors with a Q of 5.8 are used in this design.

The oscillation amplitude as a function of incident frequency is shown in Fig. 14. Comparing this with Fig. 10, two differences are observed. In Fig. 14, the curves are flatter and the locking range increases monotonically with incident amplitude. These suggest that the locking range in the DILFD is phase limited, unlike the gain-limited locking range in the

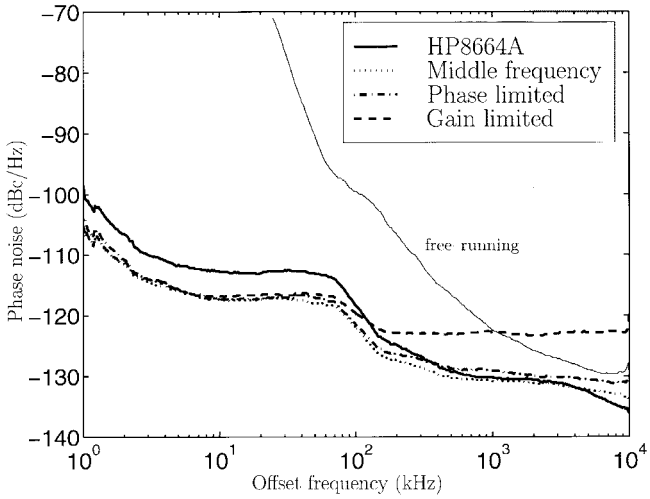

Fig. 13. Phase noise measurement in the SILFD.

SILFD at large incident amplitudes. This can partially be due to the subunity voltage gain of M3 in Fig. 8. As a result, the amplitude of the injected signal at the summing node (the common source connection of M1 and M2) of the DILFD is less than that of the SILFD. Also, the increased tail current in the presence of a large incident signal changes $f(e)$, which can effectively change the phase-limited region of the locking range in DILFD's.

More than 190 MHz of locking range is achieved with only 0.45 mW of power (Fig. 14). By increasing the power to 1.2 mW, the locking range increases to 370 MHz (12% of the center frequency). The DILFD is expected to have a better phase noise than the SILFD over the entire locking range, due to its phase-limited locking range.

The performance of the SILFD and DILFD is summarized in Table I. For comparison purposes, the performance of a conventional frequency divider made out of two back-to-back connected source-coupled-logic (SCL) latches designed in the same technology is also tabulated. The SCL divider operates at about half the frequency of the DILFD and consumes more than four times the power. The SCL divider also fails to operate above 3 GHz. The last column in Table I shows the simulated acquisition time in ILFD's. The acquisition time, which measures how fast an ILFD locks to an incident signal, is inversely proportional to the locking range. Therefore, as long as the locking range is phase limited, increasing the incident amplitude reduces the acquisition time.

C. Noise Transfer Function

To verify the noise dynamics derived in Section III, the SILFD is injection locked to an incident frequency while a second signal is injected at different offset frequencies from the incident frequency. As demonstrated in Fig. 15, two sidebands are generated in the output signal spectrum. The power below carrier of the sidebands is measured at different offset frequencies and is shown in Figs. 16 and 17. In Fig. 16, the incident power P_i is constant and the noise transfer function is measured for three noise power levels P_n.

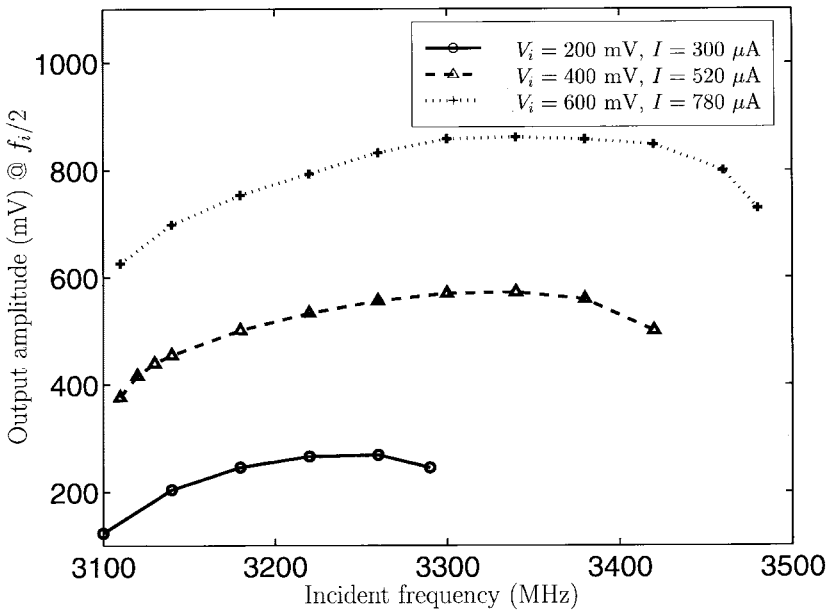

Fig. 14. Oscillation amplitude in the DILFD.

TABLE I
FREQUENCY DIVIDER PERFORMANCE

Divider	f(GHz)	V_{dd}	$I(\mu A)$	P(mW)	Δf(MHz)	t_a(ns)
SILFD	1.8	2.5	600	1.5	135	≤ 9
(Measured)			1200	3.0	191	≤ 7
DILFD	3.5	1.5	300	0.45	190	≤ 7
(Simulated)			400	0.60	260	≤ 6
			780	1.17	370	≤ 5
SCL Latch	1.8	2.0	1000	2.0	1800	
(Simulated)	3.0	Failed				

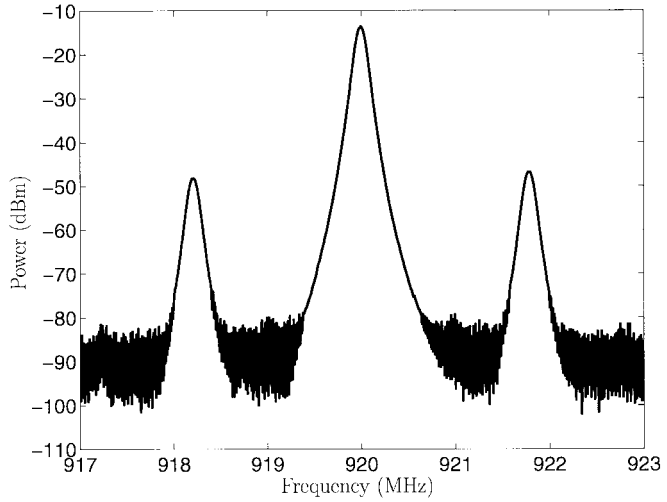

Fig. 15. Sideband generation due to noise injection at a frequency offset from the incident frequency.

As predicted by (24), reducing the noise power by 3 dB shifts the noise transfer function curve down by the same amount.

The same measurement is repeated for different incident powers while keeping the noise power constant. The results are shown in Fig. 17. When the incident power increases by 3 dB, both the loop bandwidth and the close-in noise rejection increase by 3 dB, while the far-out noise does not change. The

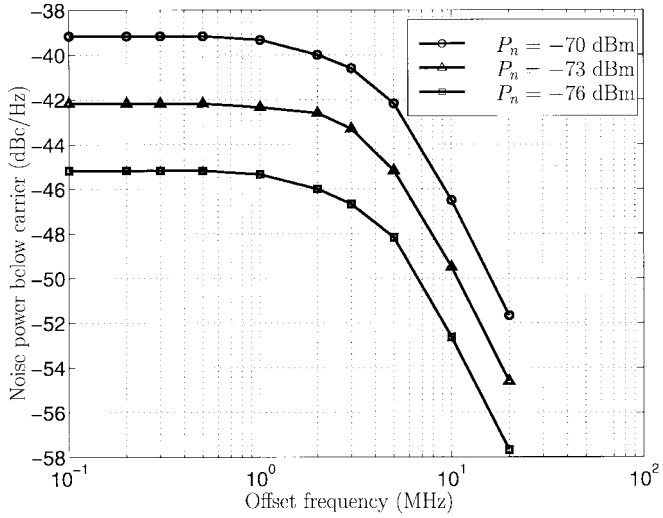

Fig. 16. Noise transfer function in the SILFD ($P_i = -40$ dBm).

noise transfer function measurement results of Figs. 16 and 17 are in very good agreement with (24).

VI. CONCLUSION

A new method is reported for calculating the locking range of injection-locked oscillators. Two different mechanisms for the failure of injection locking are introduced. It is shown mathematically that the noise transfer function of an ILO is the same as that of a first-order PLL. Two novel circuits for single-ended and differential ILFD's are proposed. The measurement results of the SILFD verify the theory of injection locking and the model for the noise dynamics of ILO's. It is shown that ILFD's can operate at frequencies where conventional digital frequency dividers fail and still consume less power than digital frequency dividers operating at lower frequencies (Table I). Unlike digital frequency dividers, the power consumption in

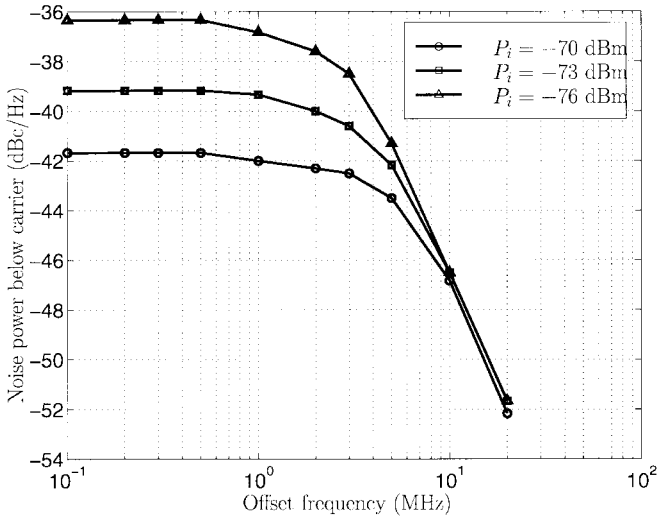

Fig. 17. Noise transfer function in the SILFD ($P_n = -70$ dBm).

an ILFD does not increase linearly with the frequency of operation. Therefore, injection-locked frequency dividers are attractive for digital CMOS frequency dividers, especially for low-power and high-frequency wireless systems.

APPENDIX A

To simplify the proof of (5), we redefine v_i, v_o, and $f(e)$ as

$$v_i = V_i \cos(\beta) \tag{25}$$

$$v_o = V_o \cos(\alpha) \tag{26}$$

$$f(e) = f(v_i + v_o) \tag{27}$$

where $\alpha = \omega_i t + \varphi$ and $\beta = \omega_o t$. Function $f(e)$ is periodic with respect to both α and β. For every β, we can define a periodic function $g(\alpha)$ as

$$g(\alpha) = f(v_o + V_i \cos(\alpha)). \tag{28}$$

Since $g(\alpha + 2\pi) = g(\alpha)$ and $g(-\alpha) = g(\alpha)$, $g(\alpha)$ can be represented by its Fourier series as

$$g(\alpha) = \sum_{m=0}^{\infty} L_m(\beta) \cos(m\alpha) \tag{29}$$

where each $L_m(\beta)$ is a Fourier series coefficient of $g(\alpha)$ and is calculated as

$$L_0(\beta) = \frac{1}{2\pi} \int_0^{2\pi} f(V_o \cos(\beta) + V_i \cos(\alpha))\, d\alpha \tag{30}$$

$$L_m(\beta) = \frac{1}{\pi} \int_0^{2\pi} f(V_o \cos(\beta) + V_i \cos(\alpha)) \cos(m\alpha)\, d\alpha. \tag{31}$$

Since each L_m is even and periodic with period 2π, it can be represented in terms of its Fourier series as

$$L_m(\beta) = \sum_{n=0}^{\infty} K_{m,n} \cos(n\beta) \tag{32}$$

where

$$K_{m,0} = \frac{1}{2\pi} \int_0^{2\pi} L_m(\beta)\, d\beta \tag{33}$$

$$K_{m,n} = \frac{1}{\pi} \int_0^{2\pi} L_m(\beta) \cos(n\beta)\, d\beta. \tag{34}$$

Now to complete the proof, insert (32) into (29) and replace $g(\alpha)$ by $f(v_i + v_o)$

$$f(v_i + v_o) = \sum_{m=0}^{\infty} \sum_{n=0}^{\infty} K_{m,n} \cos(m\alpha) \cos(n\beta). \tag{35}$$

APPENDIX B

To derive (23), we start by evaluating the excess phase introduced in the loop, excluding the phase added by the frequency selective block in a first-harmonic ILO.

The phasor representation of $e(t)$, E (Figs. 4 and 5), is calculated as the vector sum of V_i, V_o, and V_n. As E experiences the nonlinearities of $f(e)$, new harmonics are generated, but u_{ω_o}, the component of $u(t)$ with the same instantaneous frequency as $e(t)$, stays in phase with $e(t)$. So U_{ω_o}, the phasor representation of u_{ω_o}, and E have the same direction, as shown in Fig. 5. The phase difference introduced between V_o and U_{ω_o} is equal to

$$\alpha = \gamma + r \tag{36}$$

where γ is the phase difference between V_o and E_o (vector sum of V_o and V_i) and r is the phase difference between E_o and U_{ω_o} (Fig. 5). Since $V_n \ll V_i \ll V_o$, we can approximate γ and r as

$$\gamma \simeq \tan(\gamma) = \frac{V_i \sin(\varphi)}{V_o + V_i \cos(\varphi)} \simeq \frac{V_i}{V_o} \sin(\varphi) \tag{37}$$

$$r \simeq \tan(r) \simeq \frac{V_n \sin(\theta)}{E} \simeq \frac{V_n}{V_o + V_i \cos(\varphi)} \sin(\theta) \cos(\gamma) \tag{38}$$

$$r \simeq \frac{V_n}{V_o} \sin(\theta) \tag{39}$$

where

$$\theta = \varphi - \gamma - \beta \simeq \varphi - \beta. \tag{40}$$

To satisfy the phase condition, α should be canceled out by the phase introduced by the *RLC* tank ($\Delta\phi_{\mathrm{RLC}}$). Thus

$$\alpha = \Delta\phi_{\mathrm{RLC}} \simeq -\frac{2Q}{\omega_r}(\Delta\omega) = -A\Delta\omega \tag{41}$$

where

$$A = \frac{2Q}{\omega_r} \tag{42}$$

and

$$\Delta\omega = \omega - \omega_r = \omega - (\omega_o - \Delta\omega_0) = \frac{d\varphi}{dt} + \Delta\omega_o \tag{43}$$

where ω is replaced by its equivalent from (17). To calculate $(d\varphi)/(dt)$, we insert (43) and (36) into (41) and rearrange the terms

$$\frac{d\varphi}{dt} = -\Delta\omega_o - \frac{1}{A}(\gamma + r). \tag{44}$$

Equation (44) can be further expanded by replacing γ and r from (37) and (39)

$$\frac{d\varphi}{dt} = -\Delta\omega_o - \frac{1}{A}\left[\frac{V_i}{V_o} \sin(\varphi) + \frac{V_n}{V_o} \sin(\theta)\right]. \tag{45}$$

Now if we replace θ by $\varphi - \beta$ from (40) and expand $\sin(\varphi - \beta)$, (45) can be written as

$$\frac{d\varphi}{dt} = -\Delta\omega_o - \frac{1}{A}\left[\sin(\varphi)\left(\frac{V_i}{V_o} + \frac{V_n}{V_o}\cos(\beta)\right) - \frac{V_n}{V_o}\cos(\varphi)\sin(\beta)\right]. \quad (46)$$

Since $V_n \ll V_i$, we can approximate $(d\varphi)/(dt)$ as

$$\frac{d\varphi}{dt} \simeq -\Delta\omega_o - \frac{1}{A}\left[\frac{V_i}{V_o}\sin(\varphi) - \frac{V_n}{V_o}\cos(\varphi)\sin(\beta)\right] \quad (47)$$

which ends our derivation.

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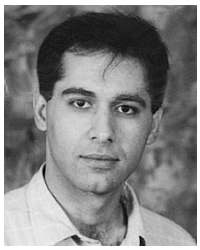

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Thomas H. Lee (S'87–M'87), for a photograph and biography, see p. 585 of the May 1999 issue of this JOURNAL.