

Simple Accurate Expressions for Planar Spiral Inductances

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Abstract—We present several new simple and accurate expressions for the DC inductance of square, hexagonal, octagonal, and circular spiral inductors. We evaluate the accuracy of our expressions, as well as several previously published inductance expressions, in two ways: by comparison with three-dimensional field solver predictions and by comparison with our own measurements, and also previously published measurements. Our simple expression matches the field solver inductance values typically within around 3%, about an order of magnitude better than the previously published expressions, which have typical errors around 20% (or more). Comparison with measured values gives similar results: our expressions (and, indeed, the field solver results) match within around 5%, compared to errors of around 20% for the previously published expressions. (We believe most of the additional errors in the comparison to published measured values is due to the variety of experimental conditions under which the inductance was measured.)

Our simple expressions are accurate enough for design and optimization of inductors or of circuits incorporating inductors. Indeed, since inductor tolerance is typically on the order of several percent, “more accurate” expressions are not really needed in practice.

Index Terms— CMOS analog integrated circuits, inductors, integrated circuit design, integrated circuit modeling.

I. INTRODUCTION

THE RISING demand for low-cost radio frequency integrated circuits (RF-IC's) has generated tremendous interest in on-chip passive components [1]. Currently, there are several integrated resistor and capacitor options and most of these implementations are easy to model. Considerable effort has also gone into the design and modeling of inductor implementations, of which the only practical options are bond wires and planar spiral geometries. Although bond wires permit a high quality factor (Q) to be achieved, with typical Q 's in the 20–50 range, their inductance values are constrained and can be rather sensitive to production fluctuations. On the other hand, planar spiral inductors have limited Q 's, but have inductances that are well-defined over a broad range of process variations. Thus, planar spiral inductors have become essential elements of communication circuit blocks such as voltage controlled oscillators (VCO's), low-noise amplifiers (LNA's), mixers, and intermediate frequency filters (IFF's).

Square spirals are popular because of the ease of their layout. Squares are generated easily even in simple Manhattan-style layout tools (such as MAGIC). However, other polygonal spirals have also been used in circuit design. Some designers prefer polygons with more than four sides to improve per-

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formance. Among these, hexagonal and octagonal inductors are used widely. Fig. 1(a)–(d) shows the layout for square, hexagonal, octagonal, and circular inductors, respectively. For a given shape, an inductor is completely specified by the number of turns n , the turn width w , the turn spacing s , and any one of the following: the outer diameter d_{out} , the inner diameter d_{in} , the average diameter $d_{\text{avg}} = 0.5(d_{\text{out}} + d_{\text{in}})$, or the *fill ratio*, defined as $\rho = (d_{\text{out}} - d_{\text{in}})/(d_{\text{out}} + d_{\text{in}})$. The thickness of the inductor has only a very small effect on inductance and will therefore be ignored in this paper.

To facilitate the design of such components, significant work has gone into modeling spiral inductors using lumped circuit models [2], [3]. Fig. 2 illustrates a commonly used model. The parasitic resistors and capacitors in this model have simple physically intuitive expressions, but the inductance value lacks a simple but accurate expression.

This inductance can be computed exactly by solving Maxwell's equations. A very accurate numerical solution may be obtained by using a three-dimensional (3-D) finite-element simulator such as MagNet [4]. However, 3-D simulators are computationally intensive and require long run times, and so are more appropriate for *design verification* than the *design* of an inductor. Another technique is to use the Greenhouse method [2], [5], [6] to compute the inductance. The Greenhouse method offers sufficient accuracy and adequate speed, but cannot provide an inductor design directly from specifications and is cumbersome for initial design.

At the other extreme we can use a simple approximate expression for the inductance [7]–[10]. While the simple expressions do predict the correct order of magnitude of the inductance, typical errors are 20% or more, which is unacceptable for circuit design and optimization.

In Section II, we describe new approximate expressions for the inductance of square, hexagonal, octagonal, and circular planar inductors. The first approximation is based on a modification of an expression developed by Wheeler [11]; the second is derived from electromagnetic principles by approximating the sides of the spirals as current-sheets; and the third is a monomial expression derived from fitting to a large database of inductors (and the exact inductance values). All three expressions are accurate, with typical errors of 2–3%, and very simple, and are therefore excellent candidates for use in design and synthesis.

The accuracy of these approximate expressions was evaluated in two ways: with field solver simulations and also with measurement data. For simulations, we used ASITIC, a simplified field solver geared for the design of inductors and transformers [12]. We used a wide range of inductors, with d_{out} varying from 100–480 μm , L varying from 0.5–100 nH, w varying from 2 μm to 0.3 d_{out} , s varying from 2

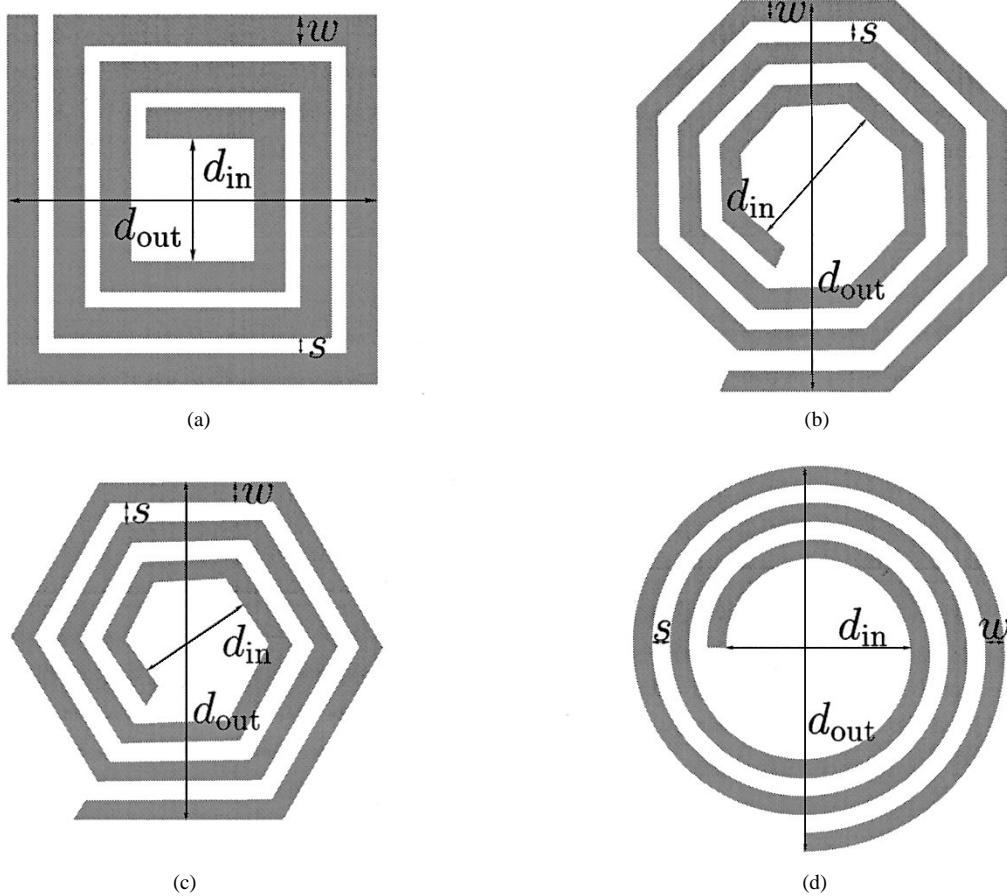


Fig. 1. On-chip inductor realizations: (a) square, (b) hexagonal, (c) octagonal, and (d) circular.

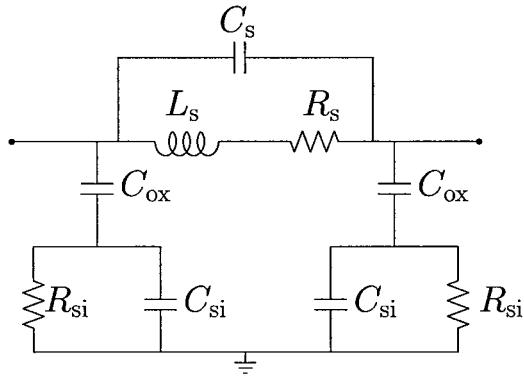


Fig. 2. Lumped inductor model.

μm to 3 w , and d_{in} varying from 0.1–0.9 d_{out} . A total of 19 000 inductors were simulated using the program ASITIC, spanning the entire design space that is of use for RF circuit designs. (We did not consider inductors larger than 100 nH, since such inductors have a total length great enough that they can no longer be considered lumped at frequencies of interest. See [13] for further discussion of this topic.) Our approximate expressions were also verified using around 60 measurement results that have been reported in the literature. Both previously published expressions and our expressions are compared to these measurements in Section IV. We summarize our findings in Section V.

II. NEW EXPRESSIONS

In this section we describe our new expressions for the inductance.

A. Modified Wheeler Formula

Wheeler [11] presented several formulas for planar spiral inductors, which were intended for discrete inductors. We have found that a simple modification of the original Wheeler formula allows us to obtain an expression that is valid for planar spiral integrated inductors

$$L_{\text{mw}} = K_1 \mu_0 \frac{n^2 d_{\text{avg}}}{1 + K_2 \rho} \quad (1)$$

where ρ is the fill ratio defined previously. The coefficients K_1 and K_2 are layout dependent and are shown in Table I. The ratio ρ represents how hollow the inductor is: for small ρ we have a hollow inductor ($d_{\text{out}} \approx d_{\text{in}}$) and for a large ρ we have a full inductor ($d_{\text{out}} \gg d_{\text{in}}$). Two inductors with the same average diameter but different fill ratios will, of course, have different inductance values. The full one has a smaller inductance because its inner turns are closer to the center of the spiral and so contribute less positive mutual inductance and more negative mutual inductance.

B. Expression Based on Current Sheet Approximation

Another simple and accurate expression for the inductance of a planar spiral can be obtained by approximating the sides

TABLE I
COEFFICIENTS FOR MODIFIED WHEELER EXPRESSION

Layout	K_1	K_2
Square	2.34	2.75
Hexagonal	2.33	3.82
Octagonal	2.25	3.55

TABLE II
COEFFICIENTS FOR CURRENT SHEET EXPRESSION

Layout	c_1	c_2	c_3	c_4
Square	1.27	2.07	0.18	0.13
Hexagonal	1.09	2.23	0.00	0.17
Octagonal	1.07	2.29	0.00	0.19
Circle	1.00	2.46	0.00	0.20

of the spirals by symmetrical current sheets of equivalent current densities [14]. For example, in the case of the square, we obtain four identical current sheets. The current sheets on opposite sides are parallel to one another, whereas the adjacent ones are orthogonal. Using symmetry and the fact that sheets with orthogonal current sheets have zero mutual inductance, the computation of the inductance is now reduced to evaluating the self-inductance of one sheet and the mutual inductance between opposite current sheets. These self- and mutual inductances are evaluated using the concepts of geometric mean distance (GMD), arithmetic mean distance (AMD), and arithmetic mean square distance (AMSD [14], [15]). The resulting expression is

$$L_{gmd} = \frac{\mu n^2 d_{\text{avg}} c_1}{2} (\ln(c_2/\rho) + c_3\rho + c_4\rho^2) \quad (2)$$

where the coefficients c_i are layout dependent and are shown in Table II. Although the accuracy of this expression worsens as the ratio s/w becomes large, it exhibits a maximum error of 8% for $s \leq 3w$. Note that typical practical integrated spiral inductors are built with $s \leq w$. The reason is that a smaller spacing improves the interwinding magnetic coupling and reduces the area consumed by the spiral. A large spacing is only desired to reduce the interwinding capacitance. In practice, this is not a concern as this capacitance is dwarfed by the underpass capacitance [2].

C. Data Fitted Monomial Expression

Our final expression is based on a data fitting technique, which yielded the expression

$$L_{\text{mon}} = \beta d_{\text{out}}^{\alpha_1} w^{\alpha_2} d_{\text{avg}}^{\alpha_3} n^{\alpha_4} s^{\alpha_5} \quad (3)$$

where the coefficients β and α_i are layout dependent and given in Table III. The expression in (3) is called a *monomial* in the variables d_{out} , w , d_{avg} , n , and s . The coefficients were obtained as follows. We first change variables to use the logarithms of the variables: $x_1 = \log d_{\text{out}}$, $x_2 = \log w$, $x_3 = \log d_{\text{avg}}$, $x_4 = \log n$, $x_5 = \log s$. Taking the logarithm of the inductance as well we can express the monomial relation (3) as

$$y = \log L = \alpha_0 + \alpha_1 x_1 + \alpha_2 x_2 + \alpha_3 x_3 + \alpha_4 x_4 + \alpha_5 x_5$$

where $\alpha_0 = \log \beta$. This is a linear-plus-constant model of y as a function of x , and is easily fit by various regression

TABLE III
COEFFICIENTS FOR DATA-FITTED MONOMIAL EXPRESSION

Layout	β	$\alpha_1 (d_{\text{out}})$	$\alpha_2 (w)$	$\alpha_3 (d_{\text{avg}})$	$\alpha_4 (n)$	$\alpha_5 (s)$
Square	$1.62 \cdot 10^{-3}$	-1.21	-0.147	2.40	1.78	-0.030
Hexagonal	$1.28 \cdot 10^{-3}$	-1.24	-0.174	2.47	1.77	-0.049
Octagonal	$1.33 \cdot 10^{-3}$	-1.21	-0.163	2.43	1.75	-0.049

or data-fitting techniques. To develop our models we used a simple least-squares fit: we chose α_i to minimize

$$\sum_{k=1}^N \left(y^{(k)} - \alpha_0 - \alpha_1 x_1^{(k)} - \alpha_2 x_2^{(k)} - \alpha_3 x_3^{(k)} - \alpha_4 x_4^{(k)} - \alpha_5 x_5^{(k)} \right)^2$$

where the sum is over our family of inductors (so $N \approx 19000$). It is also possible to use more sophisticated data-fitting techniques, e.g., one which minimizes the maximum error of the fit, or one in which the coefficients must satisfy given inequalities or bounds.

Since the monomial expression L_{mon} is developed from our library of inductors, it is important to check that it has predictive ability as well, by checking its error on inductors not in the library. Such tests reveal that the fit for such inductors is as good as the fit for the ones in the family from which the model was developed. This is hardly surprising since the fitting method compresses 19 000 numbers (i.e., the inductances) to six (i.e., the monomial coefficients), and so is not prone to “over-fitting.”

The monomial expression is useful since, like the other expressions, it is very accurate and very simple. Its real use, however, is that it can be used for optimal design of inductors and circuits containing inductors, using *geometric programming*, which is a type of optimization problem that uses monomial models [16].

III. COMPARISON TO FIELD SOLVERS

In this section we analyze the error distributions of our expressions as well as previously published expressions by comparing them to the inductance computed using the field solver ASITIC.

Fig. 3(a) shows the error distributions of previously reported expressions, when compared to the inductance computed using the field solver ASITIC [7]–[10]. We define the absolute percentage error of an approximation \hat{L} of an inductance L as $100|\hat{L}-L|/L$. The horizontal axis gives an absolute percentage error level, and the vertical axis shows the fraction of inductors (out of a family of 19 000) with error exceeding the specified level. Roughly speaking, the closer the error distribution curve to the y axis, the more accurate the expression. We can determine several important statistics from the curves. By following the horizontal line at the 50% level, we can read off the median error for each approximation. By following a vertical line at some level of error we can find the fraction of inductors for which the approximation was at least that accurate. The maximum error is given by the point where the curve hits the x axis. Consider, for example, the solid curve

TABLE IV
COMPARISON OF MEASURED INDUCTANCE VALUES WITH FIELD SOLVER INDUCTANCE VALUES AND THE VARIOUS APPROXIMATE EXPRESSIONS

Inductor #	Source	sides	n	d_{out}	w	s	L_{meas}	e_{ast}	e_{whe}	e_{gmd}	e_{mon}
1	1	4	2.75	344	29.7	1.9	3.20	3.1	5.2	6.4	3.6
2	1	4	3.75	292	13.0	1.9	6.00	-1.7	-1.2	-0.7	-0.4
3	1	4	6.50	217	5.4	1.9	12.50	2.4	1.4	2.3	4.9
4	1	4	2.75	279	18.3	1.9	3.10	0.0	2.1	2.8	1.4
5	1	4	4.75	206	7.8	1.9	6.10	0.0	-0.7	0.3	2.0
6	1	4	7.50	166	3.2	1.9	12.40	4.0	2.2	3.2	5.5
7	1	4	9.50	153	1.8	1.9	18.20	2.7	0.8	1.9	2.7
8	1	4	2.75	277	18.3	0.8	3.10	0.0	0.8	1.3	-2.0
9	1	4	2.75	307	18.3	18.0	2.90	10.3	13.5	14.6	12.4
10	1	4	3.75	321	16.5	1.9	6.10	0.0	0.2	1.1	0.7
11	1	4	7.75	225	4.4	1.9	18.10	0.6	-0.9	0.0	2.9
12	1	4	3.75	193	9.1	1.9	4.00	7.5	6.6	7.5	8.4
13	1	4	5.00	171	5.4	1.9	6.10	4.9	3.0	3.8	5.8
14	1	4	3.25	400	31.6	1.9	4.90	4.1	7.2	8.3	5.9
15	1	4	5.75	339	10.0	1.9	16.20	3.7	2.0	2.7	4.5
16	1	4	12.00	180	3.2	2.1	20.50	2.0	-1.0	-0.4	3.9
17	1	4	7.00	300	13.0	7.0	8.00	5.0	5.6	4.0	9.1
18	[2]	4	6.00	400	24.0	7.0	8.00	8.8	9.2	7.6	12.6
19	[2]	4	8.00	300	5.0	4.0	22.10	-6.3	-9.6	-8.3	-7.6
20	[2]	4	4.00	300	5.0	4.0	9.20	-5.4	-3.3	-7.2	-6.4
21	[18]	4	9.00	210	6.5	5.5	7.70	2.6	8.0	4.5	11.8
22	[18]	4	8.00	226	6.0	6.0	9.00	-1.1	-1.0	-1.4	0.7
23	[5]	4	11.00	300	9.0	4.0	15.50	-11.6	-9.7	-12.4	-3.2
24	[5]	4	8.00	300	14.0	4.0	8.30	-8.4	-6.7	-9.5	-0.9
25	[5]	4	6.00	300	19.0	4.0	5.10	-7.8	-7.2	-9.1	-2.8
26	[5]	4	3.00	300	19.0	4.0	3.30	-6.1	-7.2	-6.1	-6.5
27	[5]	4	5.00	300	24.0	4.0	3.50	-5.7	-5.2	-7.3	-1.6
28	[5]	4	9.00	230	6.5	5.5	9.70	1.0	2.3	0.6	5.6
29	[5]	4	16.00	300	5.0	4.0	34.00	-7.6	-4.2	-6.9	1.6
30	[5]	4	6.00	300	9.0	4.0	11.70	-5.1	-7.8	-6.5	-4.9
31	[5]	4	3.00	300	9.0	4.0	5.50	5.5	6.3	3.7	4.8
32	[5]	4	4.00	300	14.0	4.0	5.80	-1.7	-4.4	-3.2	-2.6
33	[5]	4	2.00	300	14.0	4.0	2.90	17.2	18.0	15.0	15.5
34	[5]	4	2.00	300	19.0	4.0	2.50	16.0	16.0	15.0	14.5
35	[5]	4	3.00	300	24.0	4.0	3.10	9.7	5.9	7.1	6.5
36	[19]	4	5.00	154	7.0	5.0	3.00	6.7	3.9	4.3	5.8
37	[19]	4	9.00	250	7.0	5.0	12.00	-0.8	0.2	-0.5	3.7
38	[13]	4	6.00	285	15.0	3.0	6.70	-7.5	-9.4	-9.1	-5.6
39	[13]	4	3.50	255	10.0	1.5	5.00	-4.0	-4.5	-5.2	-4.4
40	[13]	4	4.50	216	10.0	1.5	5.00	-6.0	-7.8	-6.6	-5.4
41	[13]	4	5.50	199	10.0	1.5	5.00	-6.0	-9.3	-8.2	-5.8
42	[13]	4	6.50	191	10.0	1.5	5.00	-6.0	-8.1	-8.1	-3.6
43	[10]	4	7.50	190	10.0	1.5	5.00	-10.0	-8.5	-10.4	-2.8
44	[20]	4	9.25	145	5.2	2.0	6.00	-3.3	-5.2	-7.0	1.3
45	[20]	4	6.75	290	13.0	7.0	7.10	1.4	3.5	2.0	7.0
46	[20]	4	2.50	290	13.0	7.0	3.00	-3.3	-2.5	-3.3	-3.4
47	[21]	4	3.25	340	25.0	6.0	3.30	-9.1	-12.1	-10.8	-11.0
48	[21]	4	4.50	300	23.0	6.0	3.40	-2.9	-4.3	-5.1	-1.4
49	[21]	4	3.00	300	18.0	6.0	3.30	-3.0	-5.9	-4.7	-5.0
50	[21]	4	5.75	190	9.5	6.0	3.40	0.0	2.5	1.1	5.6
51	[21]	4	3.00	700	90.0	6.0	3.70	-5.4	-4.9	-5.4	-6.7
52	[22]	4	4.00	262	16.0	10.0	2.60	-19.2	-19.9	-19.5	-18.5
53	[22]	4	6.00	392	16.0	10.0	8.80	-11.4	-12.6	-12.4	-10.5
54	[22]	4	8.00	532	16.0	10.0	20.40	-16.7	-17.3	-17.1	-14.6
55	[23]	8	4.00	346	18.0	2.0	5.90	0.0	-1.1	-1.6	-3.6
56	[23]	8	5.00	346	18.0	2.0	7.50	2.7	2.7	0.7	0.3
57	[23]	8	4.00	326	8.0	12.0	5.60	-7.1	-7.7	-7.8	-11.8
58	[23]	8	5.00	326	8.0	12.0	7.20	-2.5	-1.0	-2.8	-5.6
59	[12]	12	6.75	197	8.2	3.0	5.45	1.8	-	1.5	-
60	[12]	12	8.00	198	7.5	3.0	6.30	-0.5	-	-1.8	-
61	[12]	12	7.75	198	6.5	3.0	7.30	-1.9	-	-2.2	-

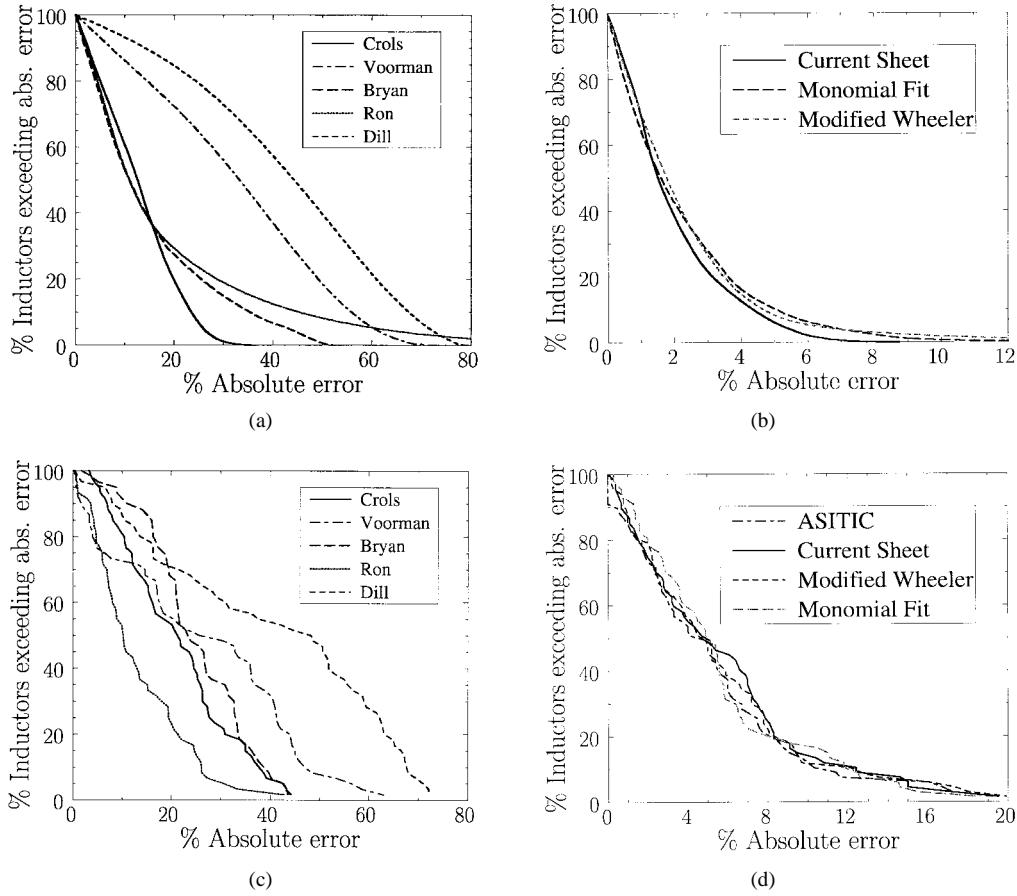


Fig. 3. Error distributions for: (a) previous expressions versus field solver simulations, (b) new expressions versus field solver simulations, (c) previous expressions versus measurements, and (d) new expressions versus measurements.

which corresponds to Crols' expression. The median error is about 18%; we can also see that the maximum error is around 25%. All of the expressions described above have significant mean offset errors, i.e., they tend to over or underestimate inductance. However, even if the expressions are scaled to zero mean error (by multiplying each by a constant correction factor or adding a fixed offset) the errors are still typically around 15–20%, and in some cases larger.

Fig. 3(b) shows the absolute error distributions for our expressions, using the same format as in Fig. 3(a), but with a different horizontal scale since the errors here are smaller. The plots show that the typical errors are in the 1–2% range, and most of the errors are smaller than 3%, almost an order of magnitude smaller than the previously published expressions shown in Fig. 3(a). Our expressions for inductance, while comparable in complexity to the previously reported expressions, exhibit substantially better accuracy.

IV. MEASUREMENT RESULTS

In this section, we compare the inductance values predicted by all the approximate expressions with 60 measured inductance values. In Table IV we compare the measured inductance values with those predicted by the various expressions. The first fifteen inductors shown in Table IV were fabricated using the top metal level (of thickness 0.9 μm) of a 0.35 μm CMOS process. The data for the remaining inductors were

obtained from previously published work. The first column in Table IV gives the inductor number; the second column shows the source of the inductor data; the third column shows the number of sides; the fourth is the number of turns (n); the fifth, sixth, and seventh columns are the outer diameter (d_{out}) turn width (w) and spacing (s) in μm ; the eighth column shows the measured or reported value of the inductance (L_{meas}) in nH. In the ninth column we give the percent relative error between L_{meas} and (L_{asi} predicted by ASITIC), which we define as $e_{\text{meas}} = 100(L_{\text{meas}} - L_{\text{asi}})/L_{\text{meas}}$. In the final three columns we give the corresponding relative errors e_{whe} , e_{gnd} , and e_{mon} for our inductance expressions (1), (2), and (3), respectively.

We observe close agreement between our expressions and the measured data, with larger errors for the smaller inductors. The reason, as explained in [17], is that the parasitic inductance inherent in the measurement setup results in large relative errors for low inductance values.

Fig. 3(c) compares the experimental values to the inductances predicted by previously published expressions, while Fig. 3(d) compares the experimental values to the inductance predicted by our formulas as well as ASITIC. Once again, it is clear that our expressions exhibit much smaller errors compared to the previous ones. It is also interesting to note how well the predictions of ASITIC compare to our expressions. This is particularly of interest in those few cases where the errors between experiment and our expressions approach

20%, which suggests substantial measurement errors, either in calibration or parameter extraction. More important, it is clear that our expressions perform as well as a field solver.

We can also put the accuracy of our formulas in the context of other variations and uncertainties in a spiral inductor. A major limitation in the design, modeling, and simulation of spirals is the uncertainty in the oxide thickness due to process variations. Process variations can cause the parasitic capacitances in the inductor model to vary by around 5–10%. These variations translate to an uncertainty in the impedance of the spiral that is of the same order of magnitude as the errors introduced by our expressions. This limitation suggests that inductance expressions with better accuracies than what we have achieved are not necessary and that our expressions are acceptable for use in circuit design and optimization.

V. CONCLUSIONS

In this paper, we have presented three simple, approximate expressions for spiral inductors of square, hexagonal, octagonal, and circular geometries. The first expression, called the modified Wheeler expression, is obtained by modifying an expression that Wheeler obtained for discrete inductors. This expression is simple and gives very good accuracy. The second expression is derived from electromagnetic principles by approximating the sides of the spiral by current sheets with uniform current distribution. This expression is intuitive and similar in form to inductance expressions for more conventional elements such as coaxial transmission lines and parallel wire transmission lines. The third expression is obtained by data-fitting techniques. Although it lacks the physically intuitive derivation of the other two approximations, it is very well suited for optimization of circuits using geometric programming.

All three expressions match field solver simulations well, with typical errors of 1–2%, and most errors smaller than around 3%. This represents a great improvement over previously published expressions, which have typical errors of around 20% or more. When compared to experimental data, the errors of our three expressions are comparable to the errors of a field solver, which suggests that the errors may be due, at least in part, to measurement error. The simplicity, versatility, and robustness of our expressions make them good candidates for circuit design and optimization applications. They can be included in a physical, scalable lumped-circuit model for spiral inductors, where, in addition to providing design insight, they allow efficient optimization schemes to be employed.

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REFERENCES

- [1] E. Pettenpaul, H. Kapusta, A. Weisberger, H. Mampe, J. Luginsland, and I. Wolff, "CAD models of lumped elements on GaAs up to 18 GHz," *IEEE Trans. Microwave Theory Tech.*, vol. 36, pp. 294–304, Feb. 1988.
- [2] C. P. Yue, C. Ryu, J. Lau, T. H. Lee, and S. S. Wong, "A physical model for planar spiral inductors on silicon," in *Proc. IEEE Int. Electron Devices Meeting*, San Francisco, CA, 1996.
- [3] R. B. Merrill, T. W. Lee, H. You, R. Rasmussen, and L. AS. Moberly, "Optimization of high Q integrated inductors for multilevel metal CMOS," in *Proc. IEEE Int. Electron Devices Meeting*, Washington, DC, 1995, pp. 38.7.1–38.7.4.
- [4] *MagNet 5 user guide: Using the MagNet version 5 package from Infolytica*, E. M. Freeman, Infolytica Corp., Montreal, P.Q., Canada, 1993.
- [5] K. B. Ashby, I. A. Koullias, W. C. Finley, J. J. Bastek, and S. Moinian, "High Q inductors for wireless applications in a complementary silicon bipolar process," *IEEE J. Solid-State Circuits*, vol. 31, pp. 4–9, Jan. 1996.
- [6] H. M. Greenhouse, "Design of planar rectangular microelectronic inductors," *IEEE Trans. Parts, Hybrids, Packaging*, vol. PHP-10, pp. 101–109, June 1974.
- [7] J. Crols, P. Kinget, J. Craninckx, and M. Steyeart, "An analytical model of planar inductors on lowly doped silicon substrates for analog design up to 3 GHz," presented at the Symp. VLSI Circuits, Dig. Tech. Papers, Honolulu, HI, 1996, pp. 28–29.
- [8] J. O. Voorman, *Continuous-Time Analog Integrated Filters*. Piscataway, NJ: IEEE Press, 1993.
- [9] H. G. Dill, "Designing inductors for thin-film applications," *Electron. Design*, vol. 12, no. 4, pp. 52–59, 1964.
- [10] H. Ronkainen, H. Kattelus, E. Tarvainen, T. Riihisaari, M. Anderson, and P. Kuivalainen, "IC compatible planar inductors on silicon," in *IEEE Proc. Circuits Devices Syst.*, Feb. 1997, vol. 144, no. 1, pp. 29–35.
- [11] H. A. Wheeler, "Simple inductance formulas for radio coils," in *Proc. IRE*, Oct. 1928, vol. 16, no. 10, pp. 1398–1400.
- [12] A. M. Niknejad and R. G. Meyer, "Analysis, design and optimization of spiral inductors and transformers for Si RF IC's," *IEEE J. Solid-State Circuits*, vol. 33, pp. 1470–1481, Oct. 1998.
- [13] J. R. Long and M. A. Copeland, "The modeling, characterization, and design of monolithic inductors for Silicon RF IC's," *IEEE J. Solid-State Circuits*, vol. 32, pp. 357–369, Mar. 1997.
- [14] E. B. Rosa, "Calculation of the self-inductances of single-layer coils," *Bull. Bureau Standards*, vol. 2, no. 2, pp. 161–187, 1906.
- [15] J. C. Maxwell, *A Treatise on Electricity and Magnetism*, 3rd ed. New York: Dover, 1967.
- [16] M. Hershenson, S. S. Mohan, S. P. Boyd, and T. H. Lee, "Optimization of inductor circuits via geometric programming," in *Design Automation Conf.*, New Orleans, LA, June 1999, pp. 994–998.
- [17] N. M. Nguyen and R. G. Meyer, "Si IC-compatible inductors and LC passive filters," *IEEE J. Solid-State Circuits*, vol. 25, pp. 1028–1031, Aug. 1990.
- [18] J. N. Burghartz, K. A. Jenkins, and M. Soyuer, "Multilevel-spiral inductors using VLSI interconnect technology," *IEEE Electron Device Lett.*, vol. 17, pp. 428–430, Sept. 1996.
- [19] A. M. Niknejad and R. G. Meyer, "Analysis and optimization of monolithic inductors and transformers for RF IC's," in *Proc. IEEE CICC'97*, Santa Clara, CA, 1997, pp. 16.3.1–16.3.4.
- [20] S. S. Mohan, C. P. Yue, M. Hershenson, T. H. Lee, and S. S. Wong, "Modeling and characterization of on-chip transformers," in *Proc. IEEE Int. Electron Devices Meeting*, San Francisco, CA, Dec. 1998, pp. 531–534.
- [21] P. Basedau and Q. Huang, "A 1 GHz monolithic oscillator in $1\mu\text{m}$ CMOS," in *Proc. Eur. Solid-State Circuits Conf.*, Ulm, Germany, 1994.
- [22] D. Eggert *et al.*, "A SOI-RF-CMOS technology on high resistivity SIMOX substrates for microwave applications to 5 GHz," *IEEE Trans. Electron Devices*, vol. 44, pp. 1981–1989, 1997.
- [23] U. Normak, *Integrated Transformer*. Kista, Sweden: KTH Kista, 1998.