A Constant-Frequency Method for Improving Light-Load Efficiency in Synchronous Buck Converters

Michael D. Mulligan, Bill Broach, and Thomas H. Lee

***Abstract*—The low-voltage synchronous rectifier buck topology suffers from low efficiency at light loads due to dissipation that does not scale with load current. In this paper we present a method for improving light-load efficiency in synchronous buck converters by reducing gate drive losses. We propose a new gate drive technique whereby the gate voltage swing dynamically scales with load current such that gate drive loss is traded for conduction loss. Since conduction losses scale with the square of load current, an optimal gate swing exists that, at light loads, is shown to be less than the supply voltage. Using this method we obtain a 6.25% increase in converter efficiency at a load current of 10 mA and operating at a constant switching frequency of 2 MHz.**

***Index Terms*—DC–DC power conversion, gate charge modulation, light-load efficiency, low power, low swing.**

I. Introduction

THE GROWTH of the portable electronics industry has demanded improvements in dc–dc converter technology in order to increase battery lifetime and enable smaller, cheaper systems. For example, brighter, full-color displays and a demand for increased talk-time in cellular phones has placed power consumption at a premium. Since many portable devices operate in low-power standby modes for a majority of the time they are on, increasing light-load converter efficiency can significantly increase battery lifetime.

The synchronous rectifier buck converter (SRBC) is popular for low-voltage power conversion because of its high efficiency and reduced area consumption [1], [2]. Shown in Fig. 1, this topology uses complementary switches to transfer energy to the filter inductance from the power source. High switching frequencies (e.g., 1–2 MHz) are preferred in order to reduce the size of the off-chip LC filter components. Unfortunately, such switching speeds exacerbate frequency-dependent losses, especially as the load current is reduced, resulting in a substantial reduction in converter efficiency.

Many techniques have been developed in an attempt to mitigate this effect. Included among these are resonant gate drive [3]–[5], pulse frequency modulation (PFM) [6], and a hybrid control scheme [7] whereby at heavy loads the converter operates in standard pulse-width modulated (PWM) fashion, but at light loads switches to PFM mode. The primary drawbacks of these methods are the complexity of their implementation and, in the case of the variable-frequency methods, their potential for generating undesired noise at subharmonics of the switching frequency. In many systems, especially those for audio applications, subharmonic noise can result in severe degradation in signal quality. Furthermore, hybrid controllers can provoke relatively large output voltage transients when switching between PWM and PFM control modes.

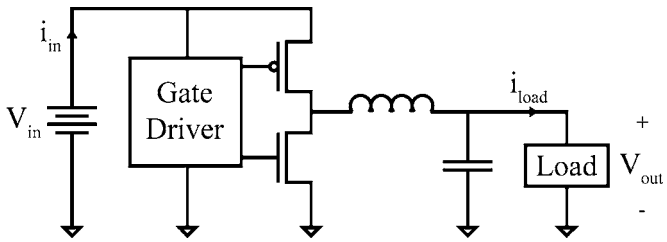

Fig. 1. Synchronous rectifier buck converters are a ubiquitous building block in portable systems.

In this paper, we propose a method for reducing gate drive losses at light loads. We show that the optimal gate drive voltage is load-dependent, and that by modulating the amount of charge deposited on the gates of the MOS switches we can affect an increase in light-load efficiency. This is done in standard PWM fashion and therefore results in neither large voltage transients due to mode-hopping nor subharmonic noise at the output.

II. Light-Load Efficiency Problem

The basic operation of the SRBC is well documented in the literature (see, e.g., [8]). As the converter load current varies over its full range, the relative contributions of individual loss mechanisms to power dissipation vary as well. Fig. 2 shows the percent contribution for the various losses in a typical converter over a two-decade load range. At heavy loads conduction loss in the channels of the MOS power devices dominates the power dissipation. Conversely, the power dissipation at light loads is dominated by loss mechanisms that do not scale with load current. The most prominent of these is gate drive loss.

III. Gate Charge Modulation

The contrary dependence of conduction loss and gate drive loss on gate voltage swing indicates the existence of an optimum

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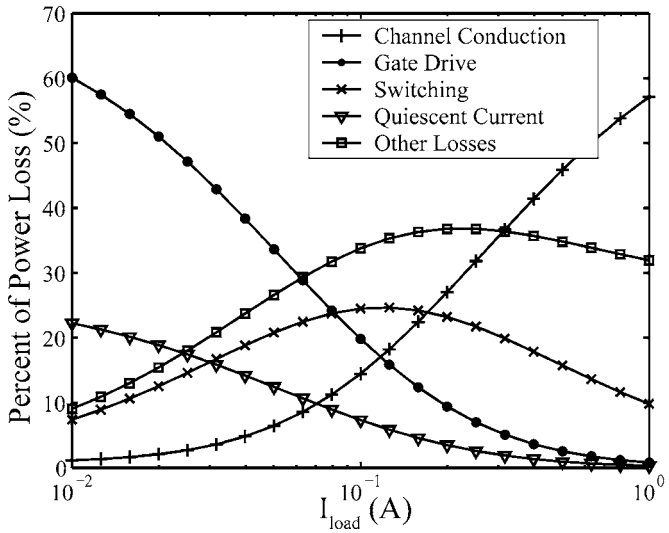

Fig. 2. Plot of the percent contributions to total converter power dissipation for the various loss mechanisms.

load-dependent gate drive voltage for each power device. Previous efforts have shown that a *static* reduced gate voltage swing improves light-load efficiency [8], [9]. Our work differs in that we take advantage of the fact that the optimal voltage swing, as will be shown, scales with load. By *dynamically* scaling the gate swing to improve light-load efficiency, we can extend the usable load current range in high-frequency, low-power SRBCs.

In this section we outline the concept of gate charge modulation (GCM), whereby gate drive loss is traded for conduction loss to achieve maximum efficiency. First, we derive expressions for the optimal NMOS and PMOS gate voltage swings. Then, we discuss our circuit implementation of the GCM driver.

A. Optimal Gate Voltage Swing

Gate charge modulation exploits a tradeoff between conduction loss and gate drive loss that results in a significant increase in converter efficiency at light loads. The efficiency of an SRBC can be represented by the following expression

$$\eta = 1 - \frac{P_{loss}}{P_{in}} \tag{1}$$

where P_{in} and P_{loss} are the input power and the power consumption of the converter, respectively. P_{loss} is the sum of many different loss mechanisms and can be expressed as

$$P_{loss} = P_{cond,p} + P_{cond,n} + P_{gate,p} + P_{gate,n} + P_0. \tag{2}$$

Here, P_{cond} and P_{gate} are the conduction and gate drive losses, respectively, and P_0 represents all losses that do not depend directly on the gate voltage of the power devices. The subscripts p and n are used to differentiate the p-type and n-type power devices. P_{cond} and P_{gate} can be expressed as

$$\begin{aligned} P_{cond,p} &= I_{rms,p}^2 R_{DS(on),p} \\ P_{cond,n} &= I_{rms,n}^2 R_{DS(on),n} \end{aligned} \tag{3}$$

and

$$\begin{aligned} P_{gate,p} &= C_{gate,p} V_{in} V_{swing,p} f_{sw} \\ P_{gate,n} &= C_{gate,n} V_{in} V_{swing,n} f_{sw}. \end{aligned} \tag{4}$$

The gate drive loss shown in (4) assumes that the reduced-swing gate voltage is derived either from a properly timed deposition of gate charge or from a secondary power supply that is linearly regulated. This result, as well as a more general result, is derived in the Appendix.

In (3) and (4), I_{rms} is the RMS current in the device channels, C_{gate} is a linear approximation of device gate capacitance, V_{swing} is the gate voltage swing, f_{sw} is the converter switching frequency, and $R_{DS(on)}$ is the effective channel resistance of the power devices when they are conducting. A first-order analysis of $R_{DS(on)}$ for the CMOS devices yields the following well-known equations:

$$\begin{aligned} R_{DS(on),p} &\approx \left[k_p \left(V_{swing,p} - |V_{Tp}|\right)\right]^{-1} \\ R_{DS(on),n} &\approx \left[k_n \left(V_{swing,n} - V_{Tn}\right)\right]^{-1} \end{aligned} \tag{5}$$

where

$$\begin{aligned} k_p &= \mu_p C_{ox} \frac{W_p}{L_p} \\ k_n &= \mu_n C_{ox} \frac{W_n}{L_n}. \end{aligned} \tag{6}$$

Again, the subscripts p and n differentiate the PMOS and NMOS device types, respectively. In (5) the drain-source voltage has been assumed to be negligible compared to the overdrive voltage.

Substituting (2) through (6) into (1), we obtain the following expression for efficiency:

$$\eta = 1 - \frac{1}{P_{in}} \left[V_{in} f_{sw} (C_{gate,p} V_{swing,p} + C_{gate,n} V_{swing,n}) + \frac{I_{rms,p}^2}{k_p \left(V_{swing,p} - |V_{Tp}|\right)} + \frac{I_{rms,n}^2}{k_n (V_{swing,n} - V_{Tn})} + P_0 \right]. \tag{7}$$

Fig. 3 shows several plots of predicted efficiency versus $V_{swing,p}$ and $V_{swing,n}$ of a typical SRBC with $V_{in} = 3.6$ V and $V_{out} = 1.8$ V, and load values of 10 mA, 35 mA, 100 mA, and 350 mA. It is clear that for lighter loads the optimal voltage swings deviate greatly from the conventional value of V_{in}.

To solve for the optimal gate swings analytically, we maximize (7) with respect to $V_{swing,p}$ and $V_{swing,n}$, and account for the upper bound imposed by the available supply voltage, V_{in}. This results in the following expressions for optimal gate voltage swing for the PMOS and NMOS devices:

$$\begin{aligned} V_{swing,p,opt} &= \min\left(V_{in}, \sqrt{\frac{I_{rms,p}^2}{k_p C_{gate,p} V_{in} f_{sw}}} + |V_{Tp}|\right) \\ V_{swing,n,opt} &= \min\left(V_{in}, \sqrt{\frac{I_{rms,n}^2}{k_n C_{gate,n} V_{in} f_{sw}}} + V_{Tn}\right). \end{aligned} \tag{8}$$

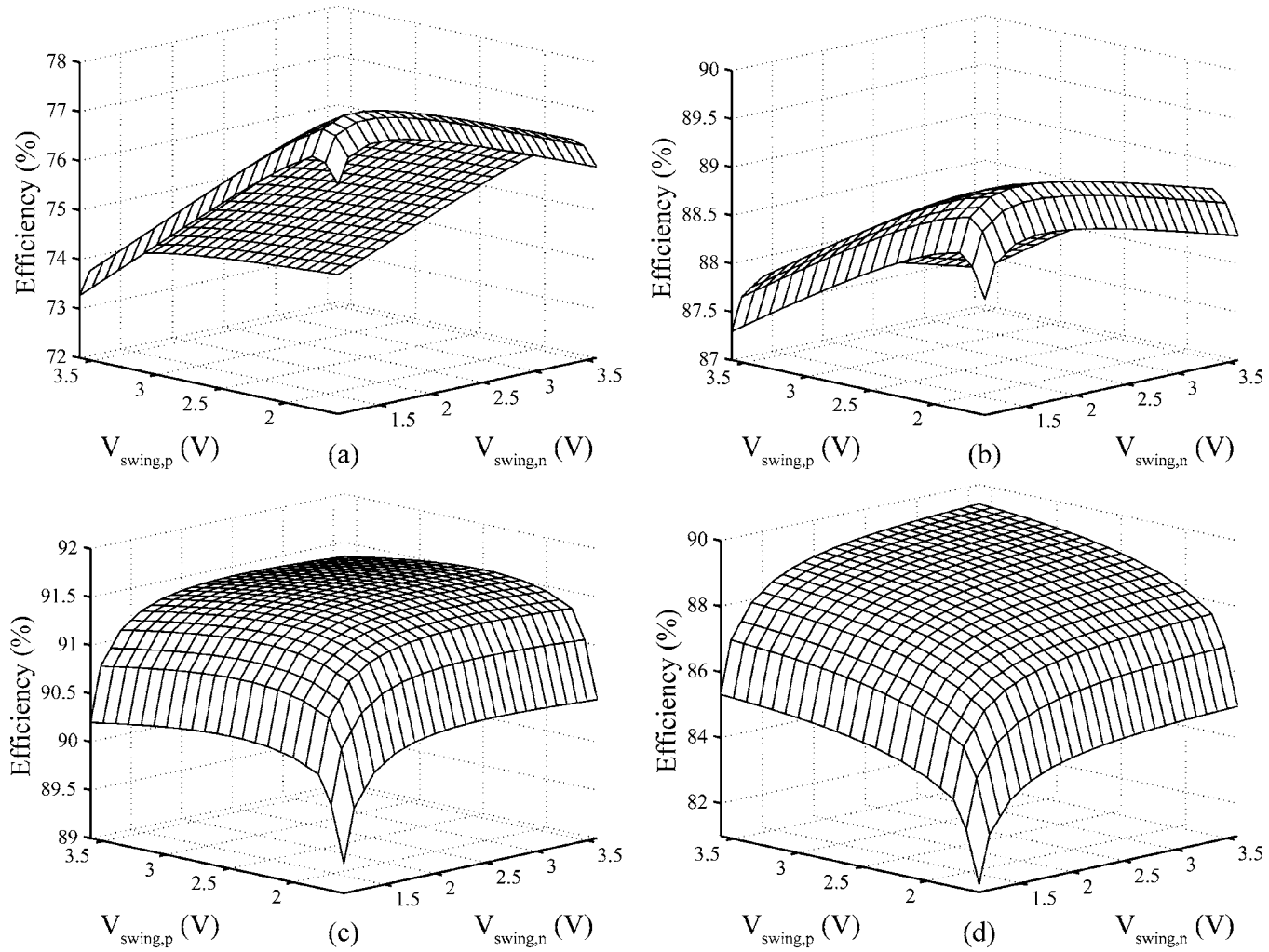

Fig. 3. Plots of simulated efficiency versus gate swing for I_{load} equal to (a) 10 mA, (b) 35 mA, (c) 100 mA, and (d) 350 mA.

Assuming linear transitions between maximum and minimum inductor current, I_{rms} for an SRBC operating in continuous conduction mode (CCM) is given as

$$I_{rms,p} = \sqrt{D\left(I_{load}^2 + \frac{\Delta i^2}{3}\right)}$$
$$I_{rms,n} = \sqrt{(1-D)\left(I_{load}^2 + \frac{\Delta i^2}{3}\right)} \quad (9)$$

where Δi is the peak-to-peak inductor current ripple. In discontinuous conduction mode (DCM), I_{rms} is given as

$$I_{rms,p} = \sqrt{\frac{I_{peak}^3 f_{sw} L}{3(V_{in} - V_{out})}}$$
$$I_{rms,n} = \sqrt{\frac{I_{peak}^3 f_{sw} L}{3V_{out}}} \quad (10)$$

where I_{peak} is the peak current through the filter inductor. In DCM, I_{peak} can be shown to be related to I_{load} via the following expression:

$$I_{peak} = \sqrt{\frac{2I_{load}V_{out}(V_{in} - V_{out})}{V_{in} f_{sw} L}}. \quad (11)$$

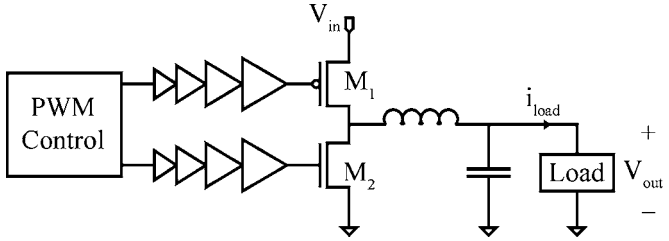

Fig. 4. Conventional gate driver using tapered buffers to drive the large CMOS power devices.

B. Circuit Implementation

A conventional gate driver for a SRBC, shown in Fig. 4, consists of several stages of tapered inverters, increasing in size nearer to the power MOSFET. The initial PWM signal is divided into separate high-side and low-side switch drive signals, $V_{drive,p}$ and $V_{drive,n}$, such that these signals are nonoverlapping, avoiding excessive power dissipation that would result from current shoot-through when both MOSFETs are conducting simultaneously.

Our gate driver, shown in Fig. 5, is similar to the conventional SRBC driver. However, in order to implement gate charge

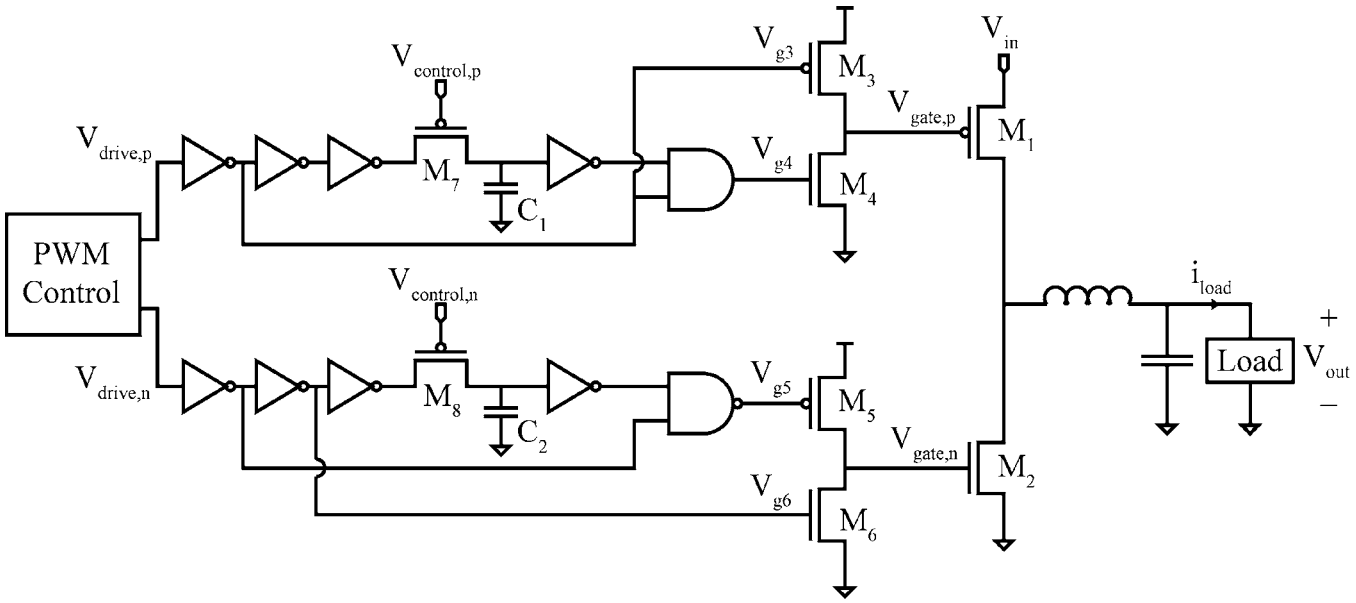

Fig. 5. Gate charge modulation (GCM) gate driver using a voltage-controlled RC delay to vary the gate swing of the CMOS power devices.

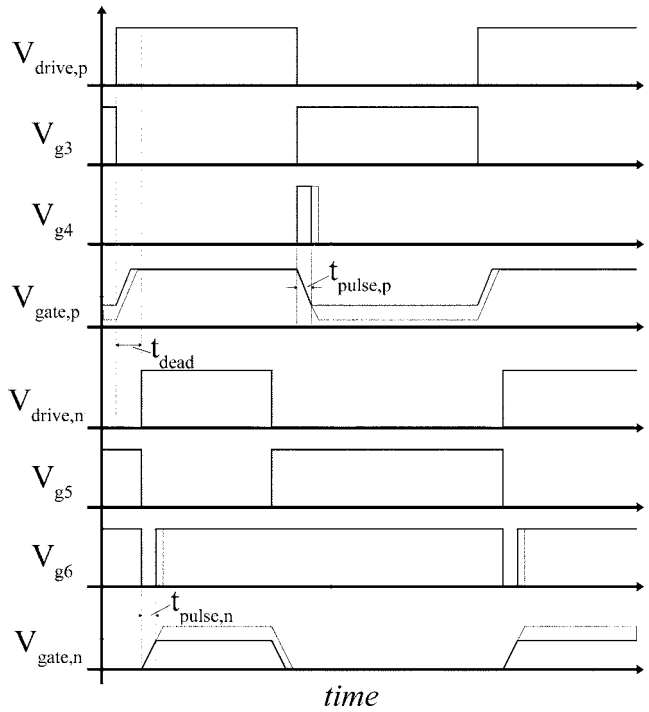

Fig. 6. Timing diagram corresponding to signals in Fig. 5. The top four axes correspond to the PMOS gate drive, the bottom four to the NMOS. The shaded regions illustrate how changes in pulse widths $t_{pulse,p}$ and $t_{pulse,n}$ modulate the gate swings $V_{gate,p}$ and $V_{gate,n}$, respectively.

modulation, we employ a voltage-controlled timed charge deposition technique. The initial PWM signal is again divided into two nonoverlapping gate-drive signals, $V_{drive,p}$ and $V_{drive,n}$. As illustrated in Fig. 6, when $V_{drive,p}$ goes HIGH, M_3 turns on and forces $V_{gate,p}$ HIGH, turning off the PMOS power device M_1. When $V_{drive,p}$ goes LOW, M_3 turns off and M_4 turns on. The amount of time M_4 conducts is governed by the effective RC time-constant of the $M_7 - C_1$ pair. Shown in Fig. 7, increasing $V_{control,p}$ increases the propagation delay through the $M_7 - C_1$ path, in turn increasing the characteristic pulse width $t_{pulse,p}$ as well as the gate swing $V_{swing,p}$. The process is similar for switching the NMOS power device.

In an autonomous system, $V_{control,p}$ and $V_{control,n}$ would be derived from knowledge of the load. Local feedback could be used to linearize the $V_{gate}/V_{control}$ relationship, and (8) would yield the working system design parameters for generating the control signals. For purposes of this work, $V_{control,p}$ and $V_{control,n}$ were left as independent characterization inputs.

It should be noted that the use of timed gate charge deposition has the benefit of requiring no secondary internal voltage supplies and can be implemented with very low power static logic elements, making it a very power efficient method for modulating V_{swing}.

IV. Efficiency Results

The filter inductance and capacitance used are 10 μH and 10 μF, respectively, and the integrated CMOS power devices have gate widths of 60 mm for the PMOS device and 21 mm for the NMOS device. Both are minimum length devices ($L_{min} = 0.5\ \mu\text{m}$). Fig. 8 shows plots of efficiency versus load current for both the full-swing and optimal-swing conditions. Also shown are efficiency plots obtained when GCM is applied to either the PMOS or the NMOS power devices separately (PMOS-only and NMOS-only curves, respectively), with the non-GCM enhance device being driven rail-to-rail. The optimal curves were obtained by sweeping $V_{control,p}$ and $V_{control,n}$ at selected load values until the maximum efficiency value is found. The plot of typical efficiency was obtained by setting $V_{control,p} = V_{control,n} = V_{in}$ to achieve rail-to-rail gate drive.

For $I_{load} = 10$ mA and $f_{sw} = 2$ MHz, GCM provides an increase of 6.25% over the conventional full-swing driver. It should be mentioned that the efficiencies achieved by our design were lower than expected. After testing, we expect that this is due to a dead-time that is much shorter than was designed

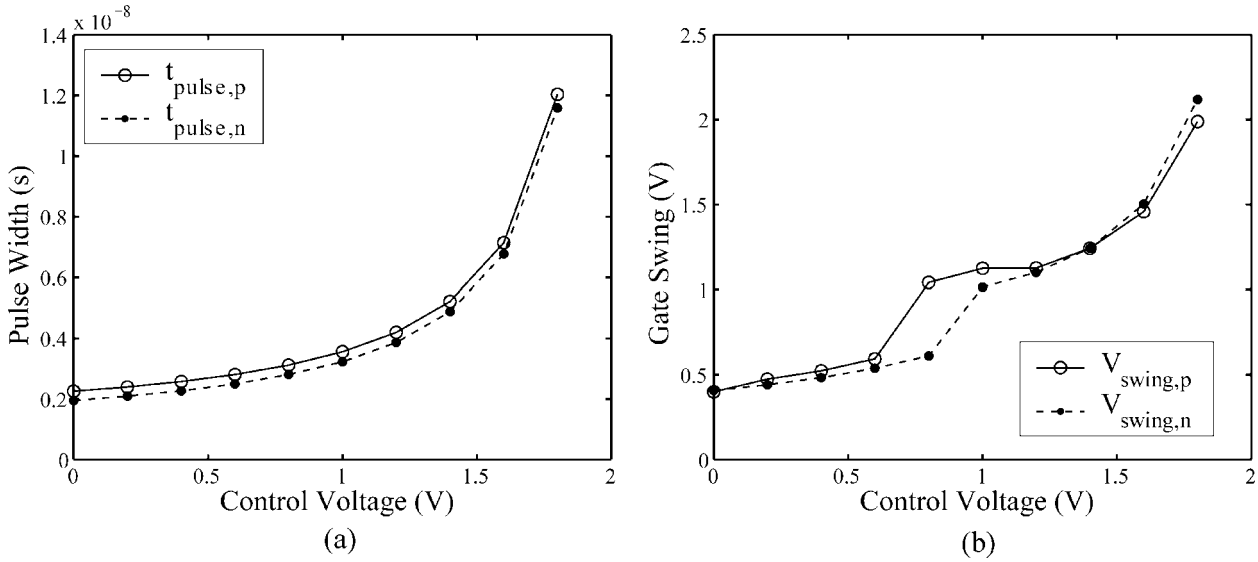

Fig. 7. Simulation results showing (a) t_{pulse} and (b) V_{swing} versus $V_{control}$ for both PMOS and NMOS power devices.

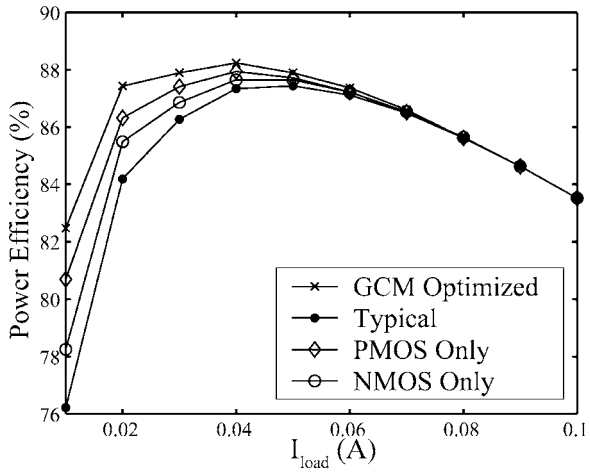

Fig. 8. Measured efficiency versus load current for $f_{sw} = 2$ MHz, $V_{in} = 3.6$ V, and $V_{out} = 1.8$ V.

for, resulting in nonnegligible shoot-through current. The relative increase in efficiency resulting from GCM is expected to increase when this design error is corrected.

V. Conclusion

By dynamically scaling the gate voltage swings of large, integrated MOS power devices, light-load efficiency can be improved and the usable load current range extended in synchronous rectifier buck converters. We have shown that the optimal voltage swing is a strong function of load current, I_{load}, both in CCM and DCM. By applying the GCM technique we were able to improve converter efficiency to greater than 80% at $I_{load} = 10$ mA while still maintaining greater than 80% efficiency at $I_{load} = 100$ mA.

Appendix

In this section, we provide a formal derivation for (4), as well as a more general equation for reduced-swing gate drive power loss. The general equation for the average power dissipation of the gate driver is

$$P_{loss} = \frac{1}{T}\int_0^T i_{in}(t)v_{in}(t)dt = \frac{V_{in}}{T}\int_0^{t_1} i_{in}(t)dt \tag{12}$$

where t_1 is the time the PMOS device is conducting, sinking current from the power supply whose voltage, V_{in}, is constant. The switching of the gate capacitance is governed by the equation

$$\int_0^{t_1} i_{in}(t)dt = C_{gate}\int_{v_{gate}(0)}^{v_{gate}(t_1)} dv_{gate} = C_{gate}(v_{gate}(t_1) - v_{gate}(0)). \tag{13}$$

By setting $V_{swing} = v_{gate}(t_1) - v_{gate}(0)$ and $f_{sw} = 1/T$, and substituting (13) into (12), we have

$$P_{loss} = C_{gate}V_{in}V_{swing}f_{sw}. \tag{14}$$

Typically, $V_{swing} = V_{in}$, yielding the well-known CV^2f relation. If we instead assume that, though the gate voltage is derived from the primary power supply, the swing is reduced by timed gate charge deposition, (14) accurately describes the gate drive power loss.

Another method for reducing gate swing is by driving the power device from a variable secondary supply voltage, which we will again call V_{swing}. In this case power dissipation appears to be given by

$$P_{loss} = C_{gate}V_{swing}^2 f_{sw}. \tag{15}$$

But because the secondary supply must be derived from the primary power source, the total gate drive power loss P_{total} must account for any loss incurred in this conversion. Defining power conversion efficiency in the usual way, $\eta = P_{out}/P_{in}$, we see that

$$P_{total} = \frac{C_{gate}V_{swing}^2 f_{sw}}{\eta}. \tag{16}$$

For the case of a linear regulator, $\eta = V_{swing}/V_{in}$, yielding

$$P_{loss} = C_{gate} V_{in} V_{swing} f_{sw}. \quad (17)$$

We see that (14) and (17) are theoretically identical. For a more complete measure of the total power loss, nonidealities in the drivers must be accounted for, as well.

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