An Analytical Compact Circuit Model for Nanowire FET

Bipul C. Paul, *Senior Member, IEEE*, Ryan Tu, Shinobu Fujita, *Member, IEEE*, Masaki Okajima, Thomas H. Lee, *Member, IEEE*, and Yoshio Nishi, *Fellow, IEEE*

***Abstract*—In this paper, we propose a quasi-analytical device model of nanowire FET (NWFET) for both ballistic and drift-diffusion current transport, which can be used in any conventional circuit simulator like SPICE. The closed form expressions for current–voltage (I–V) and capacitance–voltage characteristics are obtained by analytically solving device equations with appropriate approximations. The developed model was further verified with the measured I–V characteristics of an NWFET device. Results show a close match of the model with measured data.**

***Index Terms*—Ballistic transport, compact model, drift-diffusion transport, nanowire FET (NWFET).**

I. Introduction

CONTINUED scaling of transistor sizes into sub-50-nm dimensions has made conventional bulk MOSFET devices vulnerable to severe short-channel effects (SCEs) such as very high leakage current, poor gate control etc. [1], [2]. Various device structures such as double gate fully depleted SOI, trigate, and all around gate structures hence, have been extensively studied to restrict SCEs within a limit while achieving the primary advantages of scaling, i.e., higher performance, lower power, and ever increasing integration density [2]–[4]. Among these devices nanowire FETs (NWFETs) (a realistic implementation of all-around-gate structure) have recently drawn wide research interest due to their excellent SCE immunity compared to other contemporary device structures [5]. The superior current–voltage (I–V) characteristics of NWFETs over other devices have been successfully demonstrated both theoretically and experimentally [6]–[12]. It is also demonstrated that several non-Si materials can be used in NWFETs to achieve higher mobility [6], [8]. Subsequently, a circuit friendly compact model of these devices will further facilitate the study on their prospect in high-performance circuit applications. Although several physical device models are proposed to understand and optimize the characteristics of these devices [6], [13], [14] and are often accurate in predicting the physical behavior of the device, they are, however, not quite efficient for large circuit simulations due to the complexity in solutions, which are mostly numerical. Further, most attempts on nanowire modeling assumed ballistic transport [6], [12], [14], [15] and neglect the more realistic drift-diffusion current conduction. It has been predicted that even in transistors of this kind with channel length below 10 nm, expecting ballistic transport is quite unrealistic. A drift-diffusion model of NWFET has recently been reported, where the transistor channel is represented by a number of cascaded ballistic transistors [16]. However, the model requires that all ballistic transistors are operated in the linear region, which is not the case in reality.

In this paper, we propose a simplified circuit compatible analytical device model of NWFET for both ballistic and drift-diffusion transport, which can be efficiently used in any conventional circuit simulator like SPICE. The closed form expressions for I–V and capacitance–voltage (C–V) characteristics are obtained by analytically solving the device equation with appropriate approximation. We first obtain a quasi-analytical expression of I–V characteristics considering ballistic transport in the channel and then incorporate the drift-diffusion transport phenomena by appropriately modifying the channel mobility. While we have used a simplified field dependent mobility expression based on [17] in this analysis, a more effective mobility expression [18], however, can also be used in this model. We also compare the developed model with measured I–V characteristics of a Ge-NWFET.

The rest of this paper is organized as follows. In Section II, the developed compact model of NWFET is described considering both ballistic and drift-diffusion current transport. Section III presents the experimental verification of the above model with the measured I–V characteristics of a fabricated nanowire PFET followed by a conclusion in Section IV.

II. Compact Model of NWFET

For circuit simulation using conventional simulator like SPICE, we need an analytical expression for device (e.g., I–V and C–V) characteristics in terms of applied terminal voltages (e.g., $V_{\rm gs}$, $V_{\rm ds}$). However, it is impossible to obtain analytical expressions directly by solving self-consistent equations for nanowire transistors with small dimension. For example, the applied voltage at the gate terminal partly drops across the insulator ($V_{\rm INS}$) and partly across the channel [see Fig. 1(b)]. On top of this, the lateral electric field due to applied drain voltage further complicates the entire electrostatics. Finding an analytical solution to such a complicated system of highly

Manuscript received November 30, 2006; revised April 10, 2007. The review of this paper was arranged by Editor M. Reed.

B. C. Paul is with the Center for Integrated Systems, Stanford University, Stanford, CA 94305-4070 USA and also with Toshiba America Research, Inc., San Jose, CA 95131 USA (e-mail: bpaul@tari.toshiba.com).

R. Tu, T. H. Lee, and Y. Nishi are with the Center for Integrated Systems, Stanford University, Stanford, CA 94305-4070 USA.

S. Fujita and M. Okajima are with the Toshiba America Research, Inc., San Jose, CA 95131 USA.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2007.899397

0018-9383/$25.00 © 2007 IEEE

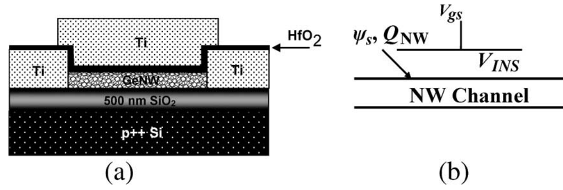


Fig. 1. (a) Schematic of a NWFET; (b) Schematic of potential drop across the device. The applied gate voltage (V_{gs}) partly drops across the insulator (V_{INS}) and partly across the nanowire channel.

nonlinear simultaneous equations is extremely difficult. As a result, most previously developed physical device models use numerical techniques to obtain device characteristics taking the surface potential Ψ_s (not the terminal potential: V_g, V_d, or V_s [Fig. 1(b)]) as the reference [6], [13], [14]. However, conventional circuit simulators can efficiently handle only analytical expressions for device properties. In this section, we obtain quasi-analytical expressions for device I–V and C–V characteristics by analytically solving these simultaneous device equations with suitable approximations.

Conceptually in an NWFET, the nanowire channel is connected between the source and drain contacts, which are in thermodynamic equilibrium. Hence, the electrostatics at source and drain contacts can be described by their individual Fermi level. Since the nanowire channel is isolated from any other source of mobile carrier, source and drain are the sole source of carriers inside the nanowire channel. A detailed description of this generic picture of nanowire MOSFET can be found in existing literature [5], [6], [14] and hence is avoided here. In such an electrostatic system, the carrier density for all valleys of any subband (nth) of a nanowire channel can be expressed as [14]

$$n_p = \sum_{\upsilon} g_{\upsilon} \int_{E_{\upsilon}^{n}}^{\infty} \frac{D_{\upsilon}^{n}(E)}{2} \left[f(E-\xi_s) + f(E-\xi_d) \right] dE \quad (1)$$

where $\xi_{s(d)}$ is the source (drain) Fermi level, E_{υ}^{n} be the conduction band minimum for the nth subband, which depends on the nanowire diameter [14], $f(E)$ is the probability that a state with energy E is occupied. $D(E)$ is the density-of-states and g_{υ} is the valley degeneracy. We assume that the tunneling of carrier from gate to the channel is negligible. Due to cylindrical geometry of NWFET, a relatively large gate insulator thickness can be used while maintaining an excellent gate control and hence, the above assumption is reasonable. Most state-of-the-art NWFETs reported in the literature also use high-κ dielectric, which further enable us to use even larger gate insulator thickness resulting in negligible gate to channel tunneling. Introducing 1-D density of states [14], the total charge (per unit length) in the nanowire channel can be written from (1) as

$$Q_{\mathrm{NW}} = \frac{q\sqrt{2k_B T}}{2\pi\hbar} \sum_{n} \sum_{\upsilon} g_{\upsilon} \sqrt{m_d^{\upsilon}} \times \left\{ \int_{0}^{\infty} \frac{E^{-1/2} dE}{1+e^{\left[\frac{E+E_{\upsilon}^{n}-q\psi_s}{k_B T}\right]}} + \int_{0}^{\infty} \frac{E^{-1/2} dE}{1+e^{\left[\frac{E+E_{\upsilon}^{n}-q(\psi_s - V_{\mathrm{ds}})}{k_B T}\right]}} \right\} \quad (2)$$

where m_d^{υ} is the density of states effective mass, and Ψ_s is the surface potential. k_B is the Boltzmann constant, T the absolute temperature, and q is the electronic charge. We consider the source potential as the reference potential and V_{ds} is the drain potential with respect to source. Note that the Fermi integrals (of order $-1/2$) in the above equation are not solvable analytically and hence, a closed form expression for charge (Q_{NW}) cannot be obtained directly. Although solving (2) analytically is not possible, an approximate closed form solution can be obtained by dividing the operating condition into several parts. For $|\psi_s| < |\psi_T|$ (below threshold, where ψ_T is the surface potential at the threshold point), when $E + E_{\upsilon}^{n} - q\psi_s \gg 0$ (for all 'E': $0 \to \infty$), (2) can be approximated to calculate the charge as

$$\begin{aligned} Q_{\mathrm{NW}} &= N_0 \left[\sum_{n} \sum_{\upsilon} g_{\upsilon} \sqrt{m_d^{\upsilon}} \left\{ \int_{0}^{\infty} E^{-1/2} e^{-\left[\frac{E+E_{\upsilon}^{n}}{k_B T}\right]} dE \right\} \right] \\ &\quad \times \left(1 + e^{-\frac{V_{\mathrm{ds}}}{\beta}}\right) e^{\frac{\psi_s}{\beta}} \\ &= \alpha e^{\frac{\psi_s}{\beta}} \end{aligned} \quad (3)$$

where

$$N_0 = \frac{q\sqrt{2k_B T}}{2\pi\hbar}$$

where $\beta(k_B T/q)$ is the thermal voltage. The main idea of this approach is to separate bias terms from the integral so that the integration can be precomputed numerically. It is observed that $\psi_T = E_{\upsilon}^{n}/q - 2\beta$ is a good choice for the above approximation because when $|\psi_s|$ is more than 2β below $|E_{\upsilon}^{n}/q|$, few thermally excited carriers will reach the conduction band. The integral of (3) can be precomputed numerically and α can be analytically obtained for any drain voltage. For $\psi_T < \psi_s \leq E_{\upsilon}^{n}/q$ (above threshold), there will be sufficient number of free carriers in the conduction band making the exponential term $(e^{[(E+E_{\upsilon}^{n}-q\psi_s)/k_B T]})$ in the denominator of the Fermi integral comparable to 1 and hence, "1" cannot be ignored as in the case of subthreshold. (2) can however, be rewritten as

$$\begin{aligned} Q_{\mathrm{NW}} &= N_0 \sum_{n} \sum_{\upsilon} g_{\upsilon} \sqrt{m_d^{\upsilon}} \\ &\quad \times \sum_{V_i = 0, V_{\mathrm{ds}}} \left[\int_{0}^{\infty} \frac{E^{-1/2} dE}{e^{\frac{E+E_{\upsilon}^{n}-q(\psi_s - V_i)}{k_B T}} \left(1 + e^{-\frac{E+E_{\upsilon}^{n}-q(\psi_s - V_i)}{k_B T}}\right)} \right] \\ &= N_0 \sum_{n} \sum_{\upsilon} g_{\upsilon} \sqrt{m_d^{\upsilon}} \\ &\quad \times \sum_{V_i = 0, V_{\mathrm{ds}}} \left[\int_{0}^{\infty} E^{-1/2} e^{-\frac{E+E_{\upsilon}^{n}-q(\psi_s - V_i)}{k_B T}} \right. \\ &\quad \left. \times \left(1 + e^{-\frac{E+E_{\upsilon}^{n}-q(\psi_s - V_i)}{k_B T}}\right)^{-1} dE \right]. \end{aligned} \quad (4)$$

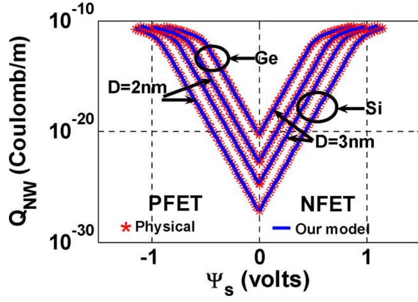


Fig. 2. $Q_{\rm NW}$ versus Ψ_s of nanowire NFETs with different wire diameters and materials (Si and Ge). Physical model represents the numerical solution of (2).

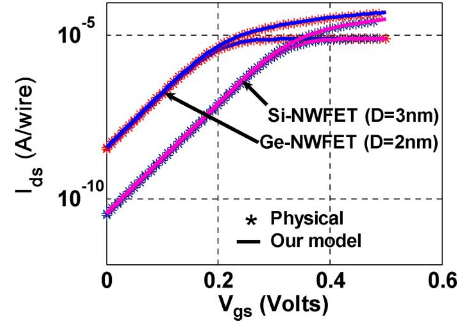


Fig. 3. $I_{\rm ds}$ versus $V_{\rm gs}$ of nanowire NFET with different diameters and materials (Si and Ge) considering ballistic transport. HfO_2 (8-nm thick) was used as insulator and a work-function difference of 0.45 eV is used for all devices.

Note that for $\psi_T < \psi_s \leq E_\upsilon^n/q$, the exponential term in the denominator is still greater than "1" and (2) is rewritten as shown above to make this a converging series. Expanding (4) now into a binomial series, and $e^{(\psi_s-\psi_T)/\beta}$ into infinite series and neglecting the higher order terms we obtain $Q_{\rm NW}$ as

$$Q_{\rm NW} = N_0 \sum_n \sum_\upsilon g_\upsilon \sqrt{m_d^\upsilon} \times \sum_{m=1}^{\infty} \left[(-1)^{m-1} e^{\frac{m(\psi_s-\psi_T)}{\beta}} \left(1+e^{-\frac{mV_{\rm ds}}{\beta}}\right) \times \int_0^\infty E^{-1/2} \left(e^{-m\cdot\left(\frac{E+E_\upsilon^n-q\psi_T}{k_BT}\right)}\right) dE \right] \tag{5a}$$

$$\approx \lambda_0 + \rho_1\lambda_1(\psi_s-\psi_T) + \rho_2\lambda_2(\psi_s-\psi_T)^2. \tag{5b}$$

λ_0, λ_1, and λ_2 are geometry, and $V_{\rm ds}$ dependent parameters (see Appendix), which can be obtained with simple algebraic calculation, while all integrations can be performed numerically. Note that the reason for approximating $Q_{\rm NW}$ into polynomial form is to obtain an analytical $V_{\rm gs} - \psi_s$ relation, which is derived later in this section. Further, although one can obtain an accurate expression by considering higher order terms (without using any correction factor), we, however, use the above polynomial of order two with constant correction factors ρ_1 and ρ_2 to obtain a simpler $V_{\rm gs} - \psi_s$ relation. For $\psi_s > E_\upsilon^n/q$, although a similar approximate solution can be achieved following the above approach, we, however, observed that (5b) also efficiently predicts the charge in this region.

Fig. 2 shows $Q_{\rm NW}$ verses ψ_s of nanowire NFETs with different wire diameters and materials (Si and Ge) obtained from physics model [14] and the above analytical model. Physical model represents the numerical solution of (2) and the analytical solution is obtained using (3) and (5b). It can be seen that the analytical model closely matches with physics model for all devices.

A. Ballistic Transport

$Q_{\rm NW}$ can now be related to gate voltage V_g through the following voltage divider equation [see Fig. 1(b)].

$$\psi_s = V_{\rm gs} - \phi_{\rm ms} - V_{\rm INS} = V_{\rm gs} - \phi_{\rm ms} - \frac{Q_{\rm NW}}{C_{\rm INS}} \tag{6}$$

where $C_{\rm INS}$ is the insulator capacitance and $\phi_{\rm ms}$ is the work function difference. Note that for different gate structures such as top-gate Ω-gate and gate-all-around structures $C_{\rm INS}$ should be modified accordingly. Substituting $Q_{\rm NW}$ in (6) from (3) and (5b), an analytical closed form expression for $V_{\rm gs} - \psi_s$ then can be obtained as (7), which is shown at the bottom of the next page, where V_T is the gate voltage (threshold voltage) corresponding to ψ_T. Knowing ψ_s in terms of the terminal voltages the drain current $I_{\rm ds}$ and gate input capacitance C_G (Fig. 1) can now be obtained following Landauer approach as [13]

$$I_{\rm ds} = \frac{qk_BT}{\pi\hbar} \sum_n \sum_\upsilon g_\upsilon \times \left[\ln\left(1+e^{(q\psi_s-E_\upsilon^n)/k_BT}\right) - \ln\left(1+e^{(q\psi_s-E_\upsilon^n-qV_{\rm ds})/k_BT}\right) \right]$$

and

$$C_G = \frac{\partial Q_{\rm NW}}{\partial V_{\rm gs}}. \tag{8}$$

Figs. 3 and 4 show I–V (I_d–V_g and I_d–V_d) characteristics of a ballistic NWFET with different materials (Si and Ge). An 8-nm-thick HfO_2 is used as insulator and a work-function difference of 0.45 eV is used for all devices. It can be observed that the above model closely matches with the physical model.

B. Drift-Diffusion Transport

Although the ballistic transport provides much higher drive current, achieving this in real devices is quite illusive. Demonstrated nanowire devices show much lower drive currents [7], [9], [11] than are expected considering ballistic transport. This is because in real devices scattering effect is not negligible and hence, ballistic transport model does not efficiently predict the current in these devices. We will now develop a more realistic device model considering drift-diffusion transport. Solving (3), (5b), and (6), an analytical $V_{\rm gs} - Q_{\rm NW}$ relation can also be obtained as (9), which is shown at the bottom of the next page.

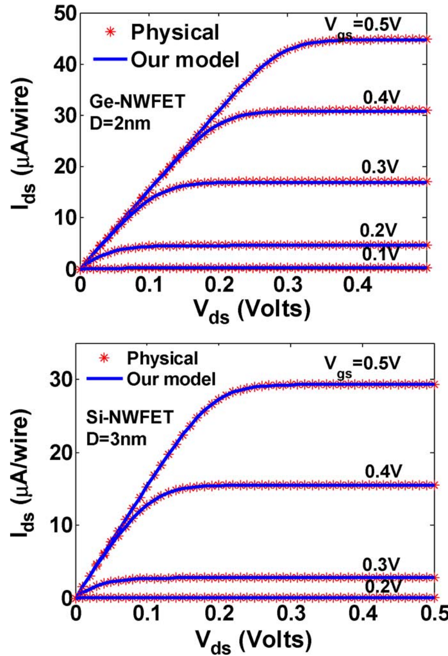


Fig. 4. $I_{\rm ds}$ versus $V_{\rm ds}$ of nanowire NFET with different materials [(a) Ge and (b) Si] considering ballistic transport. HfO_2 (8-nm thick) was used as insulator and a work-function difference of 0.45 eV is used for all devices.

The drift-diffusion current then can be obtained by analytically integrating the following [17]:

$$I_{\rm ds} = \frac{\mu}{L_{\rm eff}} \int_0^{V_{\rm ds}} Q_{\rm NW}(V_{\rm gs}, V_{\rm ds}) dV \tag{10}$$

where μ is the field dependent mobility given by

$$\mu = \frac{\mu_0}{\left(1 + \frac{\mu_0}{\nu_{\rm sat} L_{\rm eff}} V_{\rm ds}\right)}. \tag{11}$$

Substituting $Q_{\rm NW}$ from (9), the integrations in (10), however, cannot be performed in closed form and hence, further approximation on the $V_{\rm ds}$ dependence of $Q_{\rm NW}$ is required. It

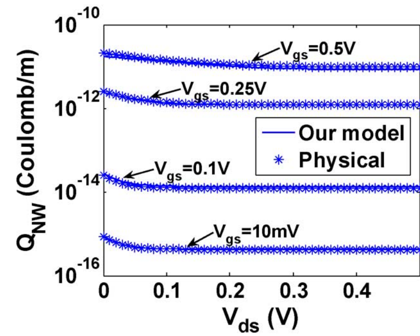


Fig. 5. Lateral field ($V_{\rm ds}$) dependence of channel charge of a Ge nanowire NFET with 2-nm-diameter ($L_{\rm eff} = 250$ nm).

can be easily observed from (1) and (2) that the channel charge with $V_{\rm ds} = 0$ will be twice that of for large $V_{\rm ds}$ ($>$ a few kT/q) for all gate voltages. $Q_{\rm NW}$ dependence on $V_{\rm ds}$ within these two limiting values is seen to be approximately exponential in nature. While this exponential function in subthreshold region is independent of $V_{\rm gs}$, it, however, depends on $V_{\rm gs}$ in the inversion region due to the strong correlation between the transverse and lateral electric field at the drain end. Hence, the modified charge expression with the above approximation on lateral field ($V_{\rm ds}$) dependence can be rewritten as (12), which is shown at the bottom of the next page, where α^* and λ^*s are the parameters from (3) and (5b) with large lateral field ($V_{\rm ds} \gg \beta$) and η can be expressed as

$$\eta = 1 + \chi \cdot (V_{\rm gs} - V_T)^{\gamma} \tag{13}$$

χ and γ are found empirically for a nanowire structure.

Fig. 5 shows the variation in channel charge of a Ge-NWFET with $V_{\rm ds}$ for different gate voltages. It can be seen that the above approximation closely predicts the lateral field ($V_{\rm ds}$) dependence of charge. Substituting $Q_{\rm NW}$ now in (10) from (12) and integrating analytically, the drift-diffusion current can be obtained as (14), which is shown at the bottom of the next page.

Figs. 6 and 7 show the I–V ($I_{\rm ds}$–$V_{\rm gs}$ and $I_{\rm ds}$–$V_{\rm ds}$) characteristics of Si and Ge NWFETs considering drift-diffusion

$$\begin{aligned}\psi_s &= V_{\rm gs} - \phi_{\rm ms} - \beta \cdot \text{lambertw}\left[\frac{\alpha}{\beta \cdot C_{\rm INS}} e^{[(V_{\rm gs}-\phi_{\rm ms})/\beta]}\right] \qquad \text{for } V_{\rm gs} \le V_T \\ &= \psi_T + \frac{-(\rho_1\lambda_1 + C_{\rm INS}) + \left[(\rho_1\lambda_1 + C_{\rm INS})^2 - 4\rho_2\lambda_2\left[\lambda_0 - C_{\rm INS}(V_{\rm gs} - \phi_{\rm ms} - \psi_T)\right]\right]^{1/2}}{2\rho_2\lambda_2} \qquad \text{for } V_{\rm gs} > V_T\end{aligned} \tag{7}$$

$$\begin{aligned}Q_{\rm NW} &= \beta C_{\rm INS} \cdot \text{ lambertw}\left[\frac{\alpha}{\beta \cdot C_{\rm INS}} e^{(V_{\rm gs}-\phi_{\rm ms})/\beta}\right] \qquad \text{for } V_{\rm gs} \le V_T \\ Q_{\rm NW} &= C_{\rm INS}\left[V_{\rm gs} - \phi_{\rm ms} - \psi_T + \frac{(\rho_1\lambda_1 + C_{\rm INS})}{2\rho_2\lambda_2}\right] \\ &\quad - C_{\rm INS}\frac{\left[(\rho_1\lambda_1 + C_{\rm INS})^2 - 4\rho_2\lambda_2\left[\lambda_0 - C_{\rm INS}(V_{\rm gs} - \phi_{\rm ms} - \psi_T)\right]\right]^{1/2}}{2\rho_2\lambda_2} \qquad \text{for } V_{\rm gs} > V_T\end{aligned} \tag{9}$$

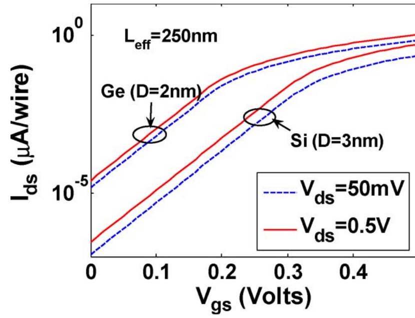


Fig. 6. I_{ds} versus V_{gs} of nanowire NFET (Si and Ge) considering drift-diffusion transport. HfO_2 (8-nm thick) was used as insulator and a work-function difference of 0.45 eV is used for all devices.

transport. All nanowires are considered $\langle 110 \rangle$ type for comparison purposes. An effective channel length (L_{eff}) of 250 nm is used for all devices in the simulation. It can be observed that current considering drift-diffusion transport is considerably smaller than the ballistic current.

III. Experimental Verification

To further validate the above compact model the I–V characteristics of a fabricated nanowire PFET was compared. Fig. 8 shows the comparison of the above nanowire model with measured I–V characteristics. The PFET device was fabricated on a 500-nm-thick SiO_2 substrate [Fig. 8(a)] with 250-nm-long Ge nanowire $(\langle 110 \rangle)$ channel (diameter $=$ 12 nm). Schottky source–drain electrodes were formed using Ti metal. An 8-nm-thick HfO_2 gate dielectric was deposited using atomic layer deposition (ALD) prior to evaporating the Ti metal gate electrode. It can be observed from Fig. 8(b) that the above model closely matches with the experimental results for a wide range of bias voltages. Note that we used a simple model [19] for Schottky source/drain contact for comparison purposes because the fabricated device had Schottky contacts at both source and drain junctions. However, in reality these devices

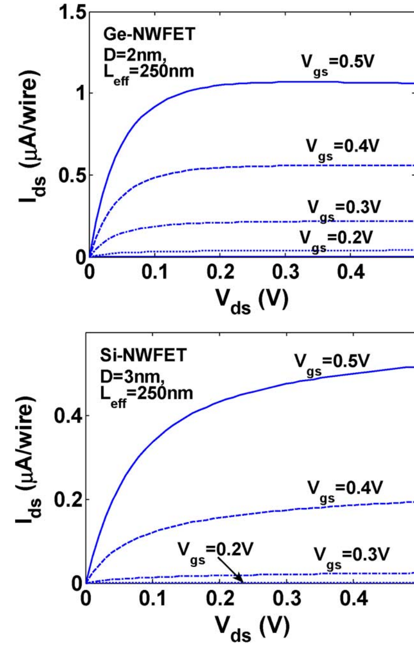


Fig. 7. I_{ds} versus V_{ds} of nanowire NFET with materials [(a) Ge and (b) Si] considering drift-diffusion transport. HfO_2 (8-nm thick) was used as insulator and a work-function difference of 0.45 eV is used for all devices.

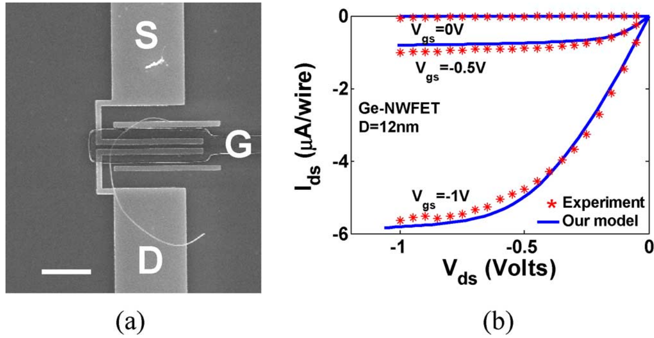
are expected to have ohmic contacts at both source and drain junctions and hence, a rigorous Schottky contact modeling may not be required.

IV. Conclusion

In this paper, we provided an analytical compact model of NWFET for both ballistic and drift-diffusion current transport. Considering the fact that a direct closed from expression for the device characteristics cannot be achieved, reasonable approximations were made to obtain an eventual analytical solution. The model is seen to be effective for a wide range of wire diameters and also showed a close agreement with

$$\begin{aligned}
Q_{\mathrm{NW}} &= \beta C_{\mathrm{INS}} \text{ lambertw}\left[\frac{\alpha^*}{\beta \cdot C_{\mathrm{INS}}} e^{(V_{\mathrm{gs}}-\phi_{\mathrm{ms}})/\beta}\right]\left(1+e^{-V_{\mathrm{ds}}/\beta}\right) \qquad \text{for } V_{\mathrm{gs}} \le V_T \\
Q_{\mathrm{NW}} &= C_{\mathrm{INS}}\left(1+e^{-\frac{V_{\mathrm{ds}}}{\eta\beta}}\right)\left[V_{\mathrm{gs}}-\phi_{\mathrm{ms}}-\psi_T+\frac{(\rho_1\lambda_1^*+C_{\mathrm{INS}})}{2\rho_2\lambda_2^*}\right] \\
&\quad - C_{\mathrm{INS}}\left(1+e^{-\frac{V_{\mathrm{ds}}}{\eta\beta}}\right)\frac{\left[(\rho_1\lambda_1^*+C_{\mathrm{INS}})^2-4\rho_2\lambda_2^*\left[\lambda_0^*-C_{\mathrm{INS}}(V_{\mathrm{gs}}-\phi_{\mathrm{ms}}-\psi_T)\right]\right]^{1/2}}{2\rho_2\lambda_2^*} \qquad \text{for } V_{\mathrm{gs}} > V_T
\end{aligned} \tag{12}$$

$$\begin{aligned}
I_{\mathrm{ds}} &= \frac{\beta\mu C_{\mathrm{INS}}}{L_{\mathrm{eff}}} \text{ lambertw}\left[\frac{\alpha^*}{\beta \cdot C_{\mathrm{INS}}} e^{(V_{\mathrm{gs}}-\phi_{\mathrm{ms}})/\beta}\right]\left(V_{\mathrm{ds}}+\beta\left[1-e^{-V_{\mathrm{ds}}/\beta}\right]\right) \quad \text{for } V_{\mathrm{gs}} \le V_T \\
I_{\mathrm{ds}} &= \frac{\mu C_{\mathrm{INS}}}{L_{\mathrm{eff}}}\left(V_{\mathrm{ds}}+\eta\beta\left[1-e^{-\frac{V_{\mathrm{ds}}}{\eta\beta}}\right]\right)\left[V_{\mathrm{gs}}-\phi_{\mathrm{ms}}-\psi_T+\frac{(\rho_1\lambda_1^*+C_{\mathrm{INS}})}{2\rho_2\lambda_2^*}\right]-\frac{\mu C_{\mathrm{INS}}}{L_{\mathrm{eff}}}\left(V_{\mathrm{ds}}+\eta\beta\left[1-e^{-\frac{V_{\mathrm{ds}}}{\eta\beta}}\right]\right) \\
&\quad \times \frac{\left[(\rho_1\lambda_1^*+C_{\mathrm{INS}})^2-4\rho_2\lambda_2^*\left[\lambda_0^*-C_{\mathrm{INS}}(V_{\mathrm{gs}}-\phi_{\mathrm{ms}}-\psi_T)\right]\right]^{1/2}}{2\rho_2\lambda_2^*} \qquad \text{for } V_{\mathrm{s}} > V_T
\end{aligned} \tag{14}$$



(a) (b)

Fig. 8. (a) SEM image of a nanowire PFET. Devices were fabricated on a 500-nm-thick SiO_2 substrates with 250-nm-long Ge nanowire ($\langle 110 \rangle$) channel ($D = 12$ nm). Schottky source–drain electrodes were formed using Ti metal. 8 nm of HfO_2 gate dielectric was deposited using ALD prior to evaporating the Ti metal gate electrode. (b) Comparison of the developed drift-diffusion current model with experimental result.

experimental result. The model therefore, can be efficiently used in large circuit simulations using NWFETs.

Appendix
Polynomial Expression of $Q_{\rm NW}$

Expanding (4) into binomial series, we get

$$Q_{\rm NW} = N_0 \sum_n \sum_v g_v \sqrt{m_d^v} \times \sum_{V_i=0,V_{\rm ds}} \left[\int_0^\infty E^{-1/2} e^{-\frac{E+E_v^n - q(\psi_s - V_i)}{k_B T}} \sum_{m=1}^{m=\infty} (-1)^{m-1} \times e^{-\frac{(m-1)\left[E+E_v^n - q(\psi_s - V_i)\right]}{k_B T}} dE \right]. \quad \text{(A1)}$$

Rearranging the summations and integration, (A1) can be rewritten as

$$Q_{\rm NW} = N_0 \sum_n \sum_v g_v \sqrt{m_d^v} \times \sum_{m=1}^\infty \left[\int_0^\infty (-1)^{m-1} E^{-1/2} \times \left(e^{-\frac{m[E+E_v^n - q(\psi_s)]}{k_B T}} + e^{-\frac{m[E+E_v^n - q(\psi_s - V_{\rm ds})]}{k_B T}} \right) dE \right]. \quad \text{(A2)}$$

It is now possible to conveniently decouple bias terms from the integration and we obtain (5a) [(A3)] after simple algebraic manipulation

$$Q_{\rm NW} = N_0 \sum_n \sum_v g_v \sqrt{m_d^v} \times \sum_{m=1}^\infty \left[(-1)^{m-1} e^{\frac{m(\psi_s - \psi_T)}{\beta}} \left(1 + e^{-\frac{mV_{\rm ds}}{\beta}}\right) \times \int_0^\infty E^{-1/2} \left(e^{-m \cdot \left(\frac{E+E_v^n - q\psi_T}{k_B T}\right)} \right) dE \right]. \quad \text{(A3)}$$

Further, expanding $e^{m(\psi_s - \psi_T)/\beta}$ into an infinite series, we get

$$Q_{\rm NW} = N_0 \sum_n \sum_v g_v \sqrt{m_d^v} \times \sum_{m=1}^\infty \left[(-1)^{m-1} \sum_{j=1}^\infty \left[\frac{(m(\psi_s - \psi_T))^{j-1}}{\beta^{j-1}(j-1)!} \right] \times \left(1 + e^{-\frac{mV_{\rm ds}}{\beta}}\right) \int_0^\infty E^{-1/2} \times \left(e^{-m \cdot \left(\frac{E+E_v^n - q\psi_T}{k_B T}\right)} \right) dE \right]. \quad \text{(A4)}$$

Hence, a polynomial expression can be obtained as

$$Q_{\rm NW} = \sum_{j=1}^\infty \lambda_{j-1} (\psi_s - \psi_T)^{j-1} \quad \text{(A5)}$$

where

$$\lambda_j = N_0 \sum_n \sum_v g_v \sqrt{m_d^v} \times \sum_{m=1}^\infty \left[(-1)^{m-1} \frac{m^{j-1}}{\beta^{j-1}(j-1)!} \left(1 + e^{-\frac{mV_{\rm ds}}{\beta}}\right) \times \int_0^\infty E^{-1/2} \left(e^{-m \cdot \left(\frac{E+E_v^n - q\psi_T}{k_B T}\right)} \right) dE \right]. \quad \text{(A6)}$$

Note that all integrations in (A6) can be precomputed. Further, note that at $\psi_s = \psi_T$ (threshold point) $Q_{\rm NW}$ can be expressed as

$$Q_{\rm NW}(\psi_T) = \lambda_0 = N_0 \sum_n \sum_v g_v \sqrt{m_d^v} \times \sum_{m=1}^\infty \left[(-1)^{m-1} \left(1 + e^{-\frac{mV_{\rm ds}}{\beta}}\right) \int_0^\infty E^{-1/2} \times \left(e^{-m \cdot \left(\frac{E+E_v^n - q\psi_T}{k_B T}\right)} \right) dE \right] \cong \alpha e^{\frac{\psi_T}{\beta}} \quad \text{[see (3)].} \quad \text{(A7)}$$

This is because at $\psi_s = \psi_T$, where $E + E_v^n - q\psi_s \gg 0$, all terms in (A7) for $m > 1$ are negligible. Hence, the continuity at the threshold point will be maintained.

References

[1] D. Frank, R. Dennard, E. Nowak, P. Solomon, Y. Taur, and H. S. P. Wong, "Device scaling limits of Si MOSFETs and their application dependencies," *Proc. IEEE*, vol. 89, no. 3, pp. 259–288, Mar. 2001.

[2] M. T. Bohr, "Nanotechnology goals and challenges for electronic applications," *IEEE Trans. Nanotechnol.*, vol. 1, no. 1, pp. 56–62, Mar. 2002.

[3] J. P. Collinge, "Multiple gate SOI MOSFETs," *Solid State Electron.*, vol. 48, no. 6, pp. 897–905, Jun. 2004.

[4] B. S. Doyle *et al.*, "High performance fully depleted tri-gate CMOS transistors," *IEEE Electron Device Lett.*, vol. 24, no. 4, pp. 263–265, Apr. 2003.
[5] J. Wang, E. Polizzi, and M. Lundstrom, "A computational study of ballistic silicon nanowire transistors," in *IEDM Tech. Dig.*, Washington, DC, Dec. 2003, pp. 695–698.
[6] J. Wang, A. Rahman, G. Klimeck, and M. Lundstrom, "Bandstructure and orientation effects in ballistic Si and Ge nanowire FETs," in *IEDM Tech. Dig.*, 2005, pp. 530–533.
[7] Y. Cui, Z. Zhong, D. Wang, W. U. Wang, and C. M. Lieber, "High performance silicon nanowire field effect transistors," *Nano Lett.*, vol. 3, no. 2, pp. 149–152, 2003.
[8] J. Xiang *et al.*, "Ge/Si nanowire heterostructures as high performance field-effect transistors," *Nature Lett.*, vol. 441, no. 7092, pp. 489–493, May 2006.
[9] N. Singh *et al.*, "High-performance fully depleted Silicon nanowire (diameter ≤ 5 nm) gate-all-around CMOS devices," *IEEE Electron Device Lett.*, vol. 27, no. 5, pp. 383–386, May 2006.
[10] K. H. Yeo *et al.*, "Gate-all-around (GAA) twin silicon nanowire MOSFET (TSNWFET) with 15 nm length gate and 4 nm radius nanowire," in *IEDM Tech. Dig.* , 2006, pp. 1–4.
[11] Y. Wang *et al.*, "Inversion mode operation of thermally oxidized modulation doped silicon nanowire field effect devices," in *Proc. DRC*, University Park, PA, 2006, pp. 193–194.
[12] T. Bryllert, L. E. Wernersson, L. E. Froberg, and L. Samuelson, "Vertical high-mobility wrap-gated InAs nanowire transistor," *IEEE Electron Device Lett.*, vol. 27, no. 5, pp. 323–325, May 2006.
[13] D. Jimenez, J. J. Saenz, B. Iniguez, J. Sune, L. F. Marsal, and J. Pallares, "Modeling of nanoscale gate-all-around MOSFETs," *IEEE Electron Device Lett.*, vol. 25, no. 5, pp. 314–316, May 2004.
[14] D. Jimenez, J. J. Saenz, B. Iniguez, J. Sune, L. F. Marsal, and J. Pallares, "Unified compact model for the ballistic quantum wire and quantum well metal–oxide–semiconductor field-effect-transistor," *J. Appl. Phys.*, vol. 94, no. 2, pp. 1061–1068, Jul. 2003.
[15] J. Chen, "A circuit-compatible model for ballistic nanowire transistors," in *Proc. Nanotech Conf.*, 2006, pp. 850–853.
[16] G. Mugnaini and G. Iannaccone, "Analytical model for nanowire and nanotube transistors covering both dissipative and ballistic transport," in *Proc. ESSDERC*, Grenoble, France, 2005, pp. 213–216.
[17] G. Baccarani and S. Reggiani, "A compact double-gate MOSFET model comprising quantum-mechanical and nonstatic effects," *IEEE Trans. Electron Devices*, vol. 46, no. 8, pp. 1656–1666, Aug. 1999.
[18] K. Dragosits, V. Palankovski, and S. Selberherr, "Mobility modeling in presence of quantum effects," in *Proc. SISPAD*, 2003, pp. 271–274.
[19] S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. Hoboken, NJ: Wiley, 1981.

Bipul C. Paul (S'97–M'01–SM'05) received B.Tech. and M.Tech. degrees in radiophysics and electronics from University of Calcutta,West Bengal, India, and the Ph.D. degree from the Indian Institute of Science, Bangalore, India.

He has been a Research Scientist at Toshiba America Research since 2005. His research interest includes device and circuit design for emerging nanotechnology, statistical design, design for yield and reliability, 3-D nanoarchitecture, ROM-based design for high-performance logic, and ultralow power design. Earlier, he was with Alliance Semiconductor, India, where he worked on synchronous DRAM design. From 2000–2005, he was with Purdue University, West Lafayette, as a Postdoctoral Fellow, where he developed several device models and statistical design techniques for nanoscale circuits and memory. He has also developed device and circuit optimization techniques for ultralow power digital subthreshold operation. He is also a Visiting Scientist at Stanford University, Stanford, CA. He has published more than 60 technical papers in international journals and conferences and invented several device and circuit design techniques.

Dr. Paul received National scholarship (India) in 1984, the senior research fellowship award from Council of Scientific and Industrial Research (Government of India) in 1995, the Best Thesis of the Year award in 1999, and the 2006 IEEE Circuits and Systems Society VLSI Transactions Best Paper Award. He has served in the technical program committees of several international conferences, including Design Automation and Test in Europe and IEEE International On-Line Testing Symposium and is presently in the Editorial Board IEE Computers and Digital Techniques and *Journal of Low Power Electronics*.

Ryan Tu received the Bachelor of Science in electrical engineering and computer science from University of California, Berkeley, in 2000, and the Ph.D. degree in materials science and engineering from Stanford University, Stanford, CA, in 2007. His thesis is titled, "Germanium Nanowire Synthesis, Alignment, and Field Effect Transistor Properties"

He received a graduate research fellowship from the National Science Foundation and is currently at Stanford.

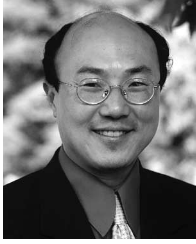
Shinobu Fujita (M'03) received the S.B., S.M., and Sc.D. degrees in applied physics from University of Tokyo, Tokyo, Japan, in 1984, 1986, and 1989, respectively.

He was with Toshiba Corporation in 1989, where he is engaged on the development of high-speed compound semiconductor devices and circuit design, and basic research on quantum devices.

He has been engaged in nanotechnology based on silicon nanodevices since 1994. Since 1999, he has extended the research area to application, particularly for information security and nonvolatile memory. Since 2003, he has been joining collaborative work on 3-D circuits based on post-Si devices with Stanford University Center for Integrated Systems as a Project Leader of Toshiba. Since 2004, he has also been leading two projects with Caltech and Toshiba America.

Masaki Okajima received the B.S. and M.S. degrees in electrical engineering from the University of Tokyo, Japan, in 1978 and 1980, respectively.

He joined the Corporate Research and Development Center, Toshiba Corporation, Kawasaki, Japan, in 1980, working on the research and development of laser diodes and visible light emitting diodes and the development of liquid crystal displays in 1995. From 1998 to 2000, he headed the Display Devices and Materials Laboratory, Corporate Research and Development Center. He joined Toshiba America Research, Inc., San Jose, CA, in 2002. His research interests include light emitting devices, display devices, and nanoscale electronic devices.



Thomas H. Lee (S'89–M'90) received the S.B., S.M., and Sc.D. degrees in electrical engineering from Massachusetts Institute of Technology, Cambridge, in 1983, 1985, and 1990, respectively.

He was with Analog Devices in 1990, where he was primarily engaged in the design of high-speed clock recovery devices. In 1992, he was with Rambus, Inc., in Mountain View, CA, where he developed high-speed analog circuitry for 500 MB/s CMOS DRAMs. He has also contributed to the development of phase-locked loops in the StrongARM, Alpha, and AMD K6/K7/K8 microprocessors. Since 1994, he has been a Professor of electrical engineering at Stanford University, Stanford, CA, where his research focus has been on gigahertz-speed wireline and wireless integrated circuits built in conventional silicon technologies, particularly CMOS. He is the holder of 43 U.S. patents and authored the book *The Design of CMOS Radio-Frequency Integrated Circuits* (2003), and *Planar Microwave Engineering* (2004), both with Cambridge University Press. He is a coauthor of four additional books on RF circuit design, and also cofounded Matrix Semiconductor.

Dr. Lee has twice received the Best Paper Award at the International Solid-State Circuits Conference (ISSCC), coauthored a Best Student Paper at ISSCC, was awarded the Best Paper prize at the Custom Integrated Circuits Conference, and is a Packard Foundation Fellowship recipient. He is an IEEE Distinguished Lecturer of both the Solid-State Circuits and Microwave Societies.

Yoshio Nishi (SM'82–F'88) received the B.S. degree in material science from Waseda University, Shinjuku, Tokyo, Japan, and the Ph.D. degree in electronics engineering from University of Tokyo, Tokyo, Japan, respectively.

He has been a Professor in the Department of Electrical Engineering (research) and also in the Department of Material Science and Engineering at Stanford University, Stanford, CA, since May 2002. He also serves as Director of Stanford Nanofabrication Facility of National Nanotechnology Infrastructure Network of U.S., and Director of Research of Center for Integrated Systems. He was with Toshiba R&D in the areas of research for semiconductor device physics and interfaces mostly in silicon, resulting in discovery of ESR PB Center at SiO_2–Si interface, the first 256-bit metal nitride oxide silicon (MNOS) nonvolatile RAM, SOS 16-bit microprocessor and the world's first 1-Mb CMOS DRAM. He moved to Hewlett–Packard in 1986 as the Director of Silicon Process Lab, followed by establishing Ultralarge-scale Integration Research Lab as the Founding Director. In 1995, he joined Texas Instruments Incorporated as Senior Vice President and Director of Research and Development for semiconductor group, and implemented new R&D model for silicon technology development, followed by establishing Kilby Center. Since May 2002, he has been a faculty member of Stanford University, and his research interest covers nanoelectronic devices and materials, including metal gate/high-κ MOS, device layer transfer for 3-D integration, nanowire devices, and resistance change nonvolatile memory materials and devices. He published more than 200 papers, including conference proceedings, and coauthored/edited nine books. He is the holder of more than 70 patents in U.S. and Japan.

Dr. Nishi, during the period of 1995–2002, he served Semiconductor Research Corporation and International Sematech as Board member, National Nanotechnology Initiative (NNI) Panel, MARCO Governing Council, etc. Currently, he serves for Science Council of Japan, as an affiliated member. He is a member of Japan Society of Applied Physics and the Electrochemical Society. Recent awards which he received include 1995 IEEE Jack Morton Award and 2002 IEEE Robert Noyce Medal.