Impact of a Process Variation on Nanowire and Nanotube Device Performance

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***Abstract*—In this paper, we present an in-depth analysis of the nanowire and nanotube device performance under process variability. Although every process parameter variation drastically affects the conventional MOSFET performance, we found that nanowire/nanotube FETs are significantly less sensitive to many process parameter variations due to their inherent device structures and geometric properties. It is observed that a two-input NAND gate with nanowire or nanotube FETs shows a more than four times less performance variation than its bulk MOSFET counterpart and about two times less than FinFET devices at the 45 and 32 nm technologies, respectively. In other words, nanowire/nanotube FETs will have a larger margin for process parameter variations than bulk and FinFET devices for an allowable performance variation limit. While it is evident that process variations are going to be a major limiting factor for conventional MOSFET devices in future generations, this analysis is expected to further encourage nanowire and nanotube research for high-performance circuit applications.**

***Index Terms*—CNFET performance under variation, nanowire FET performance under variation, process variation.**

I. Introduction

As THE conventional silicon technology approaches its limit, several emerging devices such as nanowire FETs (NWFETs) and carbon nanotube FETs (CNFETs) are being extensively studied as possible alternatives [1]–[4]. CNFETs and NWFETs are convincingly shown to have the potential of taking this place in the post silicon era. Consistent device I–V characteristics suitable for digital circuit applications with superior conductance than conventional silicon MOSFETs have been successfully demonstrated [1], [2], [4]. While inherent characteristics of these devices, such as gate controllability and drive current, are shown to be superior to those of bulk MOSFETs, it is also widely believed that variations in the fabrication process may significantly undermine those advantages. However, we observed that due to their unique geometrical structure, CNFETs and NWFETs are significantly less sensitive to variations in many geometry-related process parameters such as oxide thickness ($T_{\rm ox}$) and gate width (W), which, on the other hand, significantly affect the performance of conventional MOSFET devices. Consequently, while ever-increasing difficulty in controlling process parameter variations may become the ultimate limiting factor for conventional MOSFET devices in future technologies, carbon nanotube and nanowire devices can conveniently overcome this bottleneck.

In this paper, we provide an in-depth analysis of the performance of CNFETs and NWFETs (both Si and Ge) under process parameter variations and compare them with bulk and FinFET devices. A systematic study considering all major process parameter variations and their impact on the drive current, effective capacitance, and, finally, circuit performance of all four devices is presented to provide a clear understanding of their overall sensitivity to process variations. To the best of our knowledge, this is the first attempt to quantitatively analyze the sensitivity of NWFETs and CNFETs to process parameter variations under a benchmarking scenario with bulk MOSFET and FinFET devices. Though process technologies such as the diameter- and direction-controlled growth are yet to mature, we, however, assume a reasonably matured process; e.g., the variation (3σ) in a growth parameter such as the diameter is less than 50%, since such a matured process is required for practical use of these new devices in the future. This assumption is reasonable, considering the recent progress [1], [2], [4], and it also enables us to make a fair comparison with existing Si MOSFET devices based on the same dimension of source, drain, and gate areas. We also use a predictive technology model for both bulk and FinFET devices at the 45 and 32 nm technology nodes [5]. A two-input NAND gate with an inverter load is considered for evaluating the overall performance variation to avoid extreme simulation complexity in nanowire and nanotube devices. We show that in both the 45 and 32 nm technologies, NWFET/CNFET devices show a more than four times less performance variation than bulk MOSFET devices and significantly less (i.e., $\sim 2\times$) than FinFET devices. In other words, for a tolerable performance variation, nanowire and nanotube devices can have much larger allowable process parameter variations than those of bulk and FinFET devices.

The rest of this paper is organized as follows. Section II provides a qualitative discussion on NWFET/CNFET characteristics under a process variation. In Section III, the basic device structures of nanowire and nanotube FETs are described, along with their geometrical dimensions. The models that were used for the simulation of these devices are also briefly discussed. Section IV presents simulation results and discussion, followed by a conclusion in Section V.

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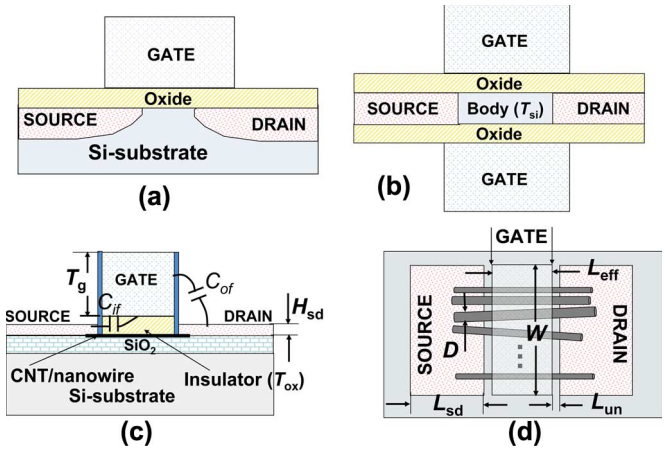

Fig. 1. (a) and (b) Schematic cross-sectional view of bulk MOSFET and FinFET devices. (c) Schematic of a nanowire/nanotube FET. (d) Top view of a nanowire/nantube transistor. Note that W here is the geometric gate width and *NOT the effective channel width* ($W_{\rm eff}$). Therefore, it does not affect $I_{\rm on}$ and only contributes to the parasitic capacitance. $W_{\rm eff}$ in these devices is obtained based on the diameter D of the tube and the number of tubes N under the gate. The $W_{\rm eff}$ variation is considered through D and N variations. Similarly, the variation in the tube/wire orientation is considered through the $L_{\rm eff}$ variation. (c) shows the fringe capacitance components specifically to explain the model in Section III-B. We, however, considered the fringe capacitance for all devices in our analysis.

II. Physical Insight to NWFET/CNFET Characteristics Under a Process Variation

Fig. 1 shows the schematic cross-sectional view of bulk MOSFET, FinFET, and top-gated nanowire and nanotube FET devices. Due to superior electrostatic geometry, nanowire and nanotube devices have better electrostatic properties than planar channel devices like bulk MOSFETs and FinFETs. FinFET devices with sandwiched fully depleted thin silicon body between two gates (front and back) has better gate control, resulting in excellent short channel effect immunity, and, hence, is more scalable than the conventional bulk MOSFET. Nanowire and nanotube devices, however, have the best gate control due to cylindrical electrostatic geometry and, hence, have the superior scalability over bulk and FinFET devices. While these devices have better scalability in terms of electrostatic properties, it is also interesting to analyze their sensitivity to process variations. Note that all these devices use lithography technique and, hence, will experience similar parametric variations. Physical dimensions such as the gate thickness, oxide thickness, channel length, and width will vary, affecting the device characteristics. However, their impact on the electrostatic characteristics (mainly drive current and capacitance) of these devices will be different. For example, while a variation in the oxide thickness $T_{\rm ox}$ strongly affects the drive current and capacitance of bulk and FinFET devices due to planar geometry, it will, however, have negligible impact on that of NWFET/CNFET devices due to cylindrical geometry. Further, the variation in the gate width W will not affect the drive current of the NWFET/CNFET devices at all. Note that, here, W [Fig. 1(d)] is the geometric gate width of nanowire and nanotube transistors and *NOT the effective channel width* $W_{\rm eff}$. Therefore, it does not affect $I_{\rm on}$ and only contributes to the parasitic capacitance. $W_{\rm eff}$ in these devices depends on the diameter D of the tube and the number of tubes N under the gate. Further, we can also keep sufficiently large gate margins (analogous to poly extension in the MOSFET technology) outside the channel area to ensure all nanotubes under the gate without affecting the device footprint. Note that the width W in bulk MOSFETs is defined by the active diffusion and not by the poly extension. This will significantly reduce the probability of any nanotube channel to be left out of the gate region, and hence, a variation in W will not affect the drive current. Similarly, while the dopant fluctuation strongly affects the characteristics of bulk and FinFET devices, the variation in growth-related parameters in nanowire and nanotube FETs such as the diameter will also affect the device characteristics. It has also been demonstrated by using the self-aligned process that nanowire and nanotube devices may not have any gate–source/drain overlap region [1]. Hence, the parasitic capacitance of these devices is dominated mainly by the gate–source/drain fringe (inner and outer) capacitance $C_{\rm fr}$ [6]. Therefore, the impact of process parameter variations on the overall capacitance C_g will be quite different in these devices. In summary, although the source of many parameter variations may be the same, the overall effect is expected to be different in all these devices due to their unique geometrical structures. Table I summarizes the qualitative impact of process parameter variations on the electrostatic characteristics of all four devices. It would now be imperative to quantitatively analyze the performance of these devices under process variation, which is discussed in the following sections.

III. Device Structures and Models

In this section, we describe the basic device structures of nanowire and nanotube FETs that are used in our analysis and the corresponding device models for drive current and capacitance.

A. Device Structures

As shown in Fig. 1(c), top-gated structures of nanowire and nanotube FETs are used in the analysis with no gate–source/drain overlap. Hence, the parasitic capacitance of these devices is considered to be only the gate–source/drain fringe (inner and outer) capacitance $C_{\rm fr}$. $W_{\rm eff}$ in these devices is obtained based on the diameter D of the tube and the number of tubes N under the gate. The $W_{\rm eff}$ variation is considered through D and N variations. Similarly, the variation in tube/wire orientation is considered through an effective channel length $L_{\rm eff}$ variation. A high-K dielectric (i.e., HfO_2) is used for all nanowire and nanotube transistors in our analysis. We also assume ohmic source/drain contacts for both nanowire and nanotube FETs.

The process parameters of such devices are divided into two categories, namely, lithography/geometry-related parameters (Table II) and nanowire/nanotube growth-related parameters such as the diameter D, nanotube chirality, and wire/tube spacing. For a low-voltage operation (as in most digital applications), since the chirality variation in carbon nanotubes does not significantly affect the device electrostatics [7], we therefore neglect chirality of variation in our analysis. The

TABLE I
SUMMARY OF THE IMPACT OF PROCESS VARIATIONS ON THE ELECTROSTATIC CHARACTERISTICS OF NANOSCALE DEVICES (A QUALITATIVE REPRESENTATION). ONLY DOMINANT PARAMETERS THAT HAVE SUBSTANTIAL IMPACT ON DEVICE CHARACTERISTICS ARE LISTED

Parameters variation	Impact on device characteristics							
	Bulk (MOS)		FinFET		NWFET		CNFET	
	I_{on}	C_g	I_{on}	C_g	I_{on}	C_g	I_{on}	C_g
L_{eff}	Strong	Strong	Weak	Strong	Weak	Weak*	Null	Weak*
T_{ox}	Strong	Strong	Strong	Strong	Weak	Weak	Weak	Weak
W	Strong	Strong	Strong	Strong	Null	Strong	Null	Strong
Dopant Fluctuation	Strong	Weak	Strong	Weak	X	X	X	X
L_{un}	X	X	X	X	Weak	Weak	Weak	Weak
D	X	X	X	X	Strong	Weak	Strong	Weak
T_{si} (FinFET)	X	X	Strong	Strong	X	X	X	X

X: Not considered.
*: The effective capacitance is dominated by fringe capacitance [6] and not the quantum capacitance.

TABLE II
ALL PARAMETERS ARE CHOSEN EQUIVALENT TO THE 45 nm TECHNOLOGY. MOST PARAMETERS HAVE THEIR USUAL MEANING, WHEREAS D IS THE TUBE/WIRE DIAMETER, T_{si} IS THE FINFET BODY THICKNESS, H_{sd} IS THE SOURCE/DRAIN METAL THICKNESS, AND L_{un} IS THE GATE–SOURCE/DRAIN UNDERLAP. OPTIMAL NANOWIRE (110 ORIENTATION) AND NANOTUBE DIAMETERS ARE CHOSEN BASED ON [3] AND [8]; WHEREAS, A TYPICAL T_{ox} [1] IS CHOSEN, CONSIDERING ITS INSIGNIFICANT IMPACT ON I_{on} (FIG. 2). ALL SIMULATIONS ARE DONE WITH A 0.9-V SUPPLY (EQUIVALENT TO THE 45 nm TECHNOLOGY), EXCEPT FOR FIGS. 10 AND 11(b)

Parameters		Bulk (MOS)	FinFET	CNFET	NWFET
Litho-graphy and geometry related	L_{eff}	~20nm	~20nm	20nm	20nm
	T_{ox}	1.1nm	1.5nm	8nm	8nm
	W	100nm	100nm	100nm	100nm
	T_g	30nm	30nm	30nm	30nm
	L_{sd}	100nm	100nm	100nm	100nm
	H_{sd}	X	X	7nm	7nm
	L_{un}	X	X	2nm	2nm
Growth	D/T_{si}	X	T_{si}=8.4nm	D=2nm	D=3nm

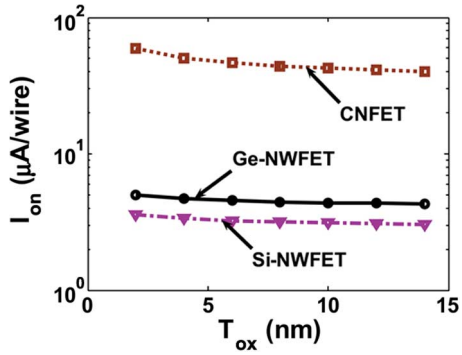

Fig. 2. I_{on} versus T_{ox} of nanowire and nanotube NFETs. HfO_2 was used as an insulator. A work–function difference of 0.45 eV is used for both nanowires and 0 eV for the nanotube.

screening effect due to intertube/interwire spacing variation is also neglected, assuming sufficiently large spacing to avoid interwire coupling. All device parameters are provided in Table II. The parameter values shown in Table II pertain to the 45 nm technology since most analysis results presented in this paper are for this technology, except otherwise mentioned. Optimal diameters of nanotube and nanowires and the orientation (i.e., $\langle 110 \rangle$) of the nanowire are chosen by following the analysis reported in [3] and [8]. Further, we observed that due to the unique geometrical structure, the drive current I_{on} of CNFETs and NWFETs is a weak function of the oxide thickness T_{ox} for a wide range (Fig. 2). A typical oxide thickness is thus chosen based on the above observation. A work-function difference of 0.45 eV is also used for all nanowires and 0 eV for the nanotube.

B. Device Models

All analyses are done, considering ballistic transport in CNFETs and drift-diffusion transport in nanowires. The analytical drive current and capacitance expressions proposed in [9] are used in all SPICE Monte Carlo simulations that involve CNFET devices; whereas, predictive device models [5] are used for the analysis of bulk and FinFET devices under variation. Note that the effect of optical phonons was not considered in the analysis. This is mainly because an analytical device model that is required for statistical analysis was not available, considering the aforementioned effect. However, it is not expected that this will change the outcome of our analysis because optical phonons only change the mean value of the current and has little correlation with process parameter variations.

A quasi-analytical drift-diffusion model of nanowire that was obtained by incorporating the scattering effect into the transport model [10] is used in the analysis. The drift-diffusion current is obtained by analytically integrating the following [11]:

$$I_{ds} = \frac{\mu}{L_{eff}} \int_0^{V_{ds}} Q_{NW}(V_{gs}, V_{ds}) dV \tag{1}$$

where μ is the field-dependent mobility, and $Q_{NW}(V_{gs}, V_{ds})$ is the charge in the nanowire channel obtained, following the approach in [9], as in (2), shown at the bottom of the next page, where α and λ are the nanowire geometry- and V_{ds}-dependent parameters, and ρ_1 and ρ_2 are correction factors. ϕ_{ms}, Ψ_T, and C_{INS} are the work function difference, surface potential

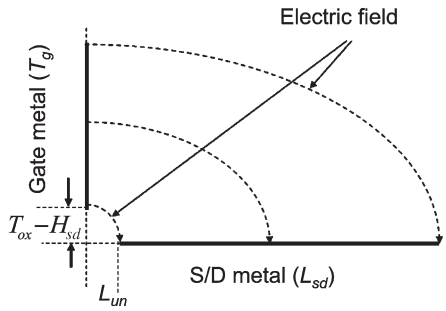

Fig. 3. Cross-sectional view of the electrostatic geometry of the fringing field for outer fringe capacitance (Fig. 1). Inner fringe capacitance is also obtained using the equivalent geometry.

at threshold, and gate insulator capacitance, respectively. A detail description of (2) can be found in [10]. The model was also experimentally verified with the I–V characteristics of a fabricated germanium nanowire PFET device.

As we have mentioned earlier, state-of-the-art nanotube or nanowire devices can be fabricated without any gate–source/drain overlap, and hence, the parasitic capacitance of these devices will be dominated mainly by fringe capacitance [6]. Fig. 3 shows the cross-sectional view of the electrostatic geometry of such a device [see Fig. 1(c)], where the gate electrode metal (height: T_g) is separated from the source/drain metal (length: $L_{\rm sd}$) approximately by $T_{\rm ox} - H_{\rm sd}$ in the vertical direction ($T_{\rm ox}$: oxide thickness; $H_{\rm sd}$: source/drain metal thickness) and by the thin oxide ($L_{\rm un}$) in the horizontal direction, which is used to isolate the gate metal during source/drain metal deposition. The fringe capacitance $C_{\rm fr}$ of this geometry can be analytically calculated using the following equation [12]:

$$C_{\rm fr} = \frac{2\varepsilon W}{\pi}\ln\left[\frac{T_{g,s/d}+\eta T_g+\sqrt{L_{\rm un}^2+(\eta T_g)^2+2T_{g,s/d}\eta T_g}}{L_{\rm un}+T_{g,s/d}}\right] + \frac{k\varepsilon W}{\pi}\ln\frac{\pi W}{\sqrt{L_{\rm un}^2+T_{g,s/d}^2}}e^{-\left|\frac{L_{\rm un}-T_{g,s/d}}{L_{\rm un}+T_{g,s/d}}\right|} \quad (3)$$

where $\eta = \exp[(L_{\rm sd}+L_{\rm un}-L_{\rm un}^2+T_g^2+2T_{g,s/d}T_g^{1/2})/\tau L_{\rm sd}]$, and $T_{g,s/d} = T_{\rm ox} - H_{\rm sd}$. ε is the permittivity of the medium, W is the device width, and k and τ are constants. A detailed description about (3) can be found in [12]. In this analysis, we used SiO_2 as the medium outside the device. We also considered all process parameters as random variables for Monte Carlo simulation in our analysis.

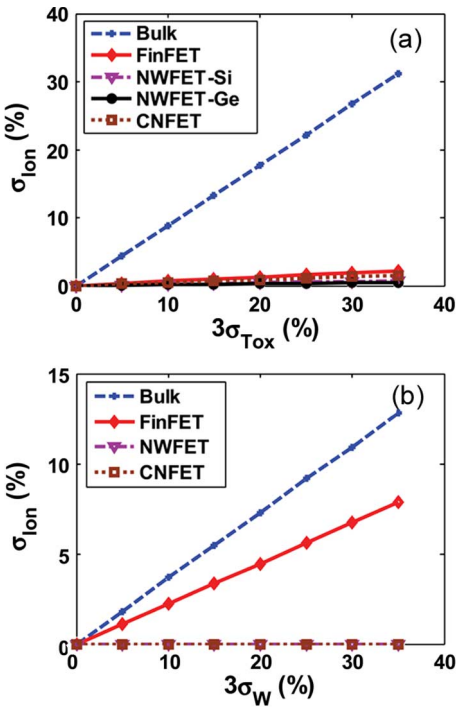

Fig. 4. Sensitivity of $I_{\rm on}$ of an NFET to (a) $T_{\rm ox}$ and (b) W variations. $I_{\rm on}$ of a FinFET device is less sensitive to the W variation than a bulk device due to less narrow-width effect; whereas, it is not sensitive in the NWFET/CNFET devices, as explained earlier (see Fig. 1).

IV. Results and Discussion

A. Impact on Drive Current

As we have discussed earlier, unlike conventional MOSFET devices, most lithography-related parameter variations do not significantly affect the drive current of nanowire and nanotube devices due to their unique geometrical structure. For example, although the variation in $T_{\rm ox}$ and W drastically affects $I_{\rm on}$ of bulk MOSFETs, $I_{\rm on}$ of NWFETs (both Si and Ge) and CNFETs is a weak function of the $T_{\rm ox}$ variation and is independent of W (Fig. 4). Note that, as we have mentioned earlier, W in NWFET/CNFET devices is not the effective channel width and only contributes to the parasitic capacitance without affecting $I_{\rm on}$ (see Fig. 1). On the other hand, though a FinFET's response to the $T_{\rm ox}$ variation is similar to that of an NWFET, it, however, has a strong dependence on the W variation [Fig. 4(b)]. Note also that, in FinFET analysis, W represents the effective channel width, and hence, its variation significantly affects the transistor drive current. However,

$$Q_{\rm NW} = \beta C_{\rm INS}\cdot lambertw\left[\frac{\alpha}{\beta\cdot C_{INS}}e^{(V_{\rm gs}-\phi_{\rm ms})/\beta}\right] \quad \text{for } V_{\rm gs}\le V_T$$

$$Q_{\rm NW} = C_{\rm INS}\left[V_{\rm gs}-\phi_{\rm ms}-\psi_T+\frac{(\rho_1\lambda_1+C_{\rm INS})}{2\rho_2\lambda_2}\right] - C_{\rm INS}\frac{\left[(\rho_1\lambda_1+C_{\rm INS})^2-4\rho_2\lambda_2\left[\lambda_0-C_{\rm INS}(V_{\rm gs}-\phi_{\rm ms}-\psi_T)\right]\right]^{1/2}}{2\rho_2\lambda_2} \quad \text{for } V_{\rm gs}>V_T \quad (2)$$

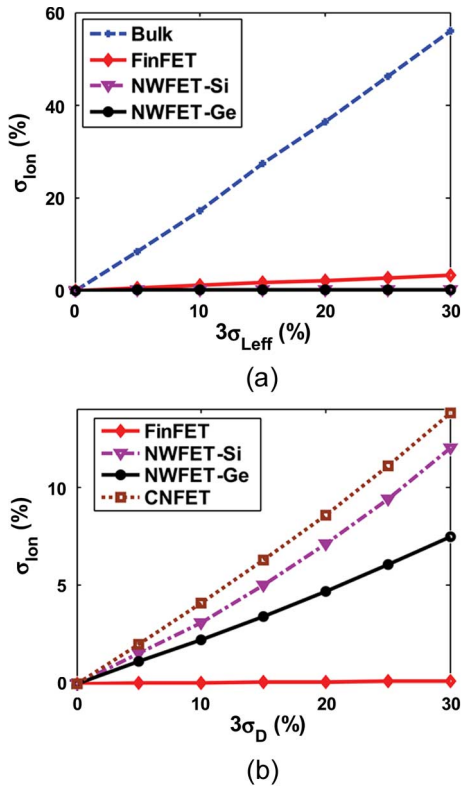

Fig. 5. $I_{\rm on}$ sensitivity to (a) the $L_{\rm eff}$ variation and (b) diameter of nanotube/nanowire and body thickness $T_{\rm si}$ variations of a FinFET. Note that the $L_{\rm eff}$ variation is attributed to both the wire orientation variation and the lithography variation.

a FinFET is less sensitive to the W variation than a bulk MOSFET because of its reduced narrow width effect. Further, though $I_{\rm on}$ of an NWFET is a function of the $L_{\rm eff}$ variation, the impact is expected to be much less than that on a bulk MOSFET or a FinFET due to a negligible short-channel effect [Fig. 5(a)]. Note that the $L_{\rm eff}$ variation is attributed to both the wire orientation variation and the lithography variation. On the other hand, $I_{\rm on}$ of CNFETs will be independent of the $L_{\rm eff}$ variation, considering ballistic transport. The variation in the diameter D, however, will considerably affect $I_{\rm on}$ of both NWFETs and CNFETs [Fig. 5(b)]. The FinFET's negligible sensitivity [Fig. 5(b)] to the body thickness $T_{\rm si}$ variation is attributed to its relatively large $T_{\rm si}$ (8.4 nm) in which regime the energy band of the device is substantially constant. Consequently, its overall $I_{\rm on}$ sensitivity under all parameter variations is comparable to NWFETs/CNFETs, despite its considerable sensitivity to the W variation (Fig. 6). Note that the random dopant effect on bulk and FinFET devices is also included in the analysis. Overall, due to unique geometrical structures, the drive current of FinFET, nanowire, and nanotube transistors are significantly less sensitive to variations than that of bulk MOSFETs (Fig. 6).

B. Impact on Capacitance

Parameter variations also affect the device capacitance, which needs to be analyzed to understand the overall impact of a variation on the performance of any device. We have mentioned earlier (Section II) that the effective device capacitance in NWFETs/CNFETs is dominated by $C_{\rm fr}$ [6], and hence, it will be less sensitive to most geometry-dependent parameter variations such as $L_{\rm sd}$, $L_{\rm un}$, $T_{\rm ox}$, and T_g for logarithmic dependence (Fig. 7). However, it strongly depends on the W variation (Fig. 8). Fig. 9 shows the impact of a variation on the overall gate capacitance C_g, where the linear change demonstrates the dominance of W. C_g's of NWFET/CNFET devices show less sensitivity than those of bulk MOSFET and FinFET devices due to the absence of overlap capacitance.

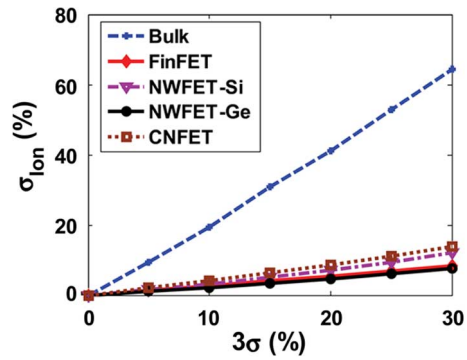

Fig. 6. Overall $I_{\rm on}$ sensitivity to all parameter variations. A random dopant effect is also included in the bulk and FinFET devices.

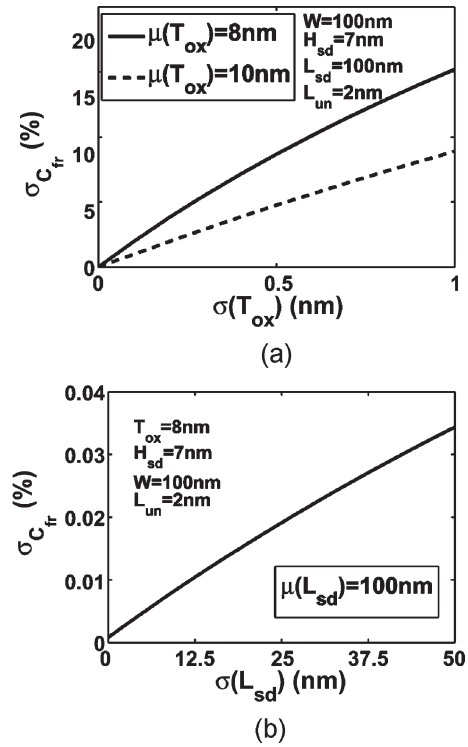

Fig. 7. Sensitivity of NWFET/CNFET fringe capacitance to $T_{\rm ox}$ and source/drain length variations. Due to logarithmic dependence, $\sigma_{C_{\rm fr}}/\sigma_{T_{\rm ox}}$ is less than 1. The effects of gate thickness T_g and underlap $L_{\rm un}$ variations are similar to $L_{\rm sd}$ and $T_{\rm ox}$ variations, respectively, due to geometrical symmetry and, hence, are not shown here.

C. Impact on Circuit Performance

Now that we have discussed the effect of process parameter variations on the drive current and capacitance of nanowire

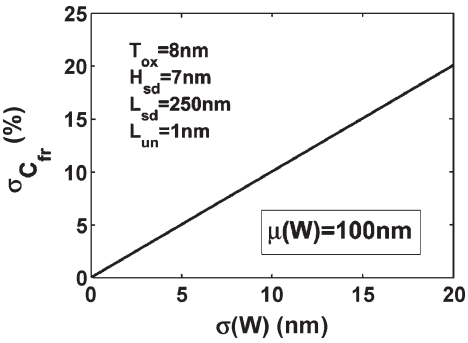

Fig. 8. $C_{\rm fr}$ sensitivity to the W variation. Note that $\sigma_{C_{\rm fr}}$ approximately linearly changes with the W variation. The linear change is due to the linear dependence of $C_{\rm fr}$ on W.

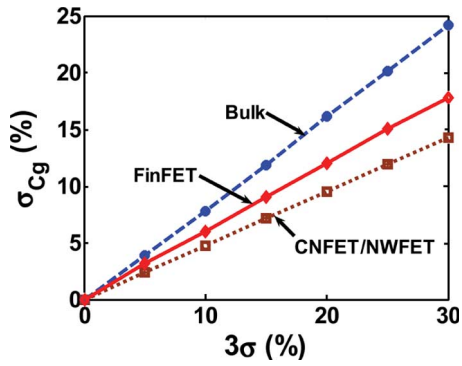

Fig. 9. Overall gate capacitance C_g sensitivity to all parameter variations. The approximate linear response demonstrates the dominance of the W variation. $C_{\rm fr}$ was added to the FinFET device based on [12] because the original model had zero fringe capacitance.

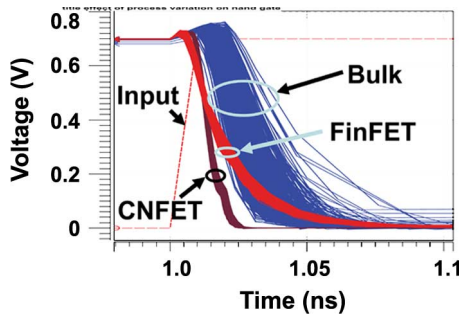

Fig. 10. Delay variation of a two-input NAND with an inverter load at the 32 nm technology node ($V_{\rm dd} = 0.7$ V and $3\sigma = 15\%$). $C_{\rm fr}$ of the FinFET device was modified based on [12]. The NWFET result was similar to that of the CNFET but is not shown due to clarity.

and nanotube FETs, it is now imperative to evaluate the circuit performance of these devices under variation. We compare the performance of a two-input NAND gate under variation at the 45 and 32 nm technologies using HSPICE Monte Carlo simulation. To avoid extremely high complexity in HSPICE Monte Carlo simulation using CNFETs and NWFETs, we used a two-input NAND gate with an inverter load for circuit performance evaluation under process variation. Fig. 10 shows the input/output waveform of CNFET, bulk MOSFET, and FinFET circuits with a 15% (3σ) variation in all process parameters. It can be seen that the performance of both the CNFET and

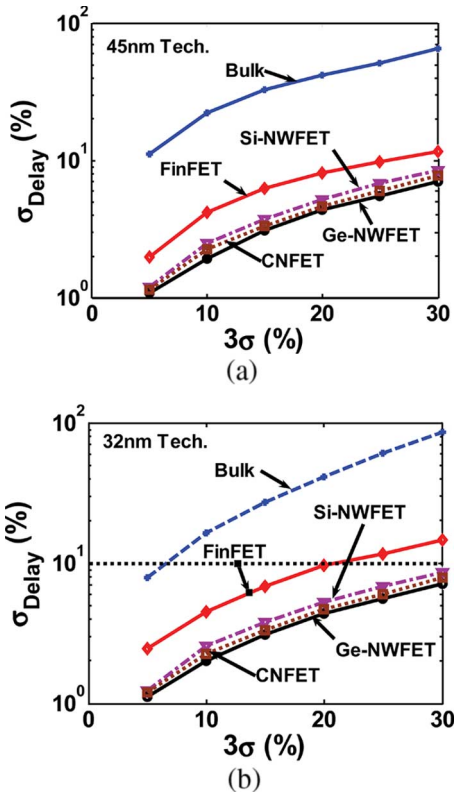

Fig. 11. Delay variation of a two-input NAND gate with an inverter load. (a) At the 45 nm technology ($V_{\rm dd} = 0.9$ V). (b) At the 32 nm technology ($V_{\rm dd} = 0.7$ V).

FinFET devices is significantly less sensitive to process variations than that of the bulk MOSFET. The simulation result of the NWFET was similar to that of the CNFET and is not shown in the figure due to clarity. Further, Fig. 11(a) and (b) compares the delay variation of the aforementioned circuits for different 3σ values at the 45 and 32 nm technologies, respectively. It can be observed that both NWFETs and CNFETs show significantly lower sensitivity (four times less) to variations than bulk MOSFET. Though the performance variation of a FinFET device is also much lower than that of a bulk device, it is, however, considerably larger than that of NWFET/CNFET devices. This further confirms the insensitivity of NWFET and CNFET device performance to many geometry/lithography-related process parameters, as discussed earlier.

Another way of interpreting the results shown in Fig. 11 is that, for a particular allowable performance variation, NWFET and CNFET devices have a much larger margin for process variations than that of a Si bulk MOSFET or FinFET device. For example, assuming that the allowable limit of a delay variation for some products using the 32 nm technology is 10% [see the horizontal dotted line in Fig. 11(b)]; while the margins for process variation (3σ) in Si bulk and FinFET devices are about 7% and 20%, respectively, that of the NWFET or CNFET is much larger than 30%. This suggests that, although the variation in some process parameters of the NWFET or CNFET may be large, there is a unique possibility that these new FETs can be put to practical use to achieve their inherent advantages such as performance and scalability.

V. Conclusion

It is widely believed that process parameter variations are going to drastically limit the prospect of future conventional MOSFET devices and that it will continue to even more severely restrict the performance of emerging devices. However, the analysis above reveals much lower sensitivity of nanotube and nanowire devices to process variations than conventional MOSFETs. We carefully analyzed the impact of process parameter variations on the performance of bulk, FinFET, NWFET, and CNFET devices. It was shown that both NWFET and CNFET devices are significantly less sensitive to stochastic variations such as process-induced variations due to their inherent device structures and geometric properties. This other way implies that for an allowable performance variation, nanowire and nanotube devices will have larger margins for process parameter variations than bulk and FinFET devices. Further, it was shown in [9] that achieving the intrinsic performance advantage of CNFET is quite a challenge in the presence of various parasitics in real circuit layouts. However, the analysis in this paper showed that even if the circuit performance of CNFETs/NWFETs is comparable to conventional complementary metal–oxide semiconductors, these devices will be better off from the system design perspective, because one has to keep lower delay margins due to their significantly less sensitivity to process parameter variations. Hence, one can expect a better overall system performance with CNFET/NWFET devices than their bulk or FinFET counterpart.

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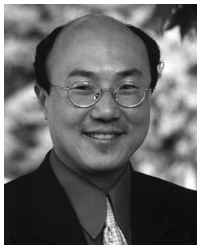

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