Issues in High Frequency Noise Simulation for Deep Submicron MOSFETs

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Outline

- Introduction
- Classical Noise Optimization
- New Noise Optimization for CMOS RF
- Bias Dependent Intrinsic Noise Performance
- Direct Tunneling Current
- Conclusions and Open Questions
- Acknowledgments

Introduction

(RF CMOS)

- Rapid f_t increase of MOSFETs, driven by the microprocessor industry, attracts RF designers.
- Promise of realizing single chip system solution.
- Noise behavior in short channel MOSFETs is not well understood yet, especially for state-of-art MOSFETs technologies.
- Substantial gate leakage current in ultrathin oxides.

Introduction *(Continue)*
(MOSFET Noise)

- Flicker (*1/f*) Noise
  - ✧ Dominant up to few MHz range
- Shot Noise
  - ✧ Dominant in the subthreshold region
  - ✧ Important in MOSFETs with ultrathin oxides below 4nm
- Thermal Noise (Velocity Fluctuation Noise)
  - ✧ Dominant in high frequencies

Classical Noise Optimization

- In general,

$$F = F_{min} + \frac{R_n}{G_s}[(G_s - G_{opt})^2 + (B_s - B_{opt})^2)$$

- Minimum noise is

$$F_{min} = 1 + 2R_n(G_{opt} + G_c)$$

when

$$G_{opt} = \sqrt{\frac{G_u}{R_n} + G_c^2} \approx \sqrt{\frac{G_u}{R_n}}$$

$$B_{opt} = -B_c$$

Classical Noise Optimization (*Continue*)

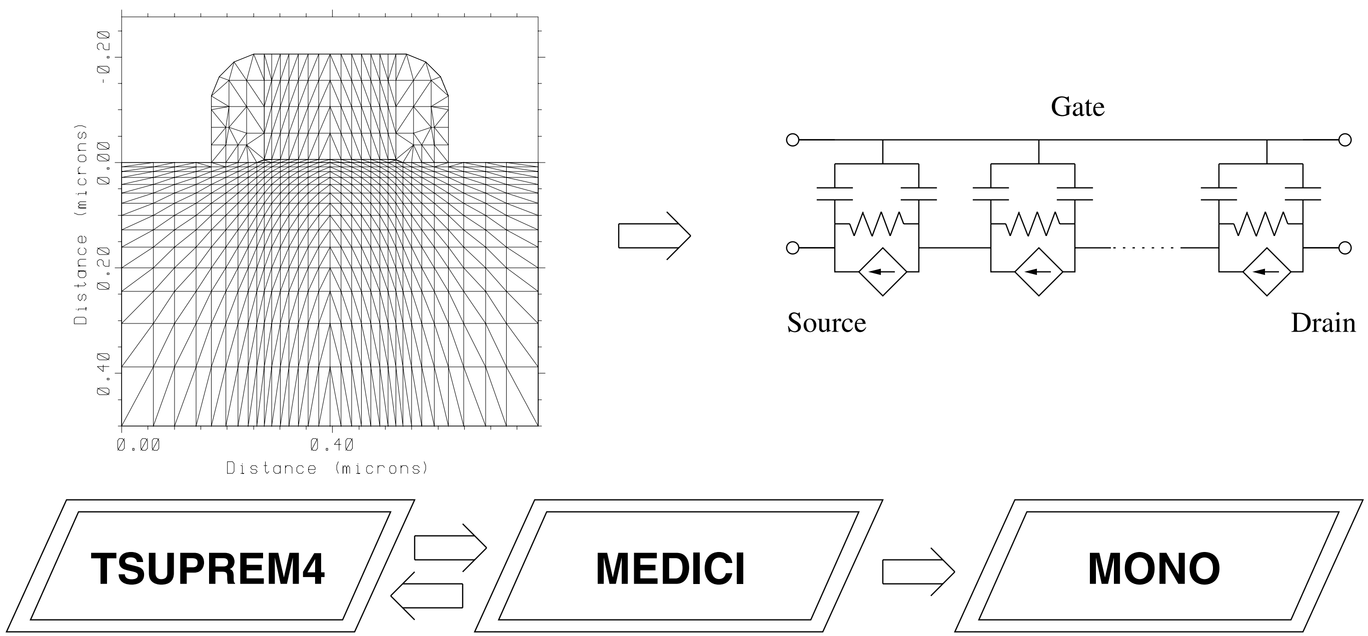
- No relation between the optimum noise match source admittance (Y_{opt}) and the optimum power gain condition.
  - ✧ Possible to minimize the noise figure with little or no gain.
  - ✧ Possible to the minimize the noise figure with a poor impedance match.
- Does not consider power consumption directly.
- Device is given with fixed characteristics.

New Noise Optimization for CMOS

- Permitting selection of device geometries.
  - ✧ Gain-constrained noise optimization.
  - ✧ Power-constrained noise optimization.
- More freedom in bias point selection.
  - ✧ Excess drain noise in short-channel MOSFETs.
  - ✧ Induced gate noise in GHz range (partially correlated to drain noise).
  - ✧ Exhaustive noise information for the entire operating conditions is needed.

Simulation Method

(Hybrid Approach)



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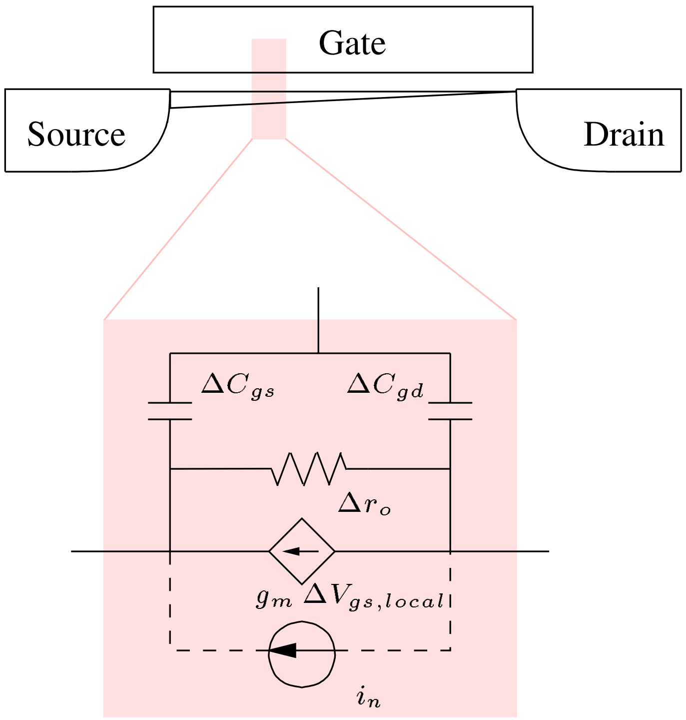
Simulation Method *(Continue)*

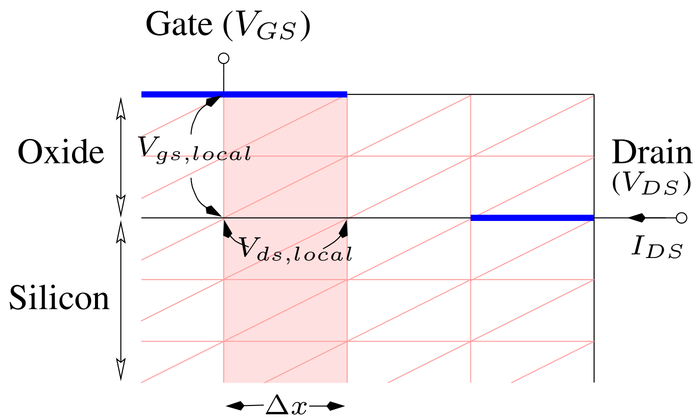
(Hybrid Approach)

- TSUPREM4 (2D process simulator)
  - ✧ Accurate structure and doping for complex processing
- MEDICI (2D device simulator)
  - ✧ Hydrodynamic model captures the physics required in short channel MOSFETs
- MONO (1D MOsfet NOise simulator)
  - ✧ Non-uniform active transmission line + IFM
  - ✧ Fast noise calculation

Simulation Method *(Continue)*

(Interface between 2D and 1D)





$$\Delta C_{gs} + \Delta C_{gd} = \frac{\Delta Q_{inv}}{\Delta V_{gs,local}}$$

$$\Delta r_o = \frac{\Delta V_{ds,local}}{\Delta I_{DS}}$$

$$g_m = \frac{\Delta I_{DS}}{\Delta V_{gs,local}}$$

$$\Delta S_{i_n} = 4\,k\,T_n\,\frac{I_{DS}}{V_{ds,local}}$$

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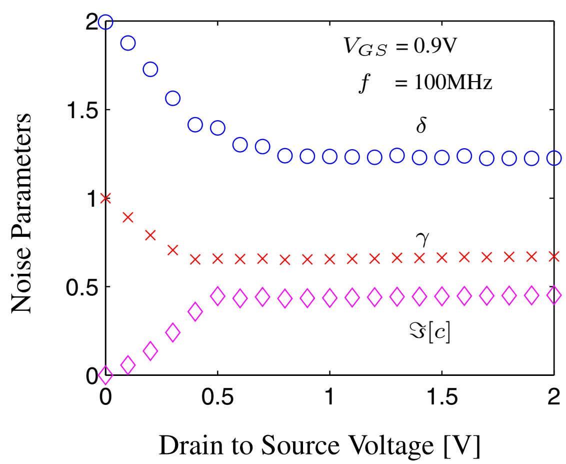
Simulation Method *(Continue)*
(Open Questions)

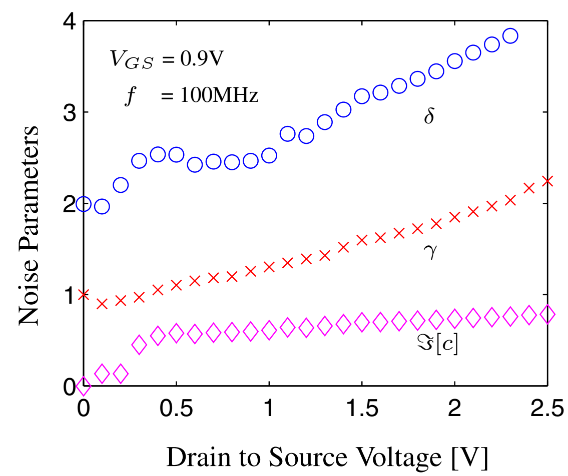
- Applicability of the Langevin stochastic source
  - ✧ Hydrodynamic transport formulation shows promise down to 0.25μm
  - ✧ Nonstationary effects ?
  - ✧ Space correlations ?
- Applicability of conventional IFM
  - ✧ Extendable beyond 0.25μm ? (Especially L_g < 0.1μm)

Bias Dependent Intrinsic Noise Performance

5µm nMOSFET



0.25µm nMOSFET



$$\gamma = \frac{\overline{i_d^2}}{4\,k\,T\,\Delta f\,g_{d0}}$$

$$\delta = \frac{\overline{i_g^2}}{4\,k\,T\,\Delta f\,\Re[Y_{GS}]}$$

$$c = \frac{\overline{i_g i_d^*}}{\sqrt{\overline{i_g^2}\,\overline{i_d^2}}}$$

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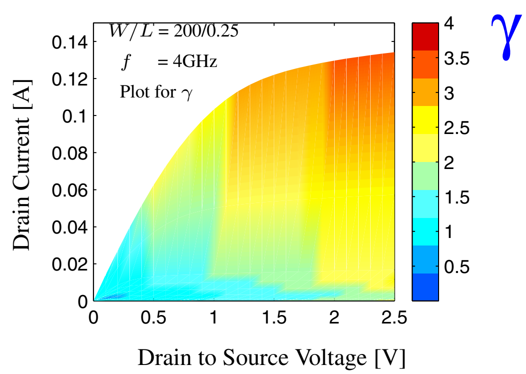
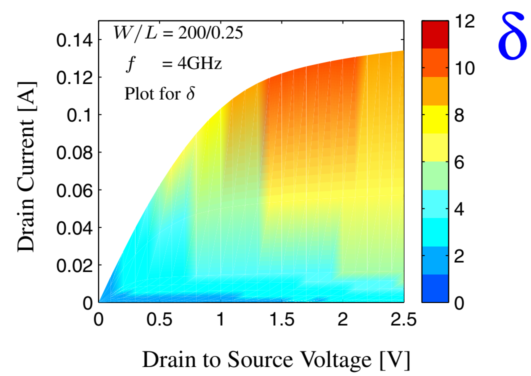
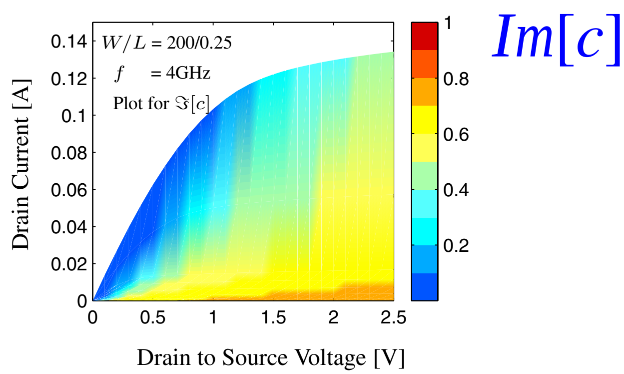
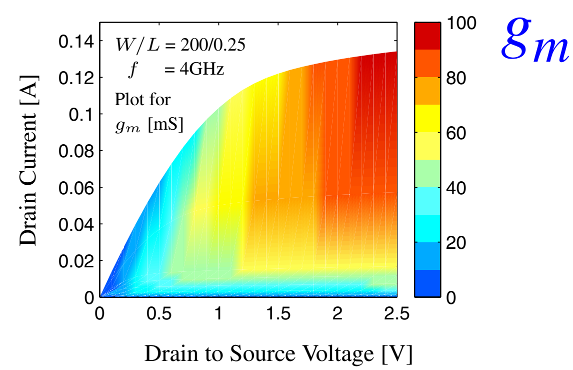
Bias Dependent Intrinsic Noise Performance (*Continue*)





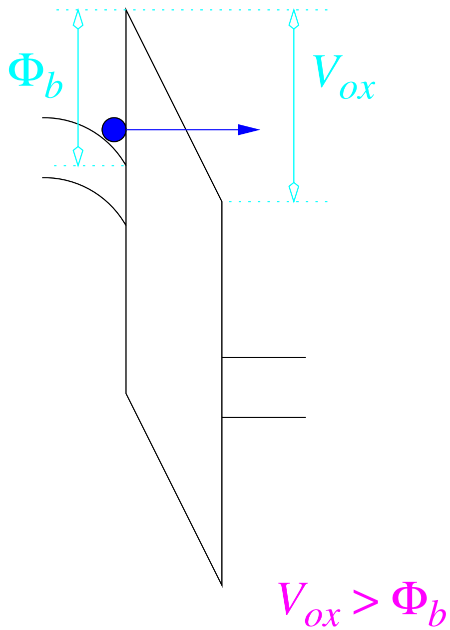




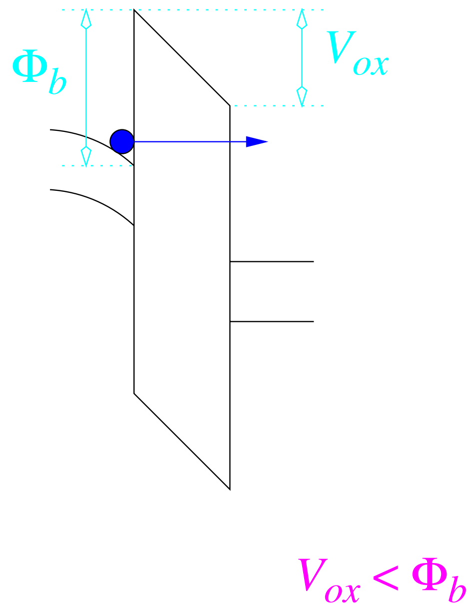
Direct Tunneling

(Tunneling Mechanism)

Fowler-Nordheim Tunneling



Direct Tunneling



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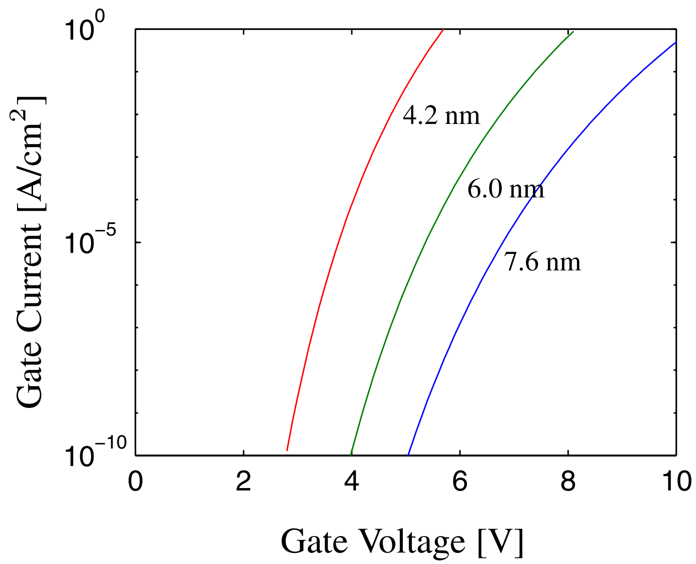
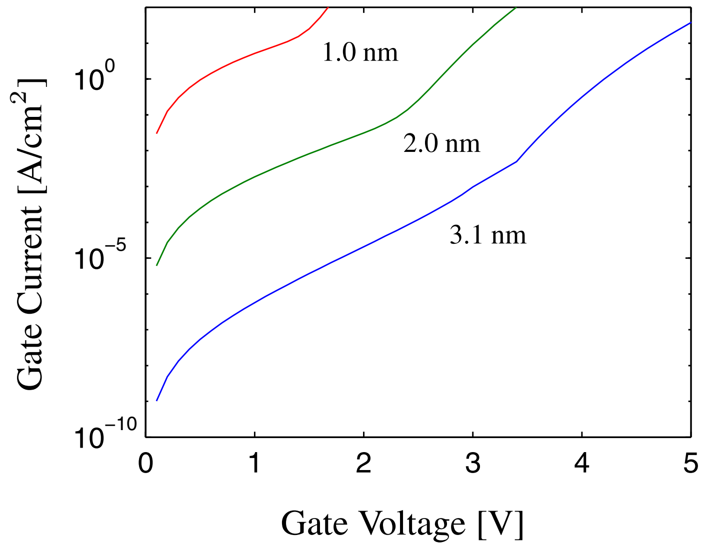
Direct Tunneling *(Continue)*

(Characteristics)

Fowler-Nordheim Tunneling

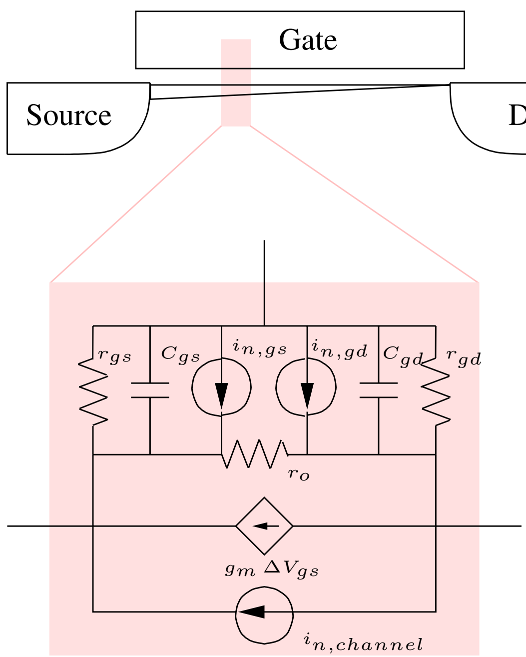


Direct Tunneling



Direct Tunneling *(Continue)*

(Impact on Noise Calculation)



- Additional conductances
  - ✧ Smaller than ωC_{gs} and ωC_{gd} from MHz range
- Extra noise sources
  - ✧ Introduce gate shot noise
  - ✧ Subsequently introduce drain shot noise as well
  - ✧ Uncorrelated with channel noise sources

Direct Tunneling *(Continue)*

(Open Questions)

- Drain shot noise becomes comparable to the drain thermal noise in oxides below 2nm.
- Rigorous modeling of the tunneling current is prerequisite.
  - ✧ Involves multi-dimensional Schrödinger equation (Unsolved problem to date).
  - ✧ Need to take into account various process conditions for on-going dielectric related researches (e.g. oxinitride)

Conclusions and Open Questions

- Bias dependent noise modeling
  - ✧ Must be exhaustive for the entire operating condition as CMOS RF design permits selection of device geometry.
  - ✧ Extendability of the conventional IFM approach beyond 0.25μm (Especially below 0.1μm) is open to question.
- Direct tunneling current
  - ✧ Oxides below 4nm introduces substantially large leakage and subsequently shot noise.
  - ✧ Multi-dimensional Schrödinger equation : unsolved to date

Acknowledgments

- Supported by SRC
  - ✧ Contract No. 98-SJ-116
- Marek Mierzwinski of HP EEsof
  - ✧ prompting and mentoring the project