1-GHz and 2.8-GHz CMOS Injection-locked Ring Oscillator Prescalers

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Abstract

We implemented prescalers that can operate up to 2.8-GHz by exploiting the injection locking phenomena in differential CMOS ring oscillators. We tested a 5-stage, 1-GHz injection-locked modulo-8 prescaler fabricated in a 0.24-µm CMOS technology that consumes 350 µW of power and occupies 0.012 mm^2 of die area. The locking range is 20 MHz and the locked phase noise is -110 dBc/Hz @ 100 kHz. A 2.8-GHz, 3-stage, modulo-4 divider is also presented.

Introduction

Recently there has been extreme interest in short-haul low-power radio systems. A low-power, radio-on-a-chip (RoC) that requires no external components can enable novel applications that are not economically feasible otherwise.

A significant portion of the power budget for any RoC system is allocated to the generation of the RF carrier and local oscillator (LO). Given this need, a low-power, completely integrated frequency synthesizer is required. The major sources of power dissipation in a frequency synthesizer are the VCO and frequency dividers. The VCO's power dissipation is determined by the frequency of operation and the phase noise performance required. Great efforts have been made recently in understanding the fundamentals of low-power operation for communications-grade integrated VCOs [1]-[2]. There is still a great need for a better understanding of low-power techniques for frequency division which is essential to reduce the overall power dissipation of integrated frequency synthesizers.

In this paper, we propose a technique that has the potential of reducing power dissipation of frequency division by up to an order of magnitude compared to conventional digital solutions. We exploited injection-locking in differential CMOS ring oscillators to implement prescalers that can operate at frequencies of up to 2.8 GHz. We also present a simplified model for injection-locked frequency dividers (ILFDs) that helps predict the locking range, and shows design insights that enable further optimization.

Model for Injection-locked Frequency Divider

Recently, there has been a lot of interest in reducing the power dissipation of integrated prescaler/frequency dividers in the 900 MHz range, most of which use current mode logic (CML) [3]. In contrast, injection-locked dividers are commonly used in applications where the frequency of operation is very high, beyond what can be achieved with flip-flop based circuits. Efforts at frequencies beyond 5 GHz have been reported using injection-locking to implement divide-by-2 prescalers in CMOS [4], and Si-BJT [5] technologies. This principle has also found common use at millimeter-wave frequencies in GaAs [6] and SiGe technologies [7]. Our goal is to exploit injection-locked ring oscillators to achieve low-power frequency division.

The injection-locking phenomenon has been known for decades and it was in 1939 that Miller proposed a regenerative frequency divider based on this principle [8]. Miller's divider can achieve division ratios greater than two by using a frequency multiplier in the feedback loop. This frequency multiplier does not have to be explicit, and can represent non-linearities present in the circuit. We can describe an ILFD using a generalized mixer-based model similar to Miller's, since the locking mechanisms are identical.

An ILFD can be modeled as shown in Fig. 1(a). We assumed a single-balanced mixer based on a differential-pair. The input voltage signal of frequency ω_{RF} is injected into the tail device ("Injector") of the differential pair, which produces an RF current which adds to I_{BIAS} flowing into the differential pair ("Mixer"). In general, due to non-linearity of the Injector, this RF current will include a DC component and all harmonics of ω_{RF}. For now, we will assume linear operation of the Injector, and ignore the DC component and higher harmonics of ω_{RF}. For $\omega_0=\omega_{RF}/M$ (where the division ratio M is an integer), the input-referred phase (α) is defined over the range $[-\pi,\pi]$.

Assuming perfect device matching, the differential-pair's transfer characteristic is non-linear with odd symmetry, as shown in Fig. 1(b). When excited by the ILFD's output at ω_0, the mixer's non-linearity produce odd harmonics at $3\omega_0$, $5\omega_0$,

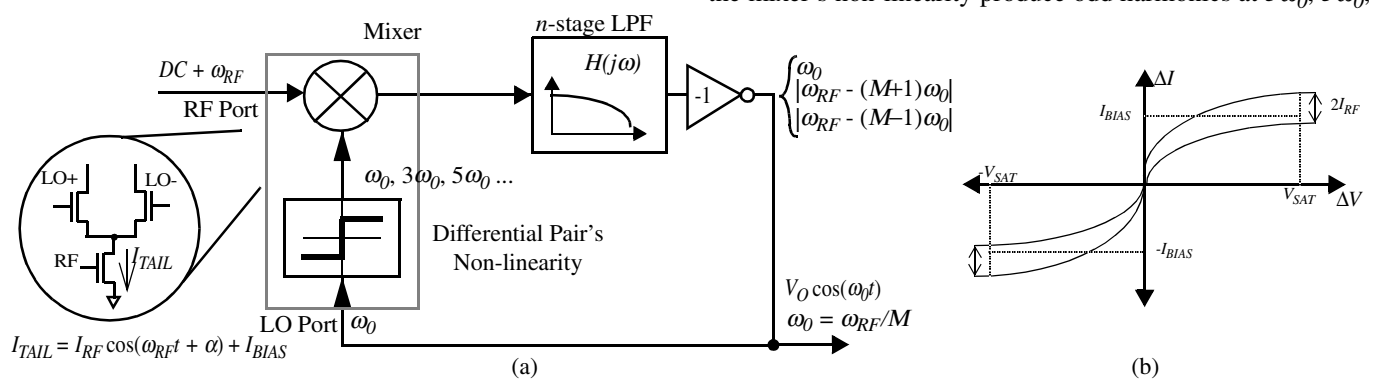

Fig. 1 (a) Model for the injection-locked frequency divider; (b) Nonlinear I-V Characteristic of the Mixer's differential pair.

etc. Therefore, the total current in the tail due to the bias and injected signals (I_{TAIL}) is modulated by ω_0 and its harmonics. The mixer products are filtered and amplified by $H(j\omega)$, which models the low-pass filtering action of n amplifier stages. In the case of a ring oscillator, this low-pass behavior is due to the interaction of the output impedance of each buffer with the input capacitance of the following stage. We assume that the filter substantially suppresses the output products of the mixer whose frequency is higher than ω_0, hence, the output voltage V_O is sinusoidal. This is a fairly good approximation as long as the number of stages is small. This output at ω_0 is fed back to the mixer's LO port, and closes the loop. Note that there is also one net inversion around the loop.

To analyze this model, we determined the open-loop transfer characteristic and separated it into phase and magnitude components. Having the right magnitude and phase shift around the loop are necessary oscillation conditions at ω_0 (Barkhausen's criteria). The ILFD maintains "lock" as long as there is an injected signal at ω_{RF} with sufficient strength. While injection-locked, the output ω_0 tracks ω_{RF}/M within the locking range of the divider. When there is no signal injection, the ILFD free-runs and ω_0 is solely determined by circuit parameters. If there is sufficient gain around the loop, the output amplitude V_O is always large— even at the edge of the ILFD's locking range. In this case, the injection locking dynamics are determined primarily by the phase relationship around the loop (phase-limited) and therefore we can ignore the amplitude expression. A large amplitude is also required to excite the mixer's LO port non-linearity, which is the mechanism that makes possible division ratios greater than two.

Keeping these issues in mind, we will now derive an expression for the locking range of the divider. The low-pass filter $H(j\omega)$ can be modeled by:

$$H(j\omega) = \frac{H_o}{\left(1 + \frac{j\omega}{\omega_0}\tan\left(\frac{\pi}{n}\right)\right)^n} \tag{1}$$

where ω_0 is the frequency of the free-running oscillator. Each stage contributes π/n to the phase, resulting in a total phase lag of 2π around the loop (including the inversion). The filter gain H_0 does not affect the subsequent phase calculations.

The differential pair in the single-balanced mixer has the transfer characteristic shown in Fig. 1(b). For square-law devices, the differential pair's saturation voltage, V_{SAT}, is defined by:

$$V_{SAT} = \sqrt{\frac{(W/L)_{TAIL}}{(W/L)_{DIFF}}} \cdot V_{ODT} \tag{2}$$

where $(W/L)_{DIFF}$ and $(W/L)_{TAIL}$ refer to the sizes of the differential pair and tail devices, respectively, and V_{ODT} is the overdrive voltage $(V_{GS}\text{-}V_T)$ of the tail device. If the voltage swing V_O is large compared to V_{SAT}, the differential pair switches abruptly. In the limit, the output of the mixer becomes

$$\Pi(t) \cdot [I_{RF} \cdot \cos(\omega t + \alpha) + I_{BIAS}] \tag{3}$$

where the mixing function $\Pi(t)$ is a square-wave. Therefore, the Fourier coefficients C_k of the mixing function can be approximated by:

$$C_k = \begin{cases} \frac{1}{k\pi} \cdot (-1)^{(k-1)/2} & \text{for } k = \text{odd} \\ 0 & \text{otherwise} \end{cases} \tag{4}$$

Writing the phase expression around the loop in Fig. 1, we get

$$\text{atan}\left(\frac{\eta_i(C_{M-1} - C_{M+1})\sin\alpha}{C_1 + \eta_i(C_{M-1} + C_{M+1})\cos\alpha}\right) = n\,\text{atan}\left(\frac{\omega}{\omega_0}\tan\left(\frac{\pi}{n}\right)\right) - \pi \tag{5}$$

and

$$\eta_i = \frac{I_{RF}}{2I_{BIAS}} \tag{6}$$

where M is the division ratio, and η_i is the injection efficiency. Using the C_k coefficients from (4), (5) can be solved exactly for the set of values ω/ω_0 which yield a solution for α in the range $[-\pi,\pi]$. To get an approximate analytical expression, we linearize the phase response of the filter around ω_0 as follows:

$$n\,\text{atan}\left(\frac{\omega}{\omega_0}\tan\left(\frac{\pi}{n}\right)\right) \cong \pi + \frac{n\sin\left(\frac{2\pi}{n}\right)}{2} \cdot \frac{\Delta\omega}{\omega_0} \tag{7}$$

where $\Delta\omega = \omega - \omega_0$. Using (7), we can write the following analytical expression for the locking range, $\Delta\omega/\omega_0$:

$$\frac{\Delta\omega}{\omega_0} \cong \frac{4}{n\sin\left(\frac{2\pi}{n}\right)}\,\text{atan}\left(\frac{k_0}{\sqrt{1 - k_1^2}}\right) \tag{8}$$

where:

$$k_0 = \eta_i\left|\frac{C_{M-1} - C_{M+1}}{C_1}\right| \tag{9}$$

and

$$k_1 = \eta_i\left|\frac{C_{M-1} + C_{M+1}}{C_1}\right| \tag{10}$$

In expression (8) we can clearly see the fundamental tradeoffs associated with an ILFD. The locking range is a function of injection efficiency η_i, and the magnitude of the Fourier coefficients C_{M-1} and C_{M+1}. Note that k_1^2 is a small number. For small values of injected signal, k_0 is small, and the locking range increases linearly with the injected signal strength.

The assumption that the mixer's switching function is a square wave is very accurate if the swing ratio $\rho_s = V_0/V_{SAT}$ is much larger than 1. If we break that assumption, the magnitude of the Fourier coefficients gets reduced significantly. As ρ_s gets smaller, the square wave assumption is no longer valid and the coefficient ratios C_k/C_1 are significantly smaller, thus degrading the achievable locking range.

The Injector's efficiency may also be limited by transconductance drop due to velocity saturation, device non-linearity, and drain junction parasitics. Short-channel effects in the Injector cause the device's I-V characteristic to deviate from a square law. Assuming that the active-region characteristic of the tail device is given by $I_{DS} = K \cdot (V_{RF} + V_{ODT})^{\gamma}$, we can redefine injection efficiency as:

$$\eta_i = \frac{I_{RF}}{2I_{DC}} = \frac{V_{RF}}{2V_{ODT}} \cdot \gamma \tag{11}$$

and

$$I_{DC} \cong I_{BIAS} \tag{12}$$

where γ is between 1 and 2. We already know that the locking range is proportional to η_i, and hence to V_{RF}/V_{ODT}.

Due to Injector non-linearities, I_{DC} rises for large injected signals ($I_{DC} > I_{BIAS}$), reducing the injection efficiency and leading to compression of the locking range. This may also

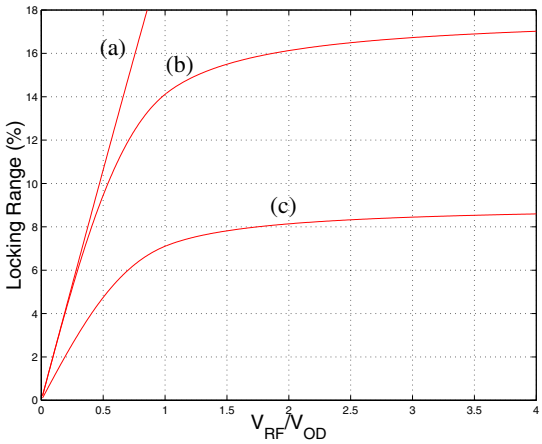

Fig. 2 Locking range of 5-stage, modulo-8 ILFD: (a) Ideal (phase-limited) case; (b) Compression due to Injector non-linearity; (c) Effect of Injector non-linearity and drain junction parasitics (50% RF current loss).

occur for large injected amplitudes, where the Injector is forced into the triode region for part of the cycle. An increase of I_{DC} also affects V_{SAT}, reducing the swing ratio.

Finally, parasitic capacitances within the mixer reduce the magnitude of the RF current which feeds into the switching differential pair. Specifically, the capacitance on the drain of the tail device provides a shunt path for I_{RF}, reducing η_i at high frequencies. Fig. 2 shows the locking range for a 5-stage, modulo-8 ILFD as a function of injected signal.

Circuit Implementation

The prescaler consists of a ring oscillator [Fig. 3(a)] that uses differential buffer delay stages with replica-feedback biasing [10]. Center frequency tuning is achieved by changing the biasing of the buffers which determines the delay through each cell. The layout of the ring oscillator is symmetrical and load balanced to avoid any skewing between the phases. Two ring oscillators were designed, with 3 and 5 buffer stages respectively. Modified cross-coupled symmetric load buffers [Fig. 3(b)] were used for their good supply noise rejection and low 1/*f* noise upconversion characteristics [2].

We injected the RF signal at the tail current source of the first buffer, using it as a single-balanced mixer. The mixing action occurs in the differential pair, and the rest of the buffer stages behave as the multipole filter $H(j\omega)$ that contribute the gain and phase shift required to sustain the oscillation.

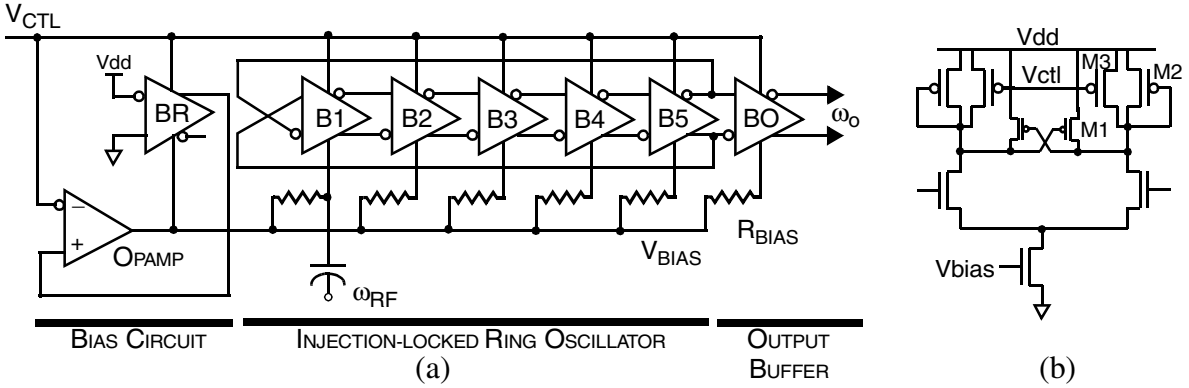

Fig. 3 Schematic diagram of Injection-locked divider: (a) 5-stage ring oscillator, (b) differential delay buffer.

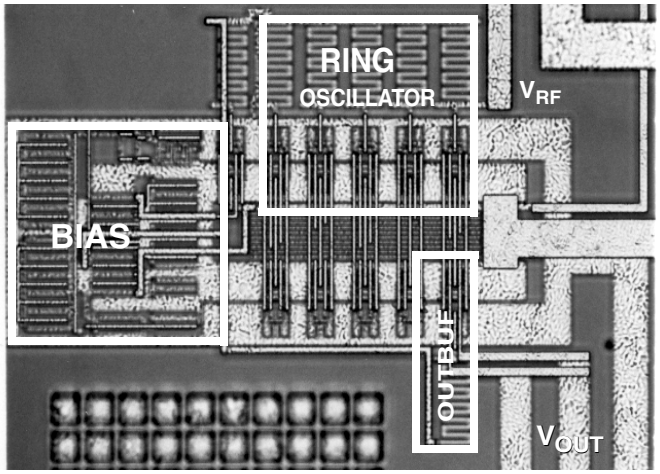

Fig. 4 Die Micrograph of the 5-stage Ring Oscillator Divider..

Measurements

Measured performance of the ILFD is summarized in Table 1. A 5-stage, modulo-8 prescaler has been implemented in a 0.24-µm CMOS technology, as shown in the micrograph of Fig. 4. It occupies 0.012 mm^2 of die area and consumes 233µW of power from a 1.5-V supply. The measured locking range is 20 MHz at 1 GHz for an injected power of 0 dBm. The 3-stage ILFD achieved a locking range of 25 MHz at 2.8 GHz (modulo-4) with -5 dBm of injection. It also occupies 0.012 mm^2 of die area and consumes 993 µW of power.

Our simulation models proved to be too optimistic, the achieved swing is smaller than expected, hence the locking range is smaller than what predicted by Spice. We also observed that the locking range is not symmetric around the free-running frequency of the ILFD, specially at higher injected power levels. This behavior is due to the increase of I_{DC} with the injected signal. Our ring oscillator is current controlled, so an increase of I_{DC} in one stage will make it slightly faster, thus shifting up the free-running frequency.

Discussion

A comparison of recently published data on low-power dividers is shown in Fig. 5 where this work is denoted by [0]. Power efficiency is defined as the ratio of the divider's maximum operation frequency to its power dissipation expressed in GHz/mW. As in [11], to achieve a fair compar-

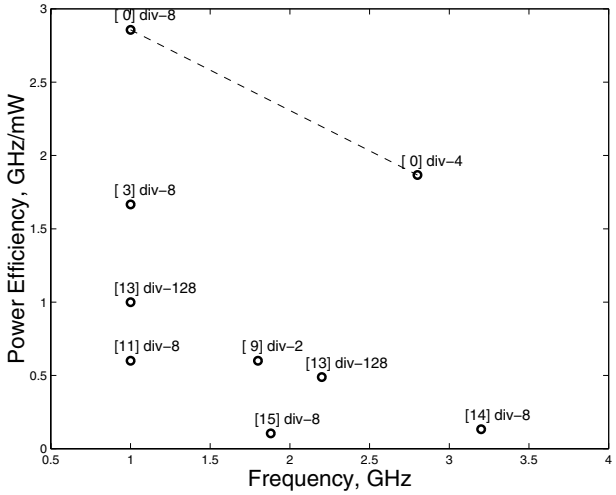

Fig. 5 Comparison of power efficiency (GHz/mW).

ison of the available data, only the consumption of the "core" divider circuits is taken into consideration for calculating the power efficiency. For the 5-stage ILFD, we achieved a power efficiency of 2.86 GHz/mW for a modulo-8 division at 1 GHz. The 3-stage modulo-4 divider achieved 2.82 GHz/mW at 2.8 GHz. To our knowledge, these power efficiencies exceed all published results at comparable frequencies.

To improve the locking range we have to scale down the Injector to lower the parasitics, thus increase the injection efficiency. This improvement is diminished by the onset of short channel effects. The tail node parasitic can also be cancelled by resonating with an inductor [12], but this is not practical at sub-GHz frequencies. We can also increase the output swing and the *W/L* ratio of the Injector, hence increasing the swing ratio. This should be weighted against the resultant increase in parasitic capacitance and power dissipation.

While a flip-flop based divider uses more power as we add more stages, the injection-locked divider does not require more stages and furthermore uses less power for higher division ratios (every stage is operating at ω_0). A single-stage LC injection-locked oscillator may be capable of even lower power operation, but the large area required for integrated inductors makes this choice impractical for sub-GHz operation. Resorting to off-chip inductors will compromise our goal of complete integration.

Conclusions

We exploited injection-locking in differential CMOS ring oscillators for frequency division at 1 GHz and 2.8 GHz. A 1 GHz, modulo-8 prescaler with the highest power efficiency (2.86 GHz/mW) ever reported was fabricated in a 0.24-µm CMOS standard digital process.

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Table 1 : Measured Performance

	5-stage ILFD	***3-stage ILFD***
Injected Frequency	1.0 GHz	2.8 GHz
Free-running Frequency	125 MHz	700 MHz
Phase Noise@100KHz	-110 dBc/Hz	-106 dBc/Hz
Locking Range		
Modulo-2	12.7 MHz (-3dBm)	125 MHz (-3dBm)
Modulo-4	32 MHz (-3dBm)	56 MHz (-5dBm)
Modulo-6	17 MHz (-3dBm)	no-lock
Modulo-8	20 MHz (-3dBm)	no-lock
Power dissipation		
Vdd	1.5 V	3.0 V
Icore	233 µA	331 µA
Ibias	108 µA	661 µA
Core power	350 µW	993 µW
Power efficiency	2.86 GHz/mW	2.82 GHz/mW

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