Phase Noise in CMOS Differential LC Oscillators

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Abstract

An analysis of phase noise in differential cross-coupled tuned tank voltage controlled oscillators is presented. The effect of active device noise sources as well as the noise due to the passive elements are taken into account. The predictions are in good agreement with the measurements for different tail currents and supply voltages. The effect of the complementary cross-coupled pair is analyzed and verified experimentally. A 1.8GHz LC oscillator with a phase noise of -121dBc/Hz at 600kHz is demonstrated, dissipating 6mW of power using spiral inductors.

Introduction

Due to their relatively good phase noise, ease of implementation and differential operation, cross-coupled LC voltage controlled oscillators play an important role in high frequency circuit design.

In this paper we apply the time variant phase noise model presented in [1] to these oscillators. We start with a very brief introduction to this model. Then we calculate the relation between the tank amplitude, the tail current source and the supply voltage. We will continue by analyzing the effect of the active device noise sources as well as the noise sources in the resistive loss in the tank. Finally, we present the experimental results which constitute measurements of the phase noise for different tail currents and supply voltages, showing good agreement with theory. We will analyze the effect of the complementary cross-coupled pair on phase noise and demonstrate it experimentally.

The Time Variant Phase Impulse Response

The phase noise of an oscillator can be characterized by its phase impulse response [1]. This impulse response characterizes the amount of phase shift caused by a given voltage (or current) impulse. To illustrate this concept we consider the ideal LC oscillator shown in Fig. 1. Assume it is already oscillating with a maximum voltage amplitude of V_{max}. The current source in parallel with the tank has a value of zero at all times except at τ, when a current impulse of area Δq is injected. All of this current goes through C as it shows the lowest impedance path for the current and the current through L cannot change instantly. This will cause a sudden change of $\Delta V = \Delta q / C$ in the capacitor voltage.

Depending on the time of injection, τ, the resultant change in the capacitor voltage, ΔV, can cause the oscillator to oscillate with a different amplitude and phase. Fig. 1 demonstrates two extreme illustrative cases. If the impulse is injected when the tank voltage is at its maximum it will cause the tank voltage to change immediately without affecting the excess phase. By excess phase we mean $\phi(t)$ in the argument of $sin[\omega t+\phi(t)]$ and not the whole argument of the sine. The second extreme case shown in Fig. 1 corresponds to an impulse injected close to a zero crossing of the tank voltage. This time, the change in the tank voltage introduces

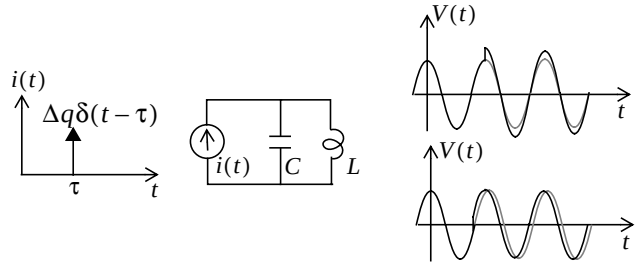

Fig. 1. Phase impulse response of an ideal LC oscillator.

some phase shift and a minimal change in amplitude. The resulting phase shift clearly depends on the instant of injection, τ. It is noteworthy that unlike the amplitude response, once the phase shift is introduced, the oscillator will oscillate with this new phase and will not go back to its previous phase.

The phase shift depends on the instance of injection and is proportional to the injected charge, Δq, for $\Delta q \ll q_{max}$, where $q_{max} = CV_{max}$. Since the system is linear for small injections [1], we can characterize the phase response completely using a time-variant impulse response, $h_\phi(t, \tau)$. This is the impulse response of a system with current (or voltage) as the input and the phase as the output. This impulse response can be written in the following form

$$h_\phi(t, \tau) = \frac{\Gamma(\omega_0 \tau)}{q_{max}} u(t - \tau) \quad \textbf{(1)}$$

where $u(t)$ is the unit step and $\Gamma(x)$ is a periodic dimensionless function with a period of 2π, called the *impulse sensitivity function* (ISF). As its name suggests, the ISF is a function which shows the sensitivity of every point on the waveform to an input impulse. It is large when a given perturbation causes a large phase shift and is small when it results in a small change in the phase [1]. In the case of an LC oscillator, it is zero at the peak and maximum at the zero crossing. By solving the differential equations with the new initial conditions, one can show that for a small Δq, the ISF for an ideal LC oscillator with sine waveform is the cosine function.

Knowing the impulse response for the linear time-variant (LTV) system, we can calculate its output to any arbitrary input using the superposition integral

$$\phi(t) = \int_{-\infty}^{\infty} h_\phi(t, \tau) i(\tau) d\tau = \int_{-\infty}^{t} \frac{\Gamma(\omega_0 \tau)}{q_{max}} i(\tau) d\tau \quad \textbf{(2)}$$

where $i(t)$ represents the input noise current. For a white input noise source with the power spectral density, $\overline{i_n^2}/\Delta f$, it follows from (2) that in $1/f^2$ region, the single sideband phase noise at an offset frequency f_{off} is given by [1]

$$L\{f_{off}\} = \frac{\Gamma_{rms}^2}{8\pi^2 f_{off}^{\ 2}} \cdot \frac{\overline{i_n^2}/\Delta f}{q_{max}^2} \quad \textbf{(3)}$$

where Γ_{rms} is the root mean square (RMS) value of the ISF. In the case of multiple noise sources, $\overline{i_n^2}/\Delta f$ represents the

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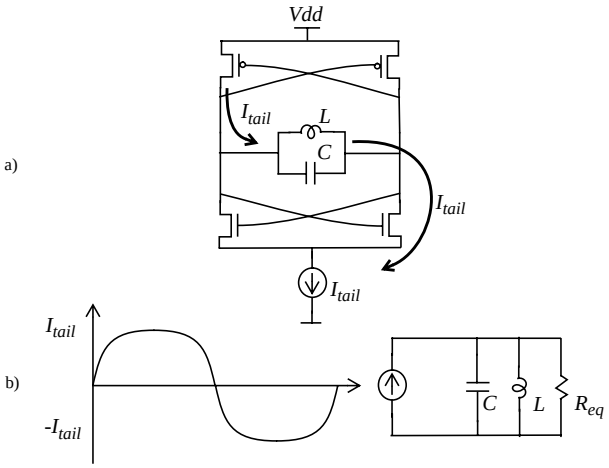

Fig. 2. a) Current flow when the stage is switched to one side b) differential equivalent circuit.

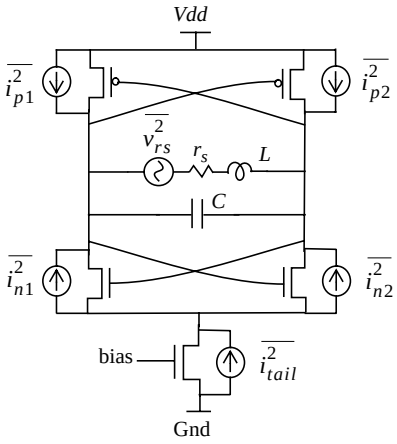

Fig. 3. Complementary LC oscillator with noise sources.

total current noise on each node and is given by the power sum of individual sources.

In the presence of device 1/*f* noise, the device noise power spectrum, $i_n^2/\Delta f$, has a 1/*f* region in addition to the white noise region, where $f_{1/f}$ is the corner frequency.

It can be seen from (2) that the upconversion of low frequency noise, such as 1/*f* noise, is governed by the dc value of the ISF. The corner frequency between $1/f^2$ and $1/f^3$ regions in the spectrum of the phase noise is denoted by f_{1/f^3}, which is related to $f_{1/f}$ through the following relation [1]

$$f_{1/f^3} = f_{1/f} \cdot \left(\frac{\Gamma_{dc}}{\Gamma_{rms}}\right)^2 \quad \textbf{(4)}$$

where Γ_{dc} is the dc value of the ISF. Since the height of the positive and negative lobes of the ISF are determined by the slope of the rising and falling edges of the output waveform, symmetry of the rising and falling edges can reduce Γ_{dc} and hence attenuate the upconversion of 1/*f* noise [1].

Tank Amplitude

In order to apply (3) we need to know q_{max} and hence the voltage swing across the tank. Fig. 2a shows the current flowing in the circuit when it is completely switched to one side. As the tank voltage changes, the current flow through the tank is reversed. The differential part of the circuit can be modeled as a current source switching between I_{tail} and $-I_{tail}$ in parallel with an RLC tank, as shown in Fig. 2b. R_{eq} is the equivalent parallel resistance of the tank which is usually dominated by the limited *Q* of the inductor.

At the frequency of resonance, the admittances of the *L* and *C* cancel, leaving R_{eq}. Harmonics of the input current are strongly attenuated by the LC tank, leaving the fundamental of the input current to induce a differential voltage swing amplitude of $(4/\pi)I_{tail}R_{eq}$ across the tank, for a rectangular current waveform. In practice the input waveform is closer to a sinusoidal wave and therefore

$$V_{max} \approx I_{tail}R_{eq} \quad \textbf{(5)}$$

provides a better approximation. We refer to this regime of operation as current limited.

Note that (5) loses its validity as the amplitude approaches the supply voltage because both NMOS and PMOS pairs will operate in the deep linear region at the peaks of the voltage and hence clip the voltage across the tank. This is equivalent to a reduction in the effective R_{eq}. Therefore for the oscillator of Fig. 2a, the tank voltage amplitude does not exceed V_{dd}, beyond some value of current. We call this region of operation voltage limited.

In the current limited regime, the tank amplitude is solely determined by the tail current source and the tank equivalent resistance and does not depend on the supply voltage. As we will see later, this has an important implication on the power dissipation of the oscillator.

Noise Sources

The effective noise power densities are also required to calculate the phase noise using (3). Fig. 3 depicts the noise sources in the oscillator. In general, these noise sources change periodically because of the periodic changes in currents and voltages of the active devices (*i.e.*, they are cyclostationary). However, we can use the value of their power densities during the most sensitive time (*i.e.* the zero crossing of the differential tank voltage) to estimate the effect of these sources [1]. Fig. 4a shows a simplified model of the sources in this balanced case. Converting the current sources to their Thevenin equivalent and writing KVL one obtains the equivalent differential circuit shown in Fig. 4b. Note that the parallel resistance is canceled by the negative resistance exhibited by the positive feedback. Therefore the total differential noise power due to the four cross-coupled devices is

$$\overline{i_{cc}^2} = \frac{1}{4}(\overline{i_{n1}^2} + \overline{i_{n2}^2} + \overline{i_{p1}^2} + \overline{i_{p2}^2}) = \frac{1}{2}(\overline{i_n^2} + \overline{i_p^2}) \quad \textbf{(6)}$$

where $i_n^2 = i_{n1}^2 = i_{n2}^2$ and $i_p^2 = i_{p1}^2 = i_{p2}^2$. Noise densities $i_n^2/\Delta f$ and $i_p^2/\Delta f$ are given by

$$\overline{i_n^2}/\Delta f = 4kT\gamma\mu C_{ox}\frac{W}{L}(V_{GS} - V_T) \quad \textbf{(7)}$$

where μ is the mobility of the carriers in the channel, C_{ox} is the oxide capacitance per unit area, *W* and *L* are the width and length of the MOS device, respectively, V_{GS} is the dc gate source voltage and V_T is the threshold voltage. Equation

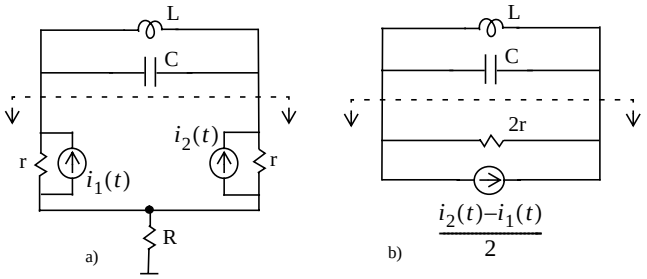

Fig. 4. a) Simplified model for the device noise sources, b) differential equivalent circuit.

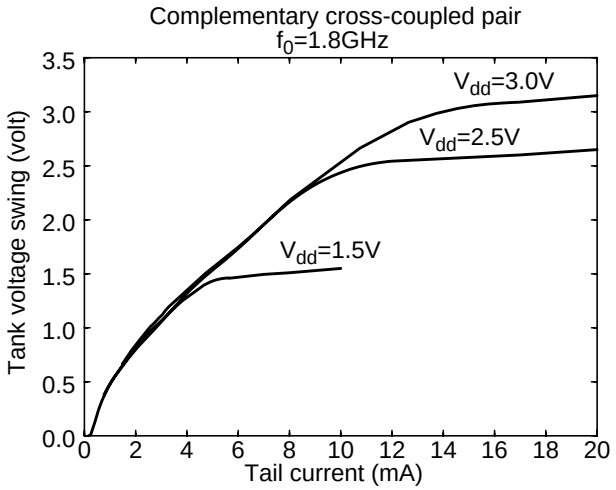

Fig. 5. Simulated tank voltage amplitude vs. tail current source.

(7) is valid for both short and long channel regimes of operation. However γ is around 2/3 for long channel mode while it is between 2 and 3 for the short channel region. [2]

In addition to these sources, the contribution of the effective series resistance of the inductor, r_s, caused by ohmic losses in the metal and substrate is given by

$$\overline{i_{rs}^2}/\Delta f = 4kT\frac{r_s C}{L} = \frac{4kT}{R_p} \quad \textbf{(8)}$$

where $R_p \approx Q^2 r_s = (L\omega_0)^2/r_s$ is the equivalent parallel resistance.

Note that the noise in vicinity of ω_0 of the tail current source has a minimal effect on the differential noise current and it can be shown that its noise around $2\omega_0$ affects the phase noise. Also its low frequency noise such as $1/f$ noise introduces phase noise through asymmetry as discussed earlier and in more detail in [1]. The $1/f$ noise in the cross-coupled devices is upconverted similarly.

Experimental Results and Conclusion

A complementary VCO with the same topology as Fig. 2, is implemented in a 0.25μm epi CMOS technology which allows five layers of metal to be used. Two square inductors in series are laid out symmetrically in metal 3, 4 and 5. The series combination of the two constitutes the tank inductor. Each inductor is 230μm on the side and has 4 turns. Vias are used across the inductors to keep the three metal layers at the same potential. The vias are interleaved to minimize the parallel capacitance of the inductor and to maximize the self-resonance frequency. Field solver simulation of this inductor predicts an inductance of 2.0nH and an effective Q of 7.5 at 1.8GHz which translates to an effective series resistance of r_s=3.02Ω for each inductor.

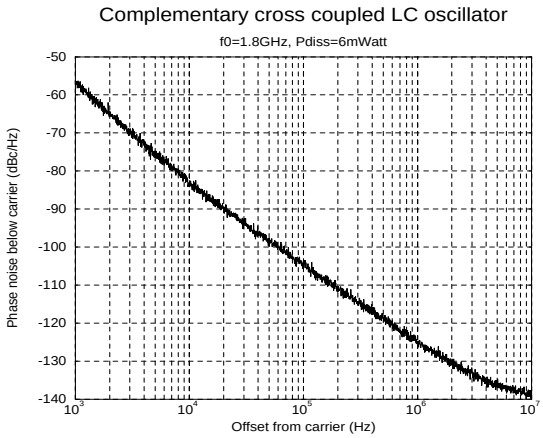

Fig. 6. Phase noise vs. offset frequency for V_{dd}=1.5V and I_{tail}=4mA

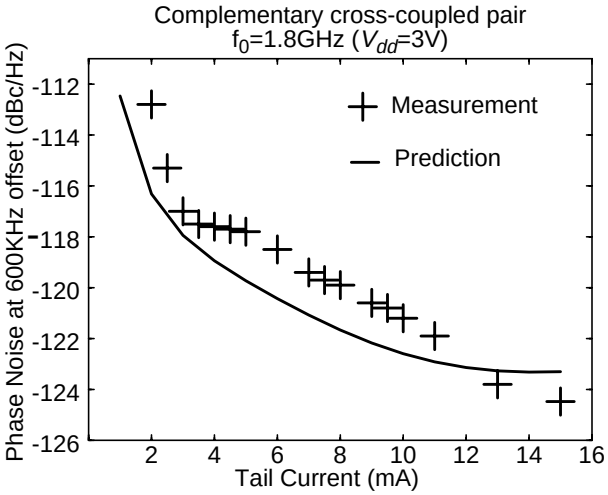

Fig. 7. Predicted and measured phase noise at 600kHz offset vs. I_{tail}.

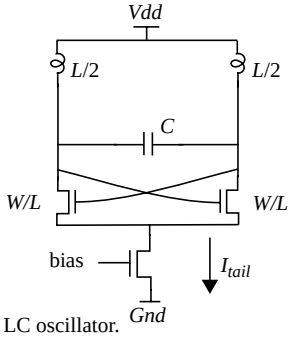

Fig. 8. All-NMOS LC oscillator.

Tank amplitude vs. tail current source is simulated for three different supply voltages and is shown in Fig. 5. As can be seen in the current limited region, the tank amplitude is proportional to the tail current, while in the voltage limited regime, it is limited by V_{dd}.

A phase noise vs. offset frequency plot for this oscillator running at 1.8GHz with a 1.5V supply and 4.0mA tail current is shown in Fig. 6. The VCO demonstrates a phase noise

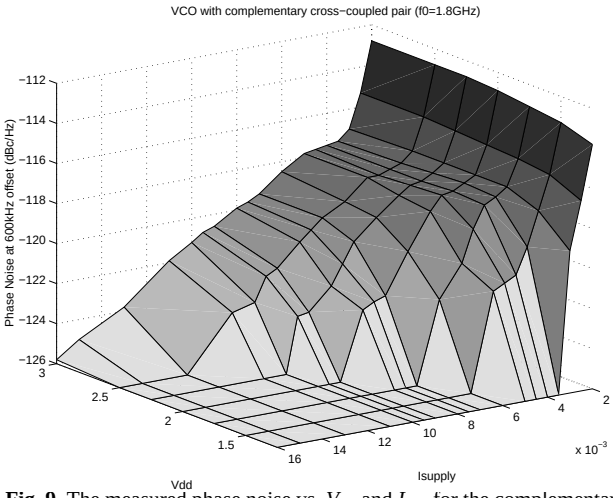

Fig. 9. The measured phase noise vs. V_{dd} and I_{tail} for the complementary LC oscillator.

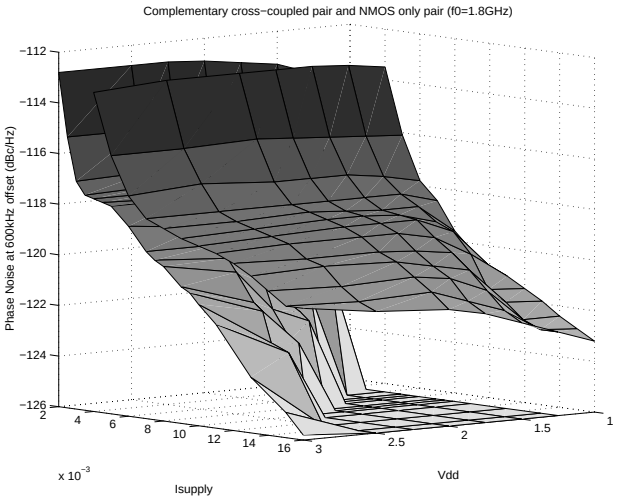

Fig. 10. The measured phase noise for the complementary and NMOS only.

of -121.0dBc/Hz at 600kHz offset, dissipating 6mW of power. An open drain differential pair is used as an output buffer and the output signal is taken from the drains of the differential pair transistors.

The VCO can be tuned using two different methods. A tuning range of 10% can be achieved using a pair of back-to-back connected MOS capacitors used as varactors. As a parallel tuning method, a pair of NMOS devices in series with metal to metal capacitors are used. This method allows a tuning range of 9%. Although it degrades the phase noise in the middle of the tuning range, it does not affect phase noise significantly at the two ends of the tuning range. Therefore using the NMOS as a switch and using the MOS capacitor to fine tune the frequency, a tuning range of 17% is achieved without significantly degrading the phase noise.

Fig. 7 shows a plot of phase noise at 600kHz vs. the tail current with a 3.0V supply. The solid line shows the prediction obtained using (3), (5), (6) and (8). A sinusoidal waveform and therefore a Γ^2_{rms} of 0.5 is assumed although a more accurate analysis to obtain Γ_{rms} can be performed. Good agreement between the theoretical predictions and measurements is observed for different bias points. To gain a better understanding of the trade-offs involved, the phase noise at 600kHz is measured for different values of the supply voltage and tail current. The result is shown in Fig. 9 where the x-axis shows the supply voltage and the y-axis is the tail current. The measured data points are shown as the nodes on the 3D mesh. Note that the bias points not achievable are shown as a flat surface. As can be seen from this graph as well as Fig. 7, increasing the tail current will improve the phase noise due to the increase in the oscillation amplitude. It also can be seen that the phase noise has a fairly weak dependence on the supply voltage, improving for lower voltages. This can be attributed to smaller voltage drops across the channel on the MOS devices which reduces the effect of velocity saturation in the short channel regime and hence lowers γ. These two observations suggest that to achieve the lowest phase noise for a given power dissipation, we should use the lowest supply voltage and the highest tail current. As can be seen from Fig. 9, the lowest achieved phase noise is -125.7dBc/Hz at 600kHz, which occurs for a supply voltage of 3.0V and a tail current of 16mA.

To investigate the effect of the PMOS devices, an all-NMOS VCO with the same tank inductor is implemented as shown in Fig. 8. The phase noise of this VCO is measured for different supply voltages and tail currents. The result is plotted together with the data from the original VCO replicated in Fig. 10. Note that the all-NMOS VCO exhibits inferior phase noise for all the measured bias points.

There are several reasons for the superiority of the complementary structure over the all-NMOS structure. The complementary structure offers better rise and fall time symmetry which results in less upconversion of $1/f$ noise and other low frequency noise sources. It also offers higher transconductance for a given current, which results in a better start-up behavior. Also the dc voltage drop across the channel is larger for the all-NMOS structure since the dc value of the drain voltage is V_{dd}. This results in stronger velocity saturation and a larger γ. As long as the oscillator operates in the current limited regime, the tank voltage swing is the same for both oscillators. However if operation deep in the voltage limited region is desired (which is seldom the case), all-NMOS structures can offer a larger voltage swing.

Acknowledgments

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