A 5GHz, 32mW CMOS Frequency Synthesizer With an Injection Locked Frequency Divider

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I. abstract

A fully integrated 5GHz phase locked loop– (PLL–) based frequency synthesizer is designed in a 0.24μm CMOS technology. A voltage–controlled differential injection–locked frequency divider (VCDILFD) is used as the first frequency divider in the PLL feedback loop to reduce power consumption and eliminate the need for an off–chip frequency divider. The total synthesizer power consumption is 32mW. The phase noise is measured to be -101dBc/Hz at 1MHz offset frequency. The PLL bandwidth is 300kHz and the measured spurious level at the adjacent channel is less than -54dBc.

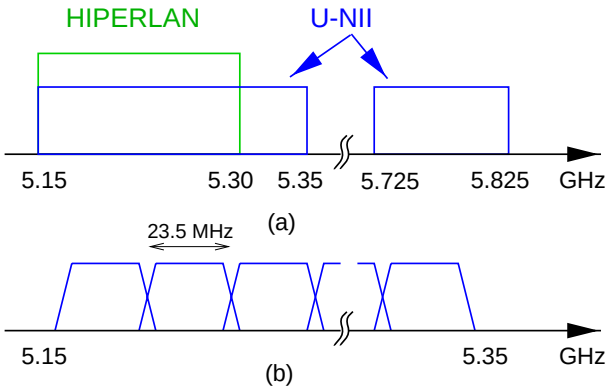

Fig. 1. (a) U–NII and HIPERLAN frequency bands. (b) Channel allocation in a U–NII band WLAN system.

II. Introduction

The demand for high data rate wireless local area networks (WLANs) with low power consumption is rapidly increasing. The unlicensed national information infrastructure (U–NII) band provides 300MHz of spectrum at 5GHz for wireless communications (Fig. 1(a)). The lower 200MHz of this band (5.15–5.35GHz) overlaps the high–performance radio LAN (HIPERLAN) frequency band. This frequency band is divided into 8 channels, each 23.5MHz wide (Fig. 1(b)). In this paper we examine the design of a fully integrated integer–N frequency synthesizer as a local oscillator (LO) for a U–NII band WLAN system. We also demonstrate the advantage of a voltage–controlled differential injection–locked frequency divider (VCDILFD) as a low power frequency divider in this high frequency synthesizer.

III. Synthesizer design

Fig. 2 shows the block diagram of the frequency synthesizer. Channel selection is performed by changing the division ratio ($\div$M) in the feedback path of the phase locked loop (PLL). To reduce power consumption and avoid an off–chip frequency divider, a low–power voltage–controlled differential injection–locked frequency divider [2],[3],[4] is used to perform the first divide–by–two operation in the PLL feedback loop. As a result of this divide–by–two the LO spacing is twice the reference frequency.

The synthesized LO frequency is $\frac{16}{17}$ of the received carrier frequency. This choice of LO frequency not only eases the issue of image rejection in the receiver [5], but also facilitates the generation of the second LO, which is $\frac{1}{16}$ of the first LO, with the same synthesizer. The frequency separation between adjacent LO signals (LO spacing) is $\frac{16}{17}$ of the channel spacing.

The variable frequency divider ($\div$M) consists of a $\div 22/23$ dual modulus prescaler followed by the program and pulse swallow counters. Only one ripple counter is used for both program and pulse swallow counters. The program counter generates one output pulse for every 10 input pulses. The output of the pulse swallow counter is controlled by the three channel select bits to perform the channel selection. A total frequency multiplication factor of 440 to 454, in steps of two, is performed from an 11MHz reference frequency. The output frequency is thus programmable from 4.840GHz to 4.994GHz in 22MHz steps.

The prescaler consists of three dual modulus divide–by–2/3 and one divide–by–2 frequency divider made of source–coupled logic (SCL) flip–flops and gates (Fig. 3). The modulus control (MC) input selects between the divide–by–22 and divide–by–23.

IV. Circuit implementation

A. VCO

Fig. 4 shows the schematic of the VCO. Two cross–coupled transistors, M1 and M2, generate the required negative impedance to cancel the losses of the LC tank. On–chip spiral inductors with patterned ground shields [8] are used in this design. The two main requirements are low phase noise and low power consumption. To reduce both power consumption and phase noise, the spiral inductors should be designed such that the effective parallel impedance of the LC tank at resonance is maximized. Therefore, assuming that the inductors are the main sources of loss in the tank, the LQ product should be

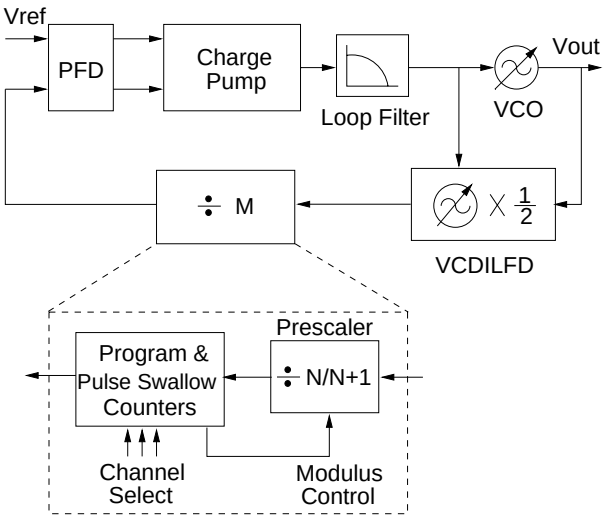

Fig. 2. Frequency synthesizer block diagram.

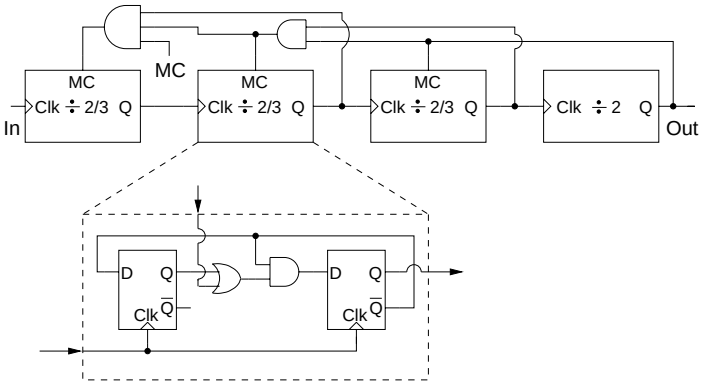

Fig. 3. Block diagram of the prescaler.

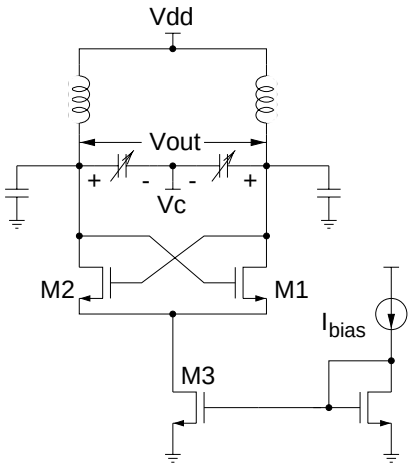

Fig. 4. Schematic of the VCO.

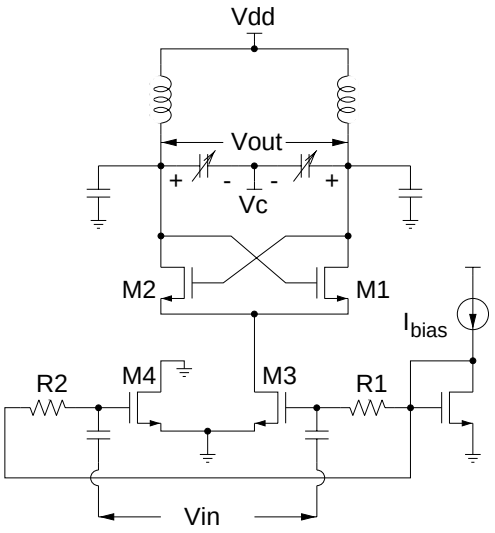

Fig. 5. Schematic of the VCDILFD.

maximized, where L is the inductance and Q is the quality factor of the spiral inductors. It is important to realize that maximizing L does not necessarily maximize the LQ product.

To design the spiral inductor, we use the same inductor model reported in [7]. The inductance is first approximated with a monomial expression as in [1]. Convex optimization is used next to find the inductor with the maximum LQ product. The inductors in this design are 3.3nH each with a quality factor of 11 at 5GHz.

Accumulation mode MOS varactors [6] are used in this design. Each varactor is laid out with 14 fingers which are 3μm wide and 0.5μm long. The quality factor of this varactor at 5GHz is estimated to exceed 60. The losses of the LC tank are thus mainly due to the inductors.

B. VCDILFD

The schematic of the VCDILFD is shown in Fig. 5. It has the same structure as the VCO shown in Fig. 4 with the incident signal (the VCO output) being injected into the gate of M3. Transistor M4 is used to provide a symmetric load for the VCO.

Unlike conventional digital frequency dividers, injection–locked frequency dividers (ILFDs) are narrowband in nature. By designing the ILFD as a voltage–controlled ILFD whose control node is tied to the VCO control voltage (Fig. 4), the center frequency of the ILFD tracks the VCO oscillation frequency. Thus the narrow locking range of the ILFD does not limit the tuning range of the PLL beyond what is determined by the VCO.

As in the VCO design, on–chip spiral inductors with patterned ground shields are used in the VCDILFD. To maximize the locking range of the ILFD, the largest practical inductance, L, should be used [4]. This inductance criterion may not maximize the LQ product (required for the minimum power consumption). Convex optimization is thus used to design an inductor with the maximum inductance such that LQ product is large enough to satisfy the specified power budget. The inductors in this design are 12nH each with a quality factor of 5.8 at the divider output frequency (2.5GHz). The varactors used in the VCDILFD are 0.5μm long accumulation mode MOS capacitors with twelve 3μm wide fingers.

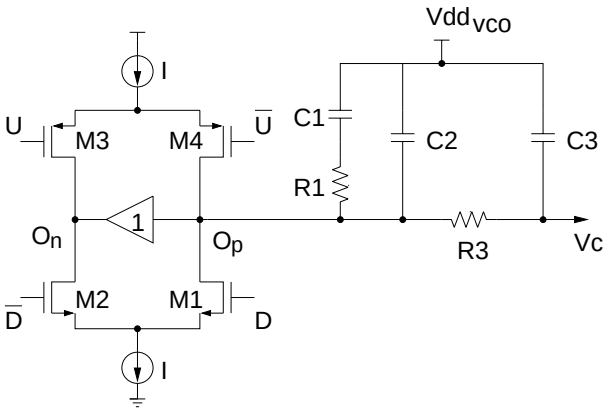

Fig. 6. Simplified schematic of the charge pump and loop filter.

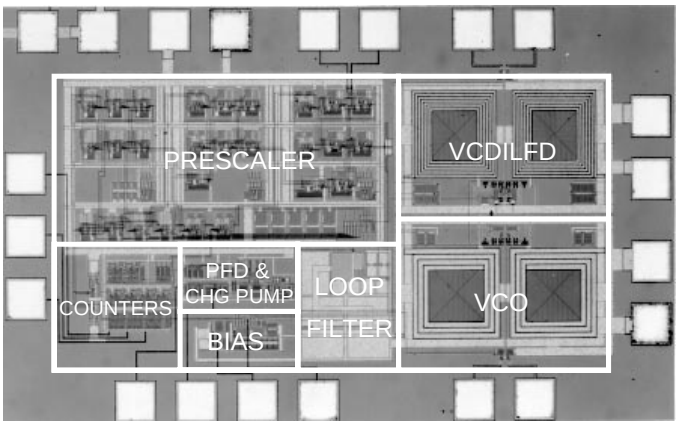

Fig. 7. Die micrograph.

C. Charge pump and loop filter

Fig. 6 shows the circuit diagram of the charge pump and loop filter. Resistor R_1 and capacitor C_1 generate a pole at the origin and a zero at $\frac{1}{R_1 C_1}$. Capacitor C_2 and the combination of R_3 and C_3 are used to add extra poles at frequencies higher than the PLL bandwidth to reduce reference feedthrough and decrease the spurious sidebands at harmonics of the reference frequency. The PLL is thus designed as a fourth–order loop with a bandwidth of about 300kHz.

The charge pump shown in Fig. 6 has a differential architecture. However, only a single output node, O_p, drives the loop filter. To prevent the node O_n from drifting to the rails when neither of the up and down signals (U and D) is active, the unity gain buffer shown in Fig. 6 is placed between the two output nodes. This buffer keeps the two output nodes at the same potential and thus reduces the charge pump offset. The power of the spurious sidebands in the synthesized output signal is thereby reduced. In this charge pump the current sources are always on and the PMOS and NMOS switches are used to steer the current from one branch of the charge pump to the other. This charge pump thus has superior leakage performance compared to charge pumps that switch the up and down current sources.

V. Measurement Results

The frequency synthesizer is designed in a 0.24μm CMOS technology. Fig. 7 shows the die micrograph of the synthesizer. The die area is 1.6mm^2 (1mm $\times$ 1.6mm), including pads.

The VCO and VCDILFD are biased at 1.5V while the rest of the synthesizer is biased at 2V. The choice of the 1.5V supply for the VCO and VCDILFD is to achieve a larger tuning range. The accumulation mode MOS capacitors in this technology have a flat–band voltage around zero volts. Thus to get the full range of capacitor variation the control voltage should be able to exceed the VCO and VCDILFD supply to produce a net negative voltage across the varactors (Fig. 4 and 5). More than 370MHz of VCO tuning range is achieved for a 1.5V variation of the control voltage (Fig. 8).

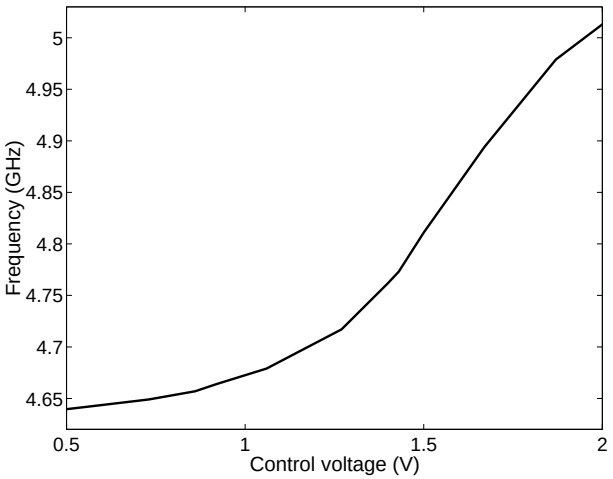

Fig. 8. VCO tuning range.

Fig. 9 displays the synthesized output spectrum. The spurious sidebands are primarily due to the mismatches in the charge pump. The spurious tones at 11MHz offset from the center frequency are more than 45dB below the carrier. The spurs at the adjacent channels are at -54dBc. The required sensitivity for this system is about -74dBm and the maximum signal level is -20dBm [5]. Thus when the desired signal is at its minimum level the signal in the adjacent channels should not be stronger than -30dBm for a minimum 10dB signal–to–interference ratio.

The phase noise measurement result of the synthesizer output signal is shown in Fig. 10. The phase noise at small offset frequencies is mainly determined by the phase noise of the reference signal. The phase noise measured at offset frequencies beyond the PLL bandwidth is the inherent VCO phase noise. The phase noise at 1MHz offset frequency is measured to be -101dBc/Hz. The phase noise at 22MHz offset frequency is extrapolated to be -127.5dBc/Hz. Therefore the signal in the adjacent channel can be 44dB stronger than that of the desired channel for a 10dB signal–to–interference ratio.

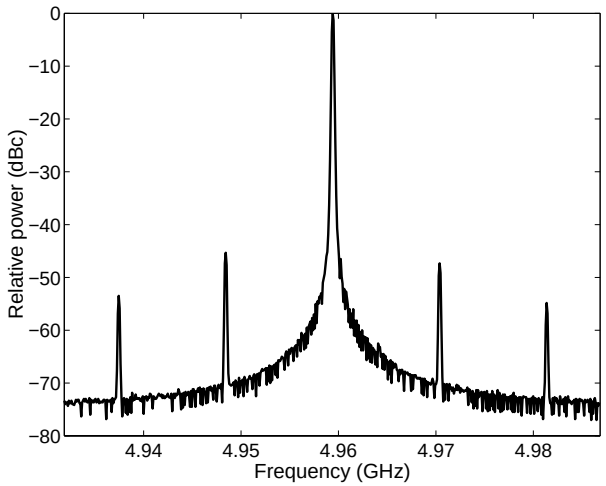

Fig. 9. Spectrum of the synthesizer output signal.

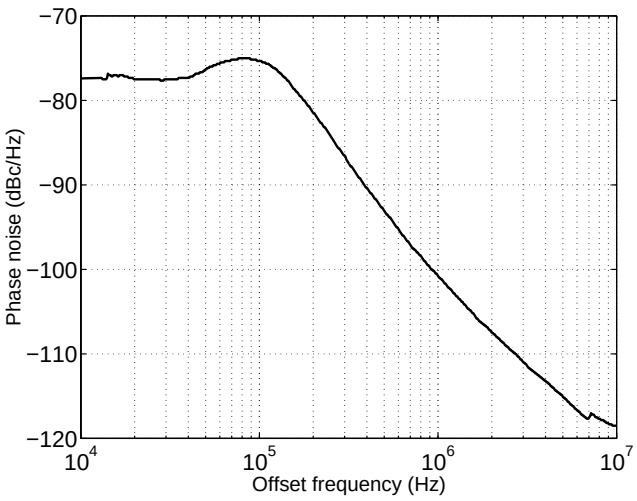

Fig. 10. Phase noise of the synthesizer output signal.

VI. Conclusion

In this work we demonstrate the design of a fully integrated, 5GHz CMOS frequency synthesizer designed for a U–NII band WLAN system. The voltage–controlled differential injection–locked frequency divider used as the first divider in the PLL feedback loop, reduces the power consumption considerably and eliminates the need for an off–chip frequency divider.

Table I summarizes the performance of the synthesizer. The spurious sidebands at offset frequencies of twice the reference signal are more than 54dB below the carrier. The measured phase noise of the synthesized LO signal is −101dBc/Hz at 1MHz offset frequency. Of the 32mW total power consumption, less than 4.2mW is consumed by the VCO and VCDILFD combined. This low power consumption is achieved by the optimized design of the spiral inductors in the VCO and VCDILFD. The prescaler operates at 2.5GHz and consumes more than 25mW, of which about 40% is consumed in the first 2/3 dual modulus divider. Therefore, the VCDILFD, which takes advantage of narrowband resonators, consumes less than $\frac{1}{8}$ the power of the first 2/3 dual modulus divider, while operating at twice the frequency. The PLL bandwidth is 300kHz and the worst case settling time to a 10ppm accuracy is estimated to be less than 7.3μs.

TABLE I
Measured synthesizer performance

Synthesizer performance	
Synthesized frequencies	4.840–4.994GHz
Reference frequency	11MHz
LO spacing	22MHz
Number of channels	8
Spur @ f_{ref}	≤ -45dBc
Spur @ $2 \times f_{ref}$	≤ -54dBc
Phase noise	−101dBc/Hz @ 1MHz
Power dissipation	
VCO	3.0mW
VCDILFD	1.2mW
Prescaler	25.4mW
Total	32mW
Supply voltage	1.5V for VCO & VCDILFD
	2.0V for the rest
Implementation	
Die area	1.6mm^2
Technology	0.24μm CMOS

VII. Acknowledgments

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