A 12.4mW CMOS Front-End for a 5GHz Wireless-LAN Receiver

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Abstract

This paper presents a 12.4mW front-end for a 5GHz wireless-LAN receiver fabricated in a 0.24-μm CMOS technology. It consists of an LNA, mixers and an automatically tuned third-order filter controlled by a low-power PLL. The filter attenuates the image-signal by an additional 12dB beyond what can be achieved by an image-reject architecture. The filter also reduces the noise contribution of the cascode devices in the LNA core. The LNA/filter combination has a noise figure of 4.8dB and the overall noise figure of the signal path is 5.2dB. The overall IIP3 is -2dBm.

Introduction

The growing popularity of notebook computers demands high data-rate wireless local area network (LAN) systems. Many existing wireless LAN systems operate in the 2.4GHz ISM band. These products currently achieve maximum data rates of 1-2Mbits/s. The need for higher data-rate wireless LAN products prompted the Federal Communications Commission (FCC) to release 300MHz of spectrum for the unlicensed national information infrastructure (U-NII)[1]. Using this newly released frequency band, wireless LAN systems can provide data rates of several tens of megabits per second. The allocated frequencies overlap the European standard for the high performance radio LAN (HIPERLAN) frequency band.

The superheterodyne architecture is the most widely used architecture for wireless receivers. Monolithic image cancellation has always been a challenge due to the design problems of on-chip filters. The use of image-reject architectures alleviates this problem to some extent. Typically, these architectures can achieve 30-40dB of image cancellation [2], [3].

This paper describes the design and implementation of a 12.4mW CMOS front-end receiver for a 5GHz wireless-LAN system. The receiver uses a tunable third-order filter controlled by an image-reject PLL structure to alter the transfer function of the low noise amplifier (LNA). The LNA/filter combination attenuates the image-signal by an additional 12dB beyond what can be achieved by an image-reject architecture.

Receiver Architecture

Wireless-LAN systems require receiver architectures with wide dynamic range. When a transmitter and receiver are close to each other, the received signal strength can be as high as −20 dBm. A highly linear receiver is needed to accommodate such strong signals. On the other hand, the received signal can be quite weak due to fading. The receiver must be sensitive enough to detect signals as small as −148dBm/Hz.

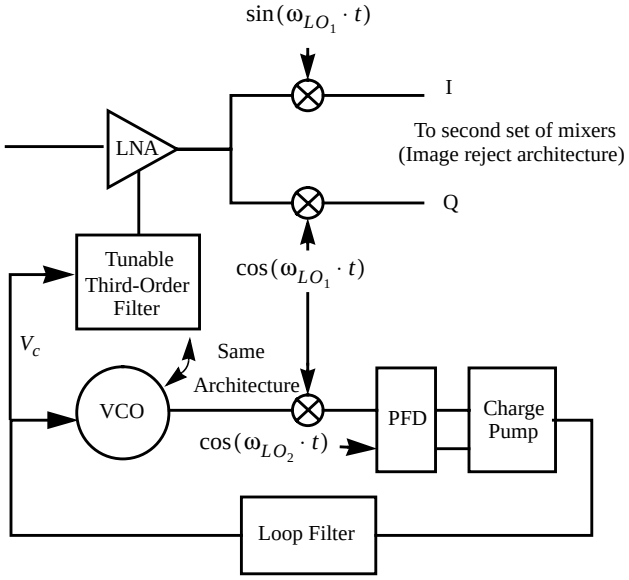

Fig. 1 Block diagram of the receive path.

(i.e., −74dBm for a 24MHz bandwidth signal [4]). To have a pre-detection signal-to-noise ratio (SNR) of at least 12dB, the overall noise figure of the receiver must be better than

$$NF = -148\text{dBm/Hz} - 12\text{dB} - (-174\text{dBm/Hz}) = 14\text{dB},$$

where −174dBm/Hz is the available noise power of the source. This noise figure is readily achievable.

Fig. 1 shows the block diagram of the receive path. The system uses two sets of local oscillators (LOs) to implement an image reject architecture. The RF input lies in the 5.15-5.35GHz frequency band. The frequency of the first LO is $16/17$ of the RF input and the frequency of the second LO is $1/17$ of the RF input [5]. Because of these choices of the LO signals, the image-signal lies within the downlink frequency spectrum of a satellite system and is relatively weak.

The LNA is followed by a first set of mixers to produce the I and Q components of the IF signal. A tunable third-order filter alters the transfer characteristic of the LNA to achieve further filtering of the image signal. A phase locked loop (PLL) automatically tunes the image-reject band of the filter to the correct image frequency.

It is important to mention that the circuit implementations of the VCO and the filter are exactly the same. Because of this similarity, the locations of the pole and zero of the filter are closely related to the oscillation frequency of the VCO. The VCO and the filter share the same control voltage, and since

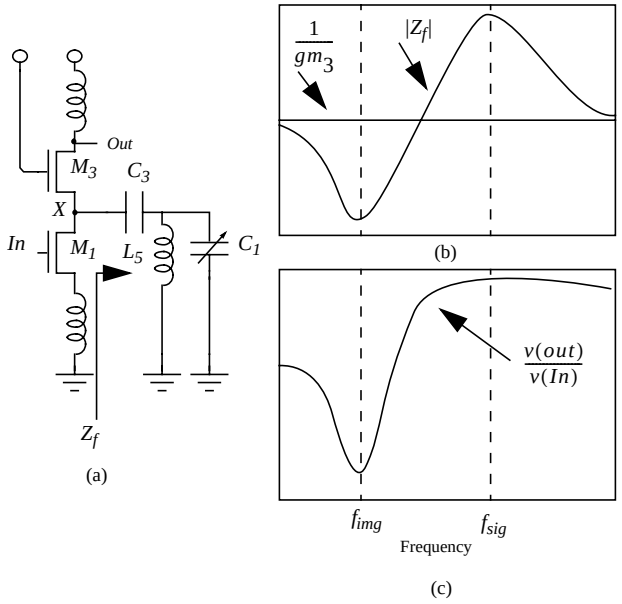

Fig. 2 (a) Circuit diagram of LNA with third order filter. (b) Input impedance of the filter versus frequency; and (c) the transfer function of the LNA/filter combination.

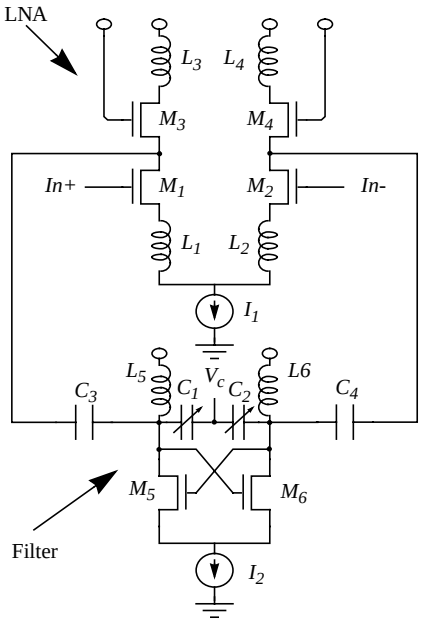

Fig. 3 Simplified circuit diagram of the LNA and filter.

they are topologically identical, locking the VCO frequency to the frequency of the image signal guarantees the rejection of the image.

A passive mixer downconverts the VCO output by mixing it with the first LO. A phase/frequency detector (PFD) compares the downconverted signal against the second LO. A charge-pump circuit and loop-filter complete the PLL. The lock condition is reached when the downconverted VCO output has the same frequency as that of the second LO. That is, the PLL locks when the VCO output is tuned to the image frequency.

This particular PLL structure eliminates the need for frequency dividers in the loop by using the pre-generated LO signals. Since there are no power hungry dividers in this structure, the image-reject PLL consumes little power (Table 1).

Fig. 2 (a) depicts how filtering can be done at high frequencies. The filter comprises an inductor, a capacitor and a varactor. The input impedance of the filter, Z_f, can be written as

$$Z_f(s) = \frac{L_5 \cdot (C_3 + C_1) \cdot s^2 + 1}{C_1 \cdot C_3 \cdot L_5 \cdot s^3 + C_3 \cdot s}. \quad (1)$$

The filter has imaginary zeros at

$$\omega_z = \pm \frac{1}{\sqrt{L_5 \cdot (C_3 + C_1)}} \quad (2)$$

and imaginary poles at

$$\omega_p = \pm \frac{1}{\sqrt{L_5 \cdot C_1}}. \quad (3)$$

Fig. 2 (b) shows the input impedance of the filter, $|Z_f|$, as well as the resistance looking into the source of the cascode device, gm_3^{-1}, as a function of frequency. For frequencies close to the location of the zero, the filter has an impedance lower than gm_3^{-1} and steals the ac current away from *M3*, thus reducing the LNA gain. At frequencies close to the pole, $|Z_f|$ is larger than gm_3^{-1} and the LNA gain is high. The resulting transfer function of the LNA/filter is shown in Fig. 2 (c). The transfer function has a narrow valley, so for correct image-cancellation the zero must occur at the correct frequency. On the other hand, the peak is wideband and the exact location of the pole is less important.

In a standard LNA structure where the filter is not present, the parasitic capacitance of node *X* degrades the noise performance by increasing the noise contribution of the cascode device, M_3. An inductor in parallel with this parasitic capacitance is a remedy to this problem. Keeping this in mind, the third order filter is designed not only to reject the image signal but also to diminish the effect of the parasitic capacitance at node *X*. Thus, by providing a pole (parallel resonance) as well as a zero (series resonance) the filter achieves image rejection and good noise performance at the same time. Although equations (1)-(3) need to be modified slightly to include the effect of this parasitic capacitance, the above argument is still valid.

Circuit Implementation

A. LNA and Filter

Fig. 3 is a simplified schematic of the LNA and filter. A differential architecture is selected for better rejection of on-chip interference. To achieve high linearity, the LNA consists of only one stage, formed by transistors M_1 through M_4. Inductive degeneration is employed in the sources of M_1 and M_2 to produce a real term in the LNA's input impedance[6].

The capacitors C_1 through C_4, and the inductors L_5 and L_6 form a differential version of the filter discussed previously. The cross-connected differential pair, M_5 and M_6, generates a

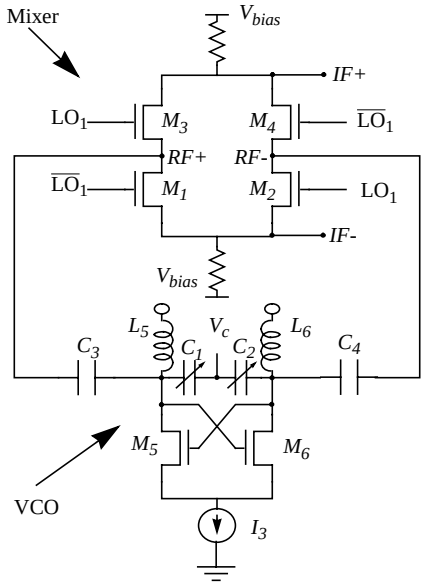

Fig. 4 A simplified circuit diagram of the VCO and loop mixer.

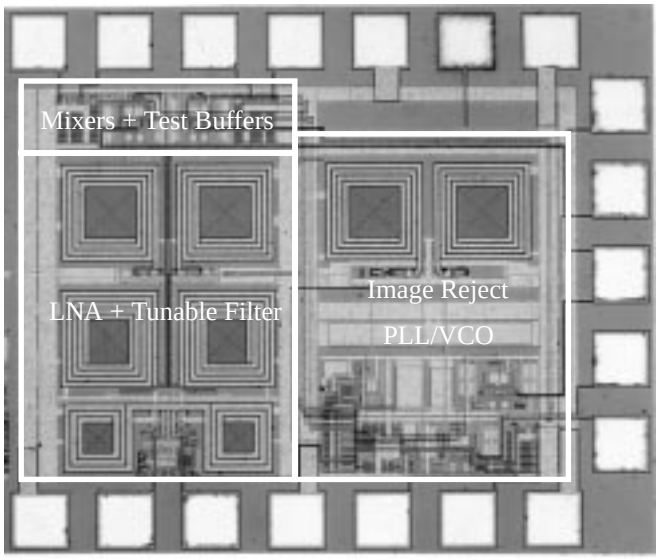

Fig. 5 Die micrograph of the receive path.

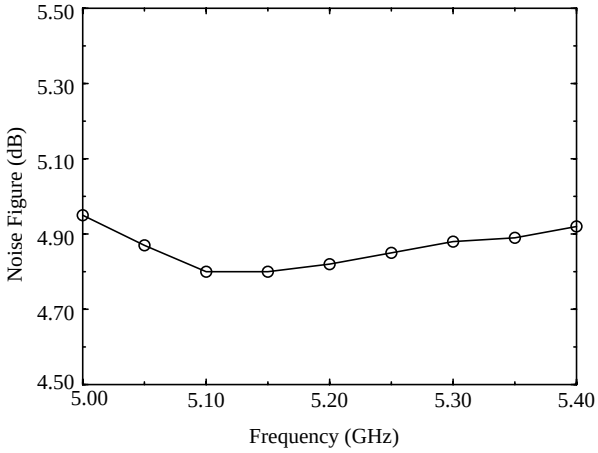

Fig. 6 Measured LNA noise figure.

negative impedance to cancel the losses in the filter, which are mainly due to the finite *Q* of the inductor. The depth of the notch in Fig. 2 (c) depends on this negative impedance. By choosing a correct value for the tail current (I_2 in Fig. 3), one can easily adjust the amount of image-rejection without jeopardizing the stability of the filter.

The voltage V_c controls the location of the pole-zero pair by changing the capacitance of accumulation mode varactors C_1 and C_2.

The filter also reduces the noise figure of the cascode devices, at the cost of adding some extra noise of its own. Since the bias currents of the M_1-M_2 pair are much lower than those of the cascode devices, the net effect is an improvement in noise figure.

B. Image-Reject PLL

Fig. 4 is a simplified circuit diagram of the VCO and mixer used in the PLL loop. The same filter structure is now used as a VCO. The only difference is the increased tail current necessary to sustain oscillation. The mixer consists of four transistors, M_1 through M_4. The similarity between the topologies depicted in Fig. 3 and Fig. 4 suggests that the oscillation frequency of the VCO is a good measure of the zero location of the filter. A PFD, charge-pump and loop filter follow the mixer to complete the loop. Since these three blocks work at the frequency of the second LO, they consume little power (1.1mW).

C. Mixers

The output of the LNA is downconverted by the first set of mixers to produce the I and Q components of the IF signal. These signal-path mixers are identical to the mixer used in the PLL (Fig. 4). Each mixer consists of four transistors, grouped together into two pairs of two transistors each. During each half cycle of the LO signal, the RF port is connected to the IF port with a different polarity, as described in detail in [6].

Measurements

The front-end receiver has been implemented in a 0.24-µm CMOS technology, and the die micrograph is shown in Fig. 5. The chip consumes 12.4mW of power from a 2V power supply and occupies 1mm^2 of die area. It uses 8 spiral inductors with patterned ground shields for improved quality factor and reduced crosstalk between spirals [7].

The LNA/filter combination has also been laid out as a separate test structure so that it could be characterized independently. As shown in Fig. 6, the differential LNA has a noise figure of 4.8dB and consumes only 7.2mW of power. The filter consumes 1mW of power and the amount of image-rejection boost is 12dB. It is possible to increase the amount of rejection even further by increasing the power consumption of the filter. The image-reject PLL consumes 3.2mW of power, of which 2.1mW is burned by the VCO.

For measurement purposes, test-buffers placed after the two mixers allow characterization of the performance of the signal path. The overall measured noise figure is 5.2dB.

Fig. 7 shows the results of a two-tone third-order intercept

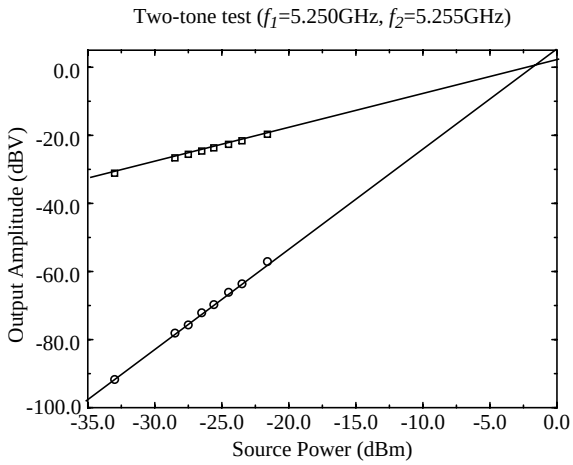

Fig. 7 Two-tone IP3 measurement for the RF front-end.

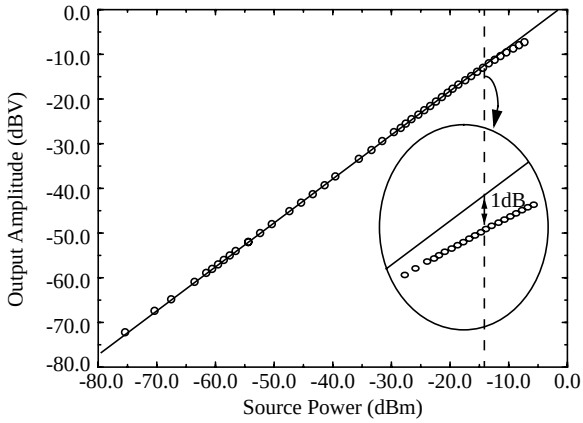

Fig. 8 1-dB compression-point measurement.

point (IP3) measurement performed on the signal path. For the IP3 test, two in-band signals are applied to the system at 5.250 and 5.255GHz. The measured input-referred IP3 is −2dBm. The input-referred 1dB compression point of the receiver is −14 dBm (Fig. 8).

In-band and out-of-band blockers usually limit the performance of a receiver. For a wireless LAN receiver, the in-band blockers (adjacent channels) are the most important blockers that limit the performance of the system. To measure the effect of in-band blockers, a 1-dB in-band blocking test is performed. Assuming a channel width of approximately 24MHz, a single in-band blocker is applied at 24MHz offset from the carrier. The power of the blocker is increased until a 1-dB reduction in the output signal is observed. According to the measurements, the 1-dB in-band blocking de-sensitization occurs when the power of the blocker is −11dBm. This number is higher than the maximum power of the adjacent channel (−20 dBm), so the in-band blocking performance is more than adequate. The performance of the system is summarized in Table 1.

Conclusions

A low-power CMOS front-end receiver for a 5GHz wireless-LAN system has been presented. A third-order filter alters the transfer function of the LNA to reject the image-signal and to decrease the noise contribution of the cascode devices in the LNA core. A PLL structure automatically tunes the filter to the correct frequency. The system is highly linear and tolerates large blockers.

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Table 1 Measured signal-path performance

LNA Performance	
Noise Figure	4.8dB
Voltage Gain	18dB
S11	-12dB
Image Rejection	12dB
Receive path (LNA+mixers) performance	
Total Noise Figure	5.2dB
Total Voltage Gain	12dB
Input-referred IP3	-2dBm
1-dB compression point	-14dBm
1-dB In-band Blocking De-sensitization	-11dBm (adjacent channel)
Power Dissipation	
LNA	7.2mW
Image-Reject Filter	1mW
Image-Reject PLL/VCO	3.2mW
Bias Circuitry	1mW
Total Power @ 2V	12.4mW
Implementation	
Die Area	$1mm^2$
Technology	0.24-µm CMOS

References

[1] K. Pahlavan, A. Zahedi and P. Krishnamurthy, "Wideband local access: wireless LAN and wireless ATM," *IEEE Communication Magazine*, pp. 34-40, Nov. 1997.

[2] B. Razavi, "Design Consideration for Direct-Conversion Receivers," *IEEE Transactions on Circuits and Systems*, vol. 44, pp. 428-435, June 1997.

[3] M. McDonald, "A 2.5GHz BiCMOS image-reject front end," *ISSCC Dig. Tech. Papers*, pp. 144-145, Feb. 1993.

[4] S. Jones, "RF system requirements for HIPERLAN," *Microwave and RF Conference Proceedings*, pp. 1-6, 1995.

[5] H. Rategh, H. Samavati, T. Lee, "A 5GHz, 32mW CMOS frequency synthesizer with an injection locked frequency divider," submitted to Symposium on VLSI Circuits, June 1999.

[6] A. Shahani, D. Shaeffer, T. Lee, "A 12-mW wide dynamic range front-end for a portable GPS receiver," *IEEE J. Solid-State Circuits*, vol. 32, pp. 2061-2070, Dec. 1997.

[7] C. Yue and S. Wong, "On-chip spiral inductors with patterned ground shields for Si-based RF IC's," *Symposium on VLSI Circuits Digest*, pp. 85-86, June 1997.