Narrowband CMOS RF Low-Noise Amplifiers

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Outline

- A brief review of classic two-port noise optimization
  - Conditions for minimum noise figure
  - The fundamental importance of correlations
- MOSFET noise models in the short-channel regime
  - Equivalent two-port noise generators
  - Second-order noise sources
- Power constrained noise optimization
- Experimental results on devices and circuits
- Summary and conclusions
Classic Two-Port Noise Optimization

- Consider noise in an arbitrary (but linear) system:

- Thermal noise of source represented by $i_S$
- Source admittance is $Y_S$
Classic Two-Port Noise Optimization

- The noisy two-port may be modeled as follows:

- In general, the external noise sources will be partially correlated
  - Correlations arise because an internal noise source may contribute to both \( i_n \) and \( e_n \) in general
  - Correlations have strong implications for noise performance
Classic Two-Port Noise Optimization

- Noise factor, $F$, is defined as the ratio of the total output noise power divided by that part of the output noise power due to the input source, when source is at 290K.

- Therefore:

$$F = \frac{\overline{i_s^2} + \overline{i_n + Ye_n}^2}{\overline{i_s^2}}$$

- Let noise current $i_n$ be expressed as sum of two terms.

  - First term, $i_u$, is fully uncorrelated with noise voltage $e_n$.
  - Other term, $i_c$, is fully correlated with $e_n$. 
Classic Two-Port Noise Optimization

- Since $i_c$ is correlated with $e_n$, we may write one as proportional to the other:

  $$i_c = Y_{c n}$$

- Note that $Y_c$ has the dimensions of an admittance
  - Correlation admittance is a mathematical construct, and is not what one measures with an impedance meter

- Re-write $F$ as

  $$F = 1 + \left| \frac{i_n + Y_c e_n}{2} \right|^2 = 1 + \frac{i_u^2 + Y_c + Y_s^2 e_n^2}{i_s^2}$$
Classic Two-Port Noise Optimization

Next, define effective noise resistances (conductances):

\[ R_n = \frac{2}{4kT\Delta f}, \quad G_u = \frac{2}{4kT\Delta f}, \quad G_S = \frac{2}{4kT\Delta f} \]

Also:

- \( Y_c = G_c + jB_c \)
- \( Y_s = G_s + jB_s \)

Finally obtain:

\[ F = 1 + \frac{G_u}{G_s} + \frac{R_n}{G_s} \left[ \left( \frac{G_s + G_c}{G_s} \right)^2 + \left( \frac{B_s + B_c}{G_s} \right)^2 \right] \]
Classic Two-Port Noise Optimization

- Minimum $F$ occurs when $B_s = -B_c = B_{\text{opt}}$ and
  
  $$G_s = \sqrt{\frac{G_u}{R_n} + G_c^2} = G_{\text{opt}}$$

- Minimum $F$ is
  
  $$F_{\text{min}} = 1 + 2R_n \left[ \frac{G_u}{R_n} + G_c^2 + G_c^2 \right]$$

- In general,
  
  $$F = F_{\text{min}} + \frac{R_n}{G_s} \left[ (G_s - G_{\text{opt}})^2 + (B_s - B_{\text{opt}})^2 \right]$$

- Thus, contours of constant noise figure are circles centered about $(G_{\text{opt}}, B_{\text{opt}})$ in the admittance or Smith plane
Classic Two-Port Noise Optimization

- Source admittance for optimum noise match does not generally have any relation to the conditions for optimum power gain
  - Possible to have great noise figure and little or no gain
  - Possible to have great noise figure and a poor impedance match
- Classical noise optimization also does not consider power consumption directly
  - Modified approach required to balance all parameters of practical interest
Simple CMOS Noise Model

• Channel thermal noise is dominant.
  \[ \bar{i}_d^2 = 4kTB \gamma g_{d0} \]

• Gate resistance minimized by good layout.
Channel Thermal Noise

- Current HSPICE Implementation:

\[ i_d^2 = \frac{8}{3} kTB g_m \]  
\[ \text{for } (\text{NLEV} < 3) \]

\[ i_d^2 = \frac{8}{3} kTB \cdot K'(V_{gs} - V_T) \frac{1 + a + a^2}{1 + a} GDSNOI \]  
\[ \text{for } (\text{NLEV} = 3) \]

- BSIM-3 Implementation:

\[ i_d^2 = \frac{4kT \mu_{\text{eff}}}{L_{\text{eff}}^2} \left| Q_{\text{inv}} \right| \]
How To Get 50Ω

Dual Feedback

Resistive Termination

1/g_m Termination

Inductive Degeneration

\[ Z_{in} = \sqrt{R_{f1}R_{f2}} \]

\[ Z_{in} = R_t \]

\[ Z_{in} = \frac{1}{g_m} \]

\[ \text{Re} [Z_{in}] = \frac{g_m}{C_{gs}} L_s \]

Need high gain.

Poor NF.

NF > 3dB

( \gamma > 1 )

Narrowband.

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LNA Input Stage

\[ Z_{in} = s(L_s + L_g) + \frac{1}{sC_{gs}} + \left( \frac{g_m}{C_{gs}} \right) L_s \approx \omega_T L_s \]

\[ G_{m,eff} = g_m Q_{in} = \frac{g_{m1}}{\omega C_{gs} (R_s + \omega_T L_s)} \]

\[ = \frac{\omega_T}{\omega R_s \left( 1 + \frac{\omega_T L_s}{R_s} \right)} = \frac{\omega_T}{2 \omega R_s} \]

Note: \( G_{m,eff} \) is independent of \( g_{m1} \)!
LNA Input Stage: Some Observations

- As noted, overall stage transconductance is independent of device $g_m$ if resonant frequency and current density are held constant.
  - Theoretically, may use arbitrarily narrow devices and still obtain the desired transconductance.

- If drain current noise were the only noise source, narrower devices would lead to monotonically decreasing noise.

- Since gain is fixed, noise figure approaches 0dB as device narrows. Power dissipation would also approach zero.

- Absurd conclusion of zero dB NF, zero power dissipation and nonzero gain should make one suspect that something is missing from the foregoing.
Induced Gate Effects

- Gate Noise Current
- Real Component of $Z_g$
Equivalent Gate Circuit

\[ V_{gs} \quad \overline{i_g^2} \quad g_g \quad C_{gs} \quad \text{-OR-} \quad V_{gs} \quad \overline{v_g^2} \quad r_g \quad C_{gs} \]

\[ \overline{i_g^2} = 4kTB\delta g_g \quad g_g = \frac{1}{5} \frac{\omega^2 C_{gs}^2}{g_{d0}} \]

“Blue” Noise
- \( \delta \) (~ 4/3) modified by hot electron effects
- \( \overline{i_g^2} \) partially correlated with \( \overline{i_d^2} \) (c = 0.395j)
- \( \overline{i_g^2} \) and \( g_g \) not modeled in HSPICE

“White” Noise

\[ \overline{v_g^2} = 4kTB\delta r_g \quad r_g = \frac{1}{5g_{d0}} \]

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MOSFET Two-Port Noise Parameters

- $B_{opt} = -B_c = -\omega C_{gs} \left(1 + \alpha |c| \sqrt{\frac{\delta}{5\gamma}}\right)$

- $B_{opt}$ is inductive, except for frequency behavior. Difficult to provide this behavior over a large bandwidth.

- $G_{opt} = \sqrt{\frac{G_u}{R_n} + G_c^2} = \alpha \omega C_{gs} \delta \left(1 - |c|^2\right) \frac{1}{5\gamma}$

- $F_{min} = 1 + 2R_n [G_{opt} + G_c] = 1 + \frac{2 \omega}{\sqrt{5\omega_T}} \gamma \delta \left(1 - |c|^2\right)$

- Note that $F_{min} = 0$dB if gate and drain noise were fully correlated. *The mere presence of noise sources does not necessarily imply nonzero NF.*
### MOSFET Two-Port Noise Parameters

- Consider only drain and induced gate current noise. Then, the following two-port parameters apply:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Expression</th>
</tr>
</thead>
<tbody>
<tr>
<td>$G_c$</td>
<td>$\approx 0$</td>
</tr>
<tr>
<td>$B_c$</td>
<td>$\omega C_{gs} \left(1 + \alpha</td>
</tr>
<tr>
<td>$R_n$</td>
<td>$\frac{\gamma g_{d0}}{2 g_m} = \frac{\gamma}{\alpha} \cdot \frac{1}{g_m}$</td>
</tr>
<tr>
<td>$G_u$</td>
<td>$\frac{\delta \omega^2 C_{gs}^2}{5 g_{d0}} \left(1 -</td>
</tr>
</tbody>
</table>
MOSFET Two-Port Noise Parameters

- Let’s now compile a short table of $F_{min}$ values:

<table>
<thead>
<tr>
<th>$g_m/\omega C_{gs}$</th>
<th>$F_{min}$ (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>0.5</td>
</tr>
<tr>
<td>15</td>
<td>0.6</td>
</tr>
<tr>
<td>10</td>
<td>0.9</td>
</tr>
<tr>
<td>5</td>
<td>1.6</td>
</tr>
</tbody>
</table>

- Numbers pessimistically assume that hot electron effects triple the mean-square noise densities.

- Even with such effects, achievable noise figures are very good.

- Question: How can these values be approached in practice?
Second-Order Noise Sources

- Practical NF values are affected by series gate resistance and epi noise.
- $F$ is increased by $R_g/R_s$, so just $10\Omega$ by itself sets a lower NF bound of $0.8\text{dB}$ in a $50\Omega$ system.
- Must use multi-fingered devices ($R_{\text{finger}} = R_{\text{SH}}W_{\text{finger}}/3L$).
- Cannot use planar spiral inductors in gate circuit if best NF is to be achieved ($\text{NF typically} > 2\text{-}3\text{dB}$).
- Thermal noise of substrate (epi) resistance modulates the back gate, giving rise to additional drain current noise:

$$
\frac{\Delta f}{\dot{i}_{\text{nd}}^2} = 4kT \left( \gamma g_{d0} + g_{mb}^2 R_{\text{epi}} \right) = 4kT g_{d0} \left( \gamma + \frac{\frac{2}{g_{mb}} R_{\text{epi}}}{g_{d0}} \right)
$$
Second-Order Noise Sources

- Effect of epi noise is equivalent to an increase in $\gamma$:

$$\gamma_{eff} = \gamma + \frac{g_{mb}^2 R_{epi}}{g_{d0}}$$

- One may compute that, typically, epi noise increases $\gamma$ by ~10%, an amount smaller than the uncertainty in $\gamma$ itself.

- Epi noise also contributes to equivalent input current noise, but this is fully correlated with the drain noise.

- Again, fundamental NF limits are set by the uncorrelated gate and drain noise components.
Narrowband LNA

- Choose inductive source degeneration to produce desired real part:

\[ L_S = \frac{R_S \cdot \left(1 + 2 \left(\frac{C_{gd}}{C_{gs}}\right)\right)}{\omega_T} \]

- Equation assumes a cascode stack with equal-sized devices

- Choose sum of gate and source degenerating inductances either to resonate with \( C_{gs} \) or to provide a susceptance equal to \( B_{opt} \).

- First choice maximizes gain, second choice minimizes NF. Difference is small because \( B_{opt} \approx \omega C_{gs} \).

- Note that classic noise optimization says nothing about power dissipation, nor anything about how to select device width.
Power-Constrained Noise Optimization

- Good approximation: Select device width roughly equal to \((500\mu\text{m}-\text{GHz})/f_0\) (for a 50Ω system).

- Adjust bias to obtain desired power dissipation.
  - Keep \(V_{\text{DS}}-V_{\text{DSAT}}\) as small as practical to minimize hot-electron effects (say, under half a volt or so).

- For equal-sized cascoding and main devices, continue to select source degeneration inductance according to:
  \[
  L_S = \frac{R_S}{\omega_T} \left[1 + 2 \left(\frac{C_{gd}}{C_{gs}}\right)\right]
  \]

- Add gate inductance to bring input to resonance.

- Noise factor bound is \(1 + 2.4(\gamma/\alpha)(\omega/\omega_T)\), so scaling continues to help directly.
Experimental Results: Devices

- For 0.5μm technology (drawn), $\text{NF}_{\text{min}} \approx 1.0\text{dB} @ 2\text{mA}, 1\text{GHz}$.
  - $\text{NF}_{\text{min}}$ decreases to $\approx 0.7\text{dB} @ \text{high } I_D$.
  - $\text{NF}_{\text{min}}$ increases to $\approx 1.3\text{dB} @ 2\text{GHz} @ \text{high } I_D$.
  - $\text{NF}_{\text{min}}$ still below $2\text{dB} @ 400\mu\text{A}, 1\text{GHz}$.

- These values apply to a single device without regard for input impedance.
  - Practical $\text{NF}_{\text{min}}$ values are perhaps 0.5dB to 1dB higher.

- Contrary to expectations, no increase in $\text{NF}_{\text{min}}$ is observed in these devices as $V_{DS}$ increases in saturation.
  - Drain engineering possibly responsible (G. Klimovitch et al., 1997).
Experimental Results: Circuits

- Single-ended versions consume half the power for a given NF than differential versions, but:
  - No rejection of common-mode noise.
  - Very sensitive to parasitics, particularly inductances in the source lead of the main transistor.

- Differential versions are relatively insensitive to hard-to-model and hard-to-control parasitics.
  - Attractive for high-volume production.
  - Common-mode rejection highly desirable for mixed-signal environments.
Experimental Results: Circuits

- Series gate inductance provided by bondwires to avoid inevitable NF degradation associated with spiral inductors.
  - Difficult to obtain accurate value without trimming, but repeatability with automated die attach and bonding equipment is very good.
  - Input Q is generally 3-5, so LNA is somewhat forgiving of moderate element value variation.
- Measured and simulated NF agree to within 0.2dB.
- $S_{11} < -15$ dB.
- Receiver IIP3 $>-16$ dBm (measurement confounded by linearity limitation of subsequent receiver stages).
  - IIP3 $>-6$ dBm for LNA itself (simulated).
Summary and Conclusions

- CMOS devices are capable of excellent noise performance in the low-GHz frequency range.
  - Noise performance will continue to improve, despite fears that hot-electron effects will nullify the benefits of scaling.
- Inductively-degenerated LNA architecture simultaneously provides near-optimum gain and NF.
  - Proper device width is important, also.
- At under 10mW dissipation, practical single-ended amplifier noise figures of ~1.5dB at 1GHz are achievable with 0.5μm technology.
- Short-channel effects improve linearity, so dynamic range per power will improve with scaling.
- Epi and gate resistance noise effects are minor, or can be made so.
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