Narrowband CMOS RF Low-Noise Amplifiers

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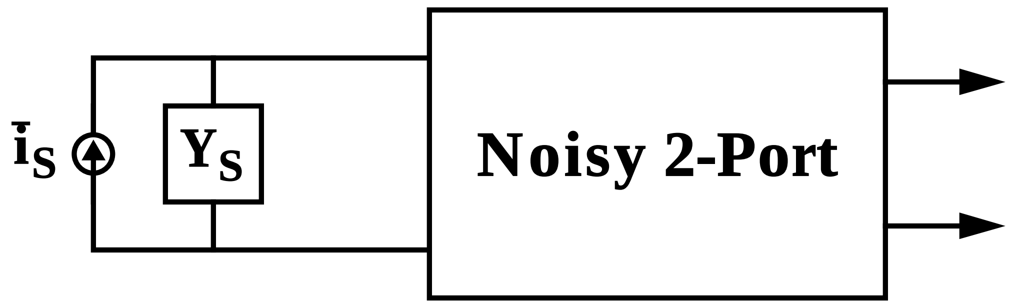
Outline

- A brief review of classic two-port noise optimization
  - Conditions for minimum noise figure
  - The fundamental importance of correlations
- MOSFET noise models in the short-channel regime
  - Equivalent two-port noise generators
  - Second-order noise sources
- Power constrained noise optimization
- Experimental results on devices and circuits
- Summary and conclusions

Classic Two-Port Noise Optimization

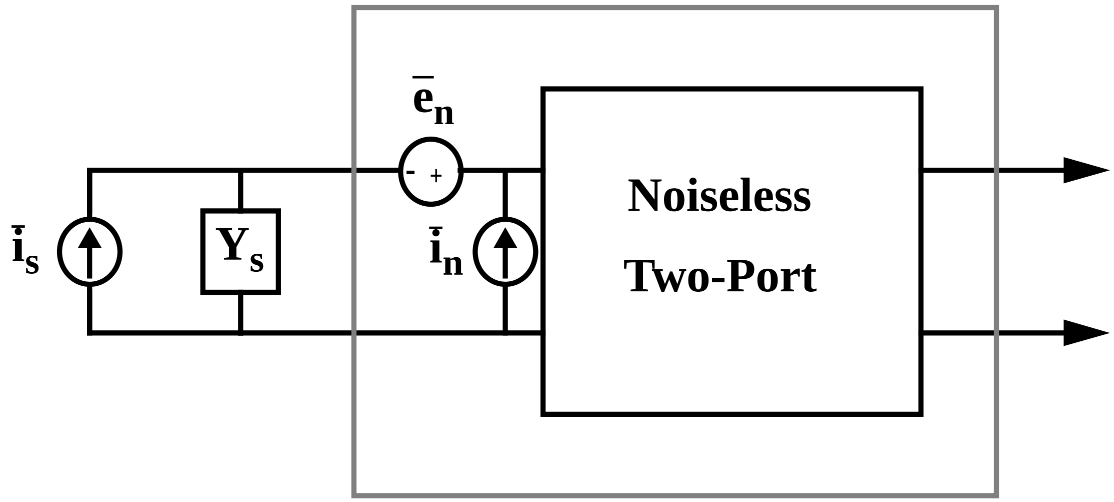
- Consider noise in an arbitrary (but linear) system:



- Thermal noise of source represented by $\bar{i}_S$
- Source admittance is Y_S

Classic Two-Port Noise Optimization

- The noisy two-port may be modeled as follows:



- In general, the external noise sources will be partially *correlated*
  - Correlations arise because an internal noise source may contribute to both i_n and e_n in general
  - Correlations have strong implications for noise performance

Classic Two-Port Noise Optimization

- **Noise factor, F, is defined as the ratio of the total output noise power divided by that part of the output noise power due to the input source, when source is at 290K**
- **Therefore:**

$$F = \frac{\overline{i_s^2} + \overline{\left|i_n + Y_s e_n\right|^2}}{\overline{i_s^2}}$$

- **Let noise current i_n be expressed as sum of two terms**
  - **First term, i_u, is fully uncorrelated with noise voltage e_n. Other term, i_c, is fully correlated with e_n.**

Classic Two-Port Noise Optimization

- Since i_c is correlated with e_n, we may write one as proportional to the other:

$$i_c = Y_c e_n$$

- Note that Y_c has the dimensions of an admittance
  - Correlation admittance is a mathematical construct, and is not what one measures with an impedance meter
- Re-write F as

$$F = 1 + \frac{\overline{\left|i_n + Y_S e_n\right|^2}}{\overline{i_S^2}} = 1 + \frac{\overline{i_u^2} + \overline{\left|Y_c + Y_S\right|^2}\,\overline{e_n^2}}{\overline{i_S^2}}$$

Classic Two-Port Noise Optimization

- **Next, define effective noise resistances (conductances):**

$$R_n \equiv \frac{\overline{e_n^2}}{4kT\Delta f},\ G_u \equiv \frac{\overline{i_u^2}}{4kT\Delta f},\ G_S \equiv \frac{\overline{i_S^2}}{4kT\Delta f}$$

- **Also:**
  - $\mathbf{Y_c = G_c + jB_c}$
  - $\mathbf{Y_s = G_s + jB_s}$
- **Finally obtain:**

$$F = 1 + \frac{G_u}{G_s} + \frac{R_n}{G_s}\left[(G_s + G_c)^2 + (B_s + B_c)^2 \right]$$

Classic Two-Port Noise Optimization

- **Minimum F occurs when $B_s = -B_c = B_{opt}$ and**

$$G_s = \sqrt{\frac{G_u}{R_n} + G_c^2} = G_{opt}$$

- **Minimum F is**

$$F_{min} = 1 + 2R_n\left[\sqrt{\frac{G_u}{R_n} + G_c^2} + G_c^2\right]$$

- **In general,**

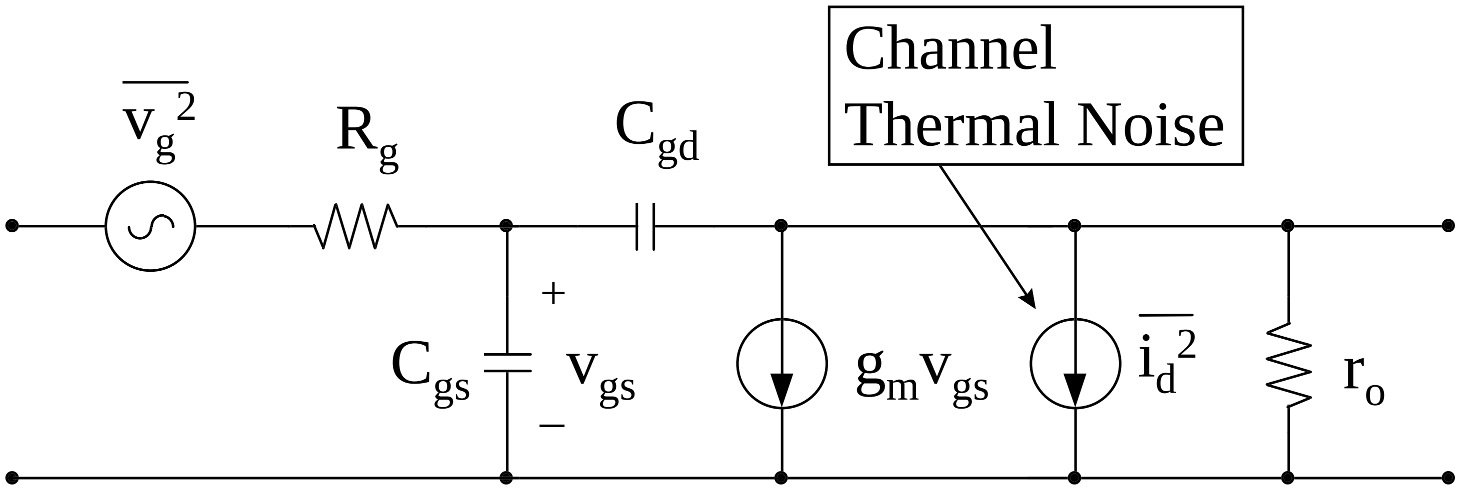
$$F = F_{min} + \frac{R_n}{G_s}\left[\left(G_s - G_{opt}\right)^2 + \left(B_s - B_{opt}\right)^2\right]$$

- **Thus, contours of constant noise figure are circles centered about (G_{opt}, B_{opt}) in the admittance or Smith plane**

Classic Two-Port Noise Optimization

- Source admittance for optimum noise match does not generally have any relation to the conditions for optimum power gain
  - Possible to have great noise figure and little or no gain
  - Possible to have great noise figure and a poor impedance match
- Classical noise optimization also does not consider power consumption directly
  - Modified approach required to balance all parameters of practical interest

Simple CMOS Noise Model



- Channel thermal noise is dominant.

$$\overline{i_d^2} = 4kTB\gamma g_{d0}$$

- Gate resistance minimized by good layout.

Channel Thermal Noise

- Current HSPICE Implementation:

$$\overline{i_d^2} = \frac{8}{3} kTBg_m \qquad \text{(NLEV < 3)}$$

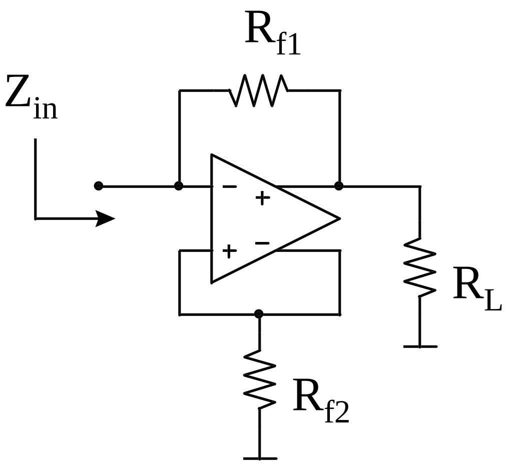
$$\overline{i_d^2} = \frac{8}{3} kTB \cdot K^{'} \left(V_{gs} - V_T\right) \frac{1 + a + a^2}{1 + a} GDSNOI \qquad \text{(NLEV = 3)}$$

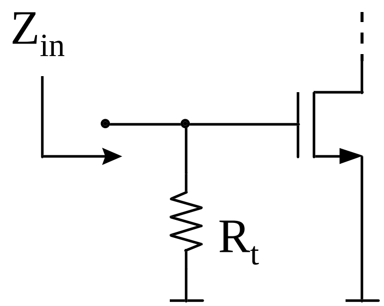
$$a = 1 - \frac{V_{ds}}{V_{dsat}}$$

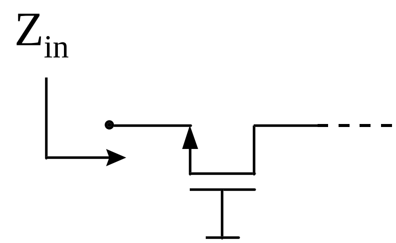
- BSIM-3 Implementation:

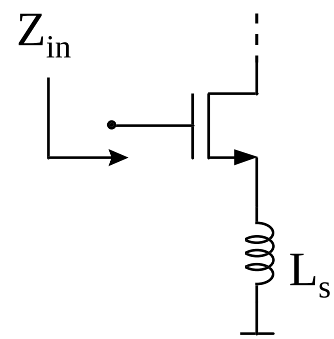
$$\overline{i_d^2} = \frac{4kT\mu_{eff}}{L_{eff}^2} \left|Q_{inv}\right|$$

How To Get 50Ω









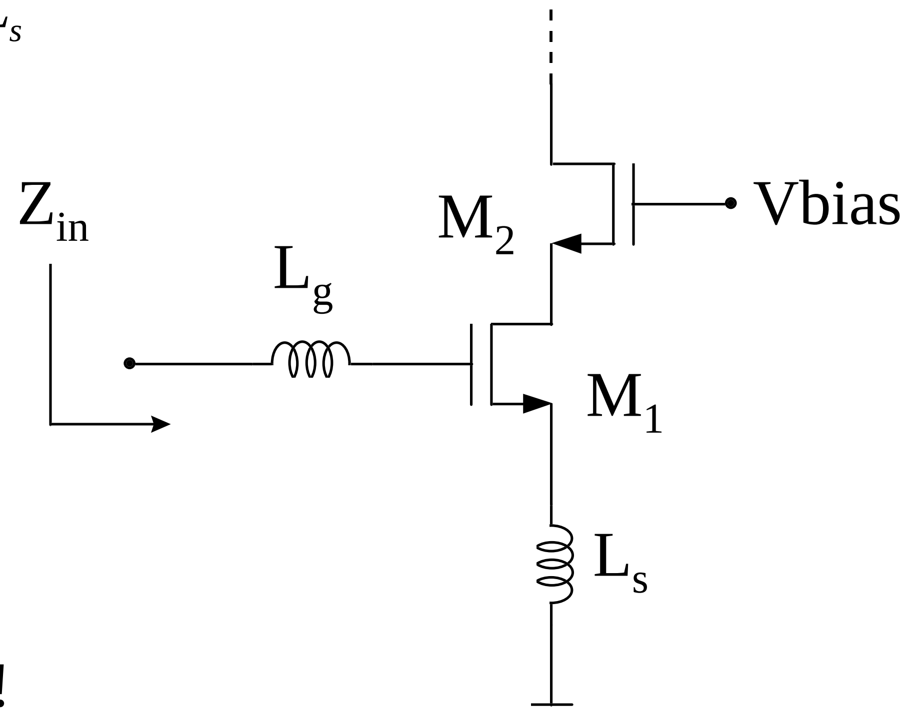
Dual Feedback	Resistive Termination	$1/g_m$ Termination	Inductive Degeneration
$Z_{in} = \sqrt{R_{f1}R_{f2}}$	$Z_{in} = R_t$	$Z_{in} = \dfrac{1}{g_m}$	$\mathrm{Re}\left[Z_{in}\right] = \dfrac{g_m}{C_{gs}} L_s$
Need high gain.	Poor NF.	NF > 3dB	Narrowband.
Stability problems.		($\gamma > 1$)	

LNA Input Stage

$$Z_{in} = s\left(L_s + L_g\right) + \frac{1}{sC_{gs}} + \left(\frac{g_m}{C_{gs}}\right)L_s \approx \omega_T L_s$$

$$G_{m,eff} = g_{m1}Q_{in} = \frac{g_{m1}}{\omega C_{gs}\left(R_s + \omega_T L_s\right)}$$

$$= \frac{\omega_T}{\omega R_s\left(1 + \frac{\omega_T L_s}{R_s}\right)} = \frac{\omega_T}{2\omega R_s}$$

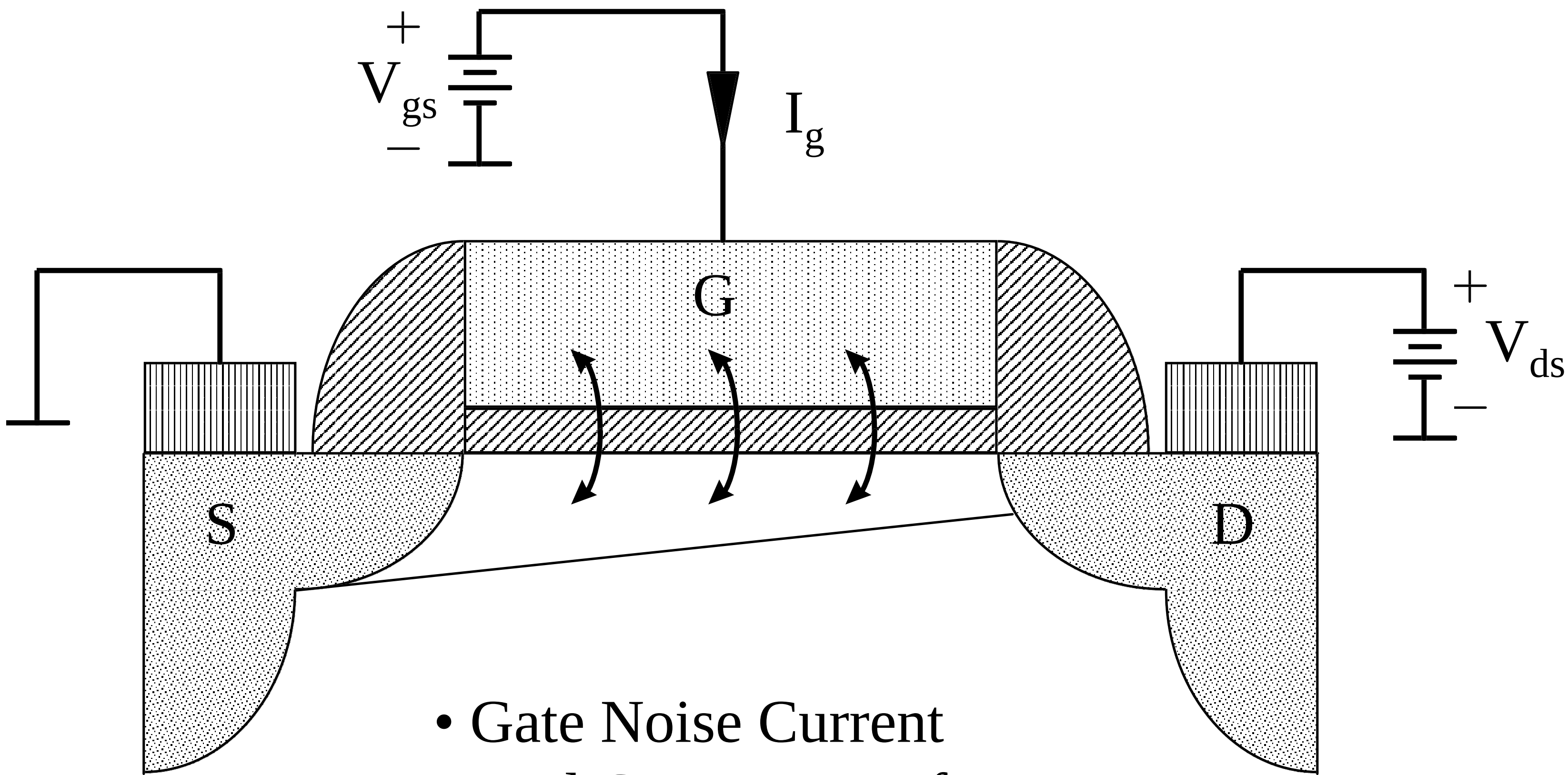


Note: $G_{m,eff}$ is <u>independent</u> of g_{m1}!

LNA Input Stage: Some Observations

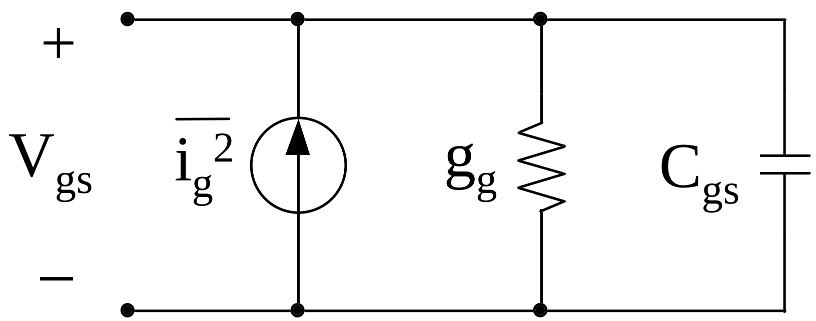
- As noted, overall stage transconductance is independent of device g_m if resonant frequency and current density are held constant.
  - Theoretically, may use arbitrarily narrow devices and still obtain the desired transconductance.
- If drain current noise were the only noise source, narrower devices would lead to monotonically decreasing noise.
- Since gain is fixed, noise figure approaches 0dB as device narrows. Power dissipation would also approach zero.
- Absurd conclusion of zero dB NF, zero power dissipation and nonzero gain should make one suspect that something is missing from the foregoing.

Induced Gate Effects

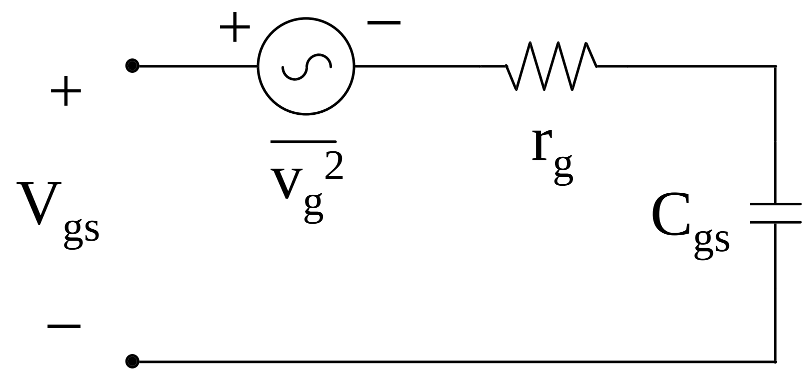


- Gate Noise Current
- Real Component of Z_g

Equivalent Gate Circuit



-OR-



$$\overline{i_g^2} = 4kTB\delta g_g \qquad g_g = \frac{1}{5}\frac{\omega^2 C_{gs}^2}{g_{d0}}$$

"Blue" Noise

$$\overline{v_g^2} = 4kTB\delta r_g \qquad r_g = \frac{1}{5 g_{d0}}$$

"White" Noise

- δ (~ 4/3) modified by hot electron effects
- $\overline{i_g^2}$ partially correlated with $\overline{i_d^2}$ (c = 0.395j)
- $\overline{i_g^2}$ and g_g not modeled in HSPICE

MOSFET Two-Port Noise Parameters

- $$B_{opt} = -B_c = -\omega C_{gs}\left(1 + \alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)$$

- **B_{opt} is inductive, except for frequency behavior. Difficult to provide this behavior over a large bandwidth.**

- $$G_{opt} = \sqrt{\frac{G_u}{R_n} + G_c^2} = \alpha\omega C_{gs}\sqrt{\frac{\delta}{5\gamma}\left(1 - |c|^2\right)}$$

- $$F_{min} = 1 + 2R_n\left[G_{opt} + G_c\right] \approx 1 + \frac{2}{\sqrt{5}}\frac{\omega}{\omega_T}\sqrt{\gamma\delta\left(1 - |c|^2\right)}$$

- **Note that F_{min} = 0dB if gate and drain noise were fully correlated. *The mere presence of noise sources does not necessarily imply nonzero NF.***

MOSFET Two-Port Noise Parameters

- Consider only drain and induced gate current noise. Then, the following two-port parameters apply:

Parameter	Expression
G_c	≈ 0
B_c	$\omega C_{gs}\left(1+\alpha\lvert c\rvert\sqrt{\frac{\delta}{5\gamma}}\right)$
R_n	$\frac{\gamma g_{d0}}{g_m^2} = \frac{\gamma}{\alpha}\cdot\frac{1}{g_m}$
G_u	$\frac{\delta\omega^2 C_{gs}^2\left(1-\lvert c\rvert^2\right)}{5g_{d0}}$

MOSFET Two-Port Noise Parameters

- Let's now compile a short table of F_{min} values:

$g_m/\omega C_{gs}$	F_{min} (dB)
20	0.5
15	0.6
10	0.9
5	1.6

- Numbers pessimistically assume that hot electron effects triple the mean-square noise densities.
- Even with such effects, achievable noise figures are very good.
- Question: How can these values be approached in practice?

Second-Order Noise Sources

- Practical NF values are affected by series gate resistance and epi noise.
- F is increased by R_g/R_s, so just 10Ω by itself sets a lower NF bound of 0.8dB in a 50Ω system.
  - Must use multi-fingered devices ($R_{finger} = R_{SH} W_{finger}/3L$).
  - Cannot use planar spiral inductors in gate circuit if best NF is to be achieved (NF typically > 2-3dB).
- Thermal noise of substrate (epi) resistance modulates the back gate, giving rise to additional drain current noise:

$$\frac{\overline{i_{nd}^2}}{\Delta f} = 4kT\left(\gamma g_{d0} + g_{mb}^2 R_{epi}\right) = 4kTg_{d0}\left(\gamma + \frac{g_{mb}^2 R_{epi}}{g_{d0}}\right)$$

Second-Order Noise Sources

- ❑ **Effect of epi noise is equivalent to an increase in γ:**

$$\gamma_{eff} = \gamma + \frac{g_{mb}^2 R_{epi}}{g_{d0}}$$

- ❑ **One may compute that, typically, epi noise increases γ by ~10%, an amount smaller than the uncertainty in γ itself.**

- ❑ **Epi noise also contributes to equivalent input current noise, but this is fully correlated with the drain noise.**
  - ❑ **Again, fundamental NF limits are set by the *uncorrelated* gate and drain noise components.**

Narrowband LNA

- Choose inductive source degeneration to produce desired real part:

$$L_S \approx \frac{R_S \cdot \left[1 + 2\left(C_{gd}/C_{gs}\right)\right]}{\omega_T}$$

  - Equation assumes a cascode stack with equal-sized devices
- Choose sum of gate and source degenerating inductances either to resonate with C_{gs} or to provide a susceptance equal to B_{opt}.
  - First choice maximizes gain, second choice minimizes NF. Difference is small because $B_{opt} \approx \omega C_{gs}$.
- Note that classic noise optimization says nothing about power dissipation, nor anything about how to select device width.

Power-Constrained Noise Optimization

- **Good approximation: Select device width roughly equal to (500μm-GHz)/f_0** (for a 50Ω system).
- **Adjust bias to obtain desired power dissipation.**
  - **Keep V_{DS}–V_{DSAT} as small as practical to minimize hot-electron effects (say, under half a volt or so).**
- **For equal-sized cascoding and main devices, continue to select source degeneration inductance according to:**

$$L_S \approx \frac{R_S \cdot \left[1 + 2\left(C_{gd}/C_{gs}\right)\right]}{\omega_T}$$

- **Add gate inductance to bring input to resonance.**
- **Noise factor bound is 1 + 2.4(γ/α)(ω/ω_T), so scaling continues to help directly.**

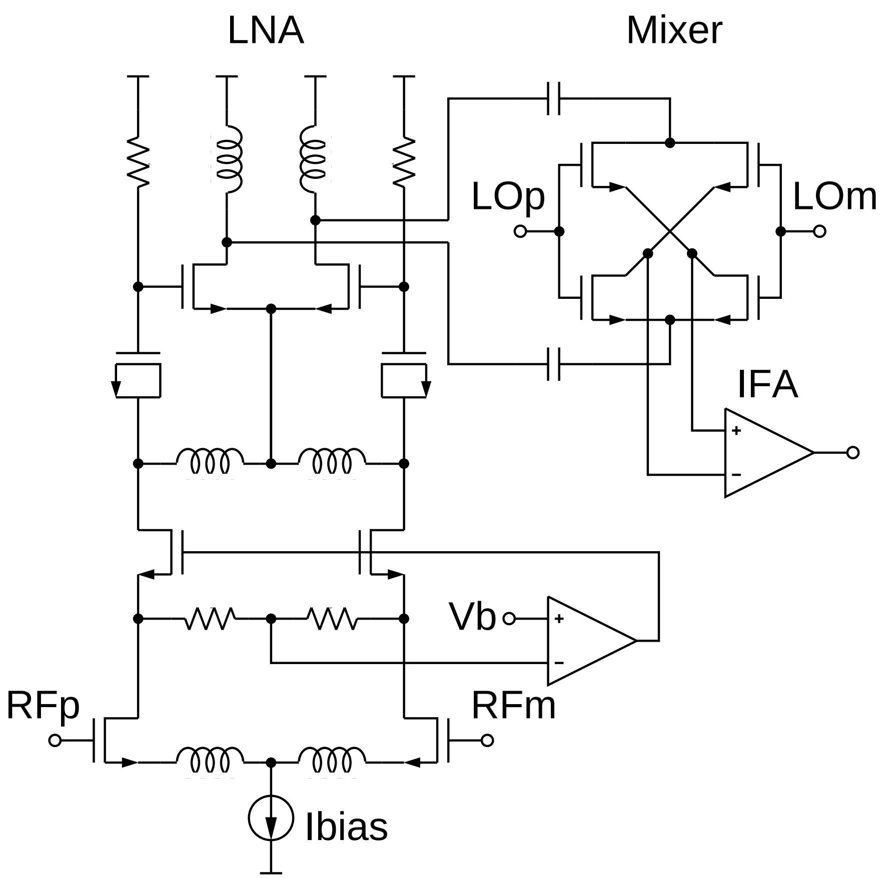
Experimental Results: Devices

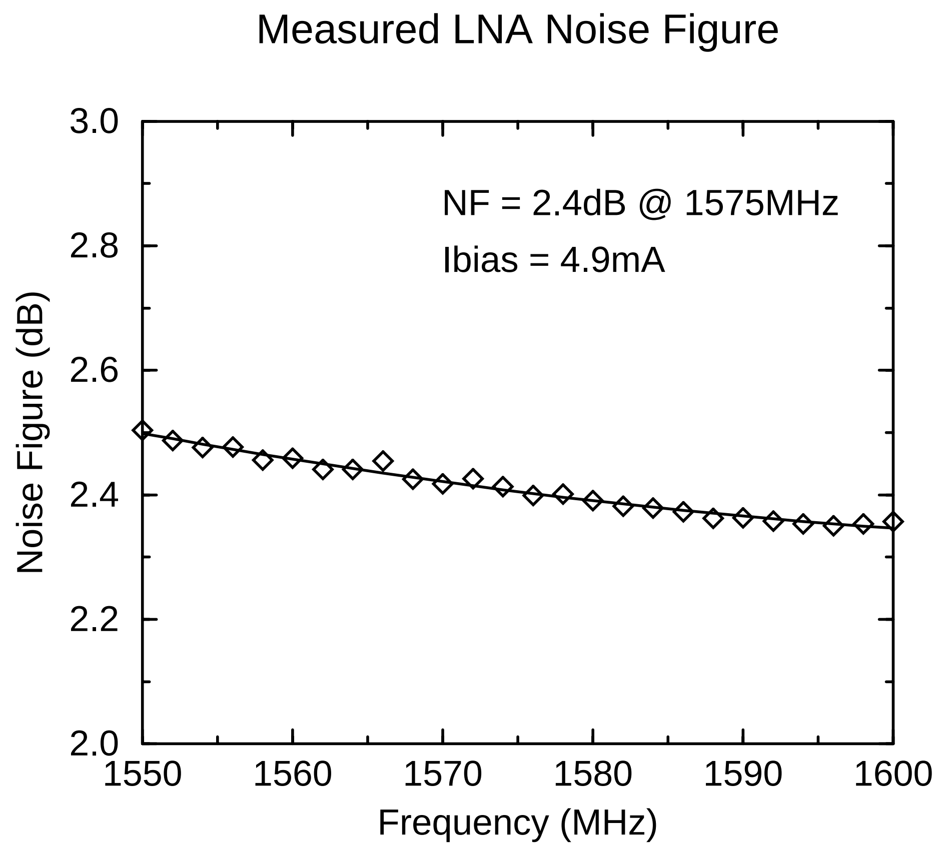
- For 0.5μm technology (drawn), $NF_{min} \approx$ 1.0dB @ 2mA, 1GHz.
  - NF_{min} decreases to ≈ 0.7dB @ high I_D.
  - NF_{min} increases to ≈ 1.3dB @ 2GHz @ high I_D.
  - NF_{min} still below 2dB @ 400μA, 1GHz.
- These values apply to a single device without regard for input impedance.
  - Practical NF_{min} values are perhaps 0.5dB to 1dB higher.
- Contrary to expectations, no increase in NF_{min} is observed in these devices as V_{DS} increases in saturation.
  - Drain engineering possibly responsible (G. Klimovitch et al., 1997).

Experimental Results: Circuits

- Single-ended versions consume half the power for a given NF than differential versions, but:
  - No rejection of common-mode noise.
  - Very sensitive to parasitics, particularly inductances in the source lead of the main transistor.
- Differential versions are relatively insensitive to hard-to-model and hard-to-control parasitics.
  - Attractive for high-volume production.
  - Common-mode rejection highly desirable for mixed-signal environments.

CIRCUITS: LNA / MIXER





Shahani, Shaeffer and Lee, "A 12mW Wide Dynamic Range CMOS GPS Receiver," ISSCC 1997

Experimental Results: Circuits

- Series gate inductance provided by bondwires to avoid inevitable NF degradation associated with spiral inductors.
  - Difficult to obtain accurate value without trimming, but repeatability with automated die attach and bonding equipment is very good.
  - Input Q is generally 3-5, so LNA is somewhat forgiving of moderate element value variation.
- Measured and simulated NF agree to within 0.2dB.
- $S_{11} < -15$dB.
- Receiver IIP3 > –16dBm (measurement confounded by linearity limitation of subsequent receiver stages).
  - IIP3 > –6dBm for LNA itself (simulated).

Summary and Conclusions

- CMOS devices are capable of excellent noise performance in the low-GHz frequency range.
  - Noise performance will continue to improve, despite fears that hot-electron effects will nullify the benefits of scaling.
- Inductively-degenerated LNA architecture simultaneously provides near-optimum gain and NF.
  - Proper device width is important, also.
- At under 10mW dissipation, practical single-ended amplifier noise figures of ~1.5dB at 1GHz are achievable with 0.5μm technology.
- Short-channel effects improve linearity, so dynamic range per power will improve with scaling.
- Epi and gate resistance noise effects are minor, or can be made so.

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