Physical Modelling of Enhanced High-Frequency Drain and Gate Current Noise in Short-Channel MOSFETs

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Abstract

Short-channel CMOS technologies have shown growing prominence for a number of RF applications, such as wide-band wireless communication systems. However, the issue of excessive noise in submicron devices remains a major impediment to CMOS-based low-noise RF design. This paper expands very limited theoretical work existing in the field and presents new results in a form suitable for circuit design applications.

We analyze the high-frequency noise behavior of a short-channel Metal-Oxide-Silicon Field-Effect Transistor (MOSFET) in saturation within the scope of the drift-diffusion model.

As a result of hot-electron effects in a significant portion of a *short* channel, both drain current noise and channel-induced gate current noise turn out to be strong functions of the field distribution in the high-field region and therefore of biasing conditions.

We present both first-principle and semi-phenomenological calculations of the noise factors and compare them with experimental results.

Under the worst-case conditions, such as a very short channel length and a maximum channel field much higher than the saturation field, the gate current noise factor increases much faster with the channel field than the drain current noise factor. As the channel field rises, the imaginary part of the (imaginary) correlation coefficient between the gate and drain currents noise decreases from its value 0.395 for the low-field long-channel case, and may even become negative in the high-field short-channel limit.

Both noise factors, as well as the magnitude and the sign of their correlation coefficient, are important in low-noise high-frequency MOSFET design, e.g. in (Bi)CMOS RF circuits.

1 Introduction

First we consider high-frequency drain current noise of a short-channel Metal-Oxide-Silicon Field-Effect Transistor (MOSFET) in saturation [3]. "High frequencies" here means a wide range beyond the 1/f noise frequency up to the maximum frequency where the quasistatic approximation for the MOSFET still works.

Since the length of this abstract is limited, the calculations are only outlined in a concise and general form, more details and results will be published at a later time.

The model used is based on the drift-diffusion approximation, an approach which allows us to estimate noise factors for channel lengths exceeding $\sim 0.3\mu m$. It is also possible (though computationally extensive) to generalize this model beyond the drift-diffusion approximation to describe noise in the deep submicron regime.

The drain current noise factor is defined by:

$$\overline{i_d^2} = \gamma 4 k_B T \Delta f g_{d0} \ ,$$

where g_{d0} is the drain conductance at zero voltage between the drain and source.

The relationship we confirm analytically is that the shorter the channel the stronger the dependence of the noise factor γ on the channel field [4], [5]. Even using a very crude approximation for the noise temperature, we predict values of γ for moderate saturation from [4] with 11% average error (please see the Appendix).

In addition to drain noise, gate noise also becomes important in the RF regime. The gate current noise factor , is defined by [1]:

$$\overline{i_g^2} = ,\ 4k_BT\frac{\omega^2C_0^2}{g_{d0}}\Delta f \qquad (1)$$

(C_0 is the total gate-channel capacitance) and is expected to be an even stronger function of the maximum longitudinal field E_D in a short-channel device in saturation:

$$\Delta,\ \sim \Delta\gamma\frac{E_D^2}{E_c^2} \qquad (2)$$

where E_c stands for saturation field; $\Delta,\ , \Delta\gamma$ describe how much gate and drain noise factors increase from their long-channel values. (In the long-channel limit, the noise factors in saturation are:
$\gamma = 2/3, \ , \ = 16/135 = 0.12$)

2 Calculation principles and summary

Since the length of this abstract is limited, the calculations are only outlined in a concise, general, and sometimes simplified form.

To find drain current noise, we divide the channel into *independent* voltage noise sources and integrate their contributions to the drain noise current over the channel length. Such a division is valid except in the ultrahigh-field regime or for ultrasubmicron channel lengths (please see also [6]).

The MOSFET is split into low-field and high-field regions, the longitudinal field on their border being $E_c \sim 4 \times 10^4 V/cm$.

We use the following notation in the development that follows:
L_c, L_2 are the lengths of the low- and high-field regions respectively
$L_{tot} = L_c + L_2$ is the effective channel length
I_D is the drain current
$V(y)$ is channel voltage
V_G and V_T are the gate and threshold voltage respectively
$V_D \equiv V(L_{tot})$ is the drain voltage
V_c is the channel voltage on the border between the two regions
$C_{eff} = C_{ox}/(1 + C_{cb}/C_{ox})w$ is the product of the effective (i.e. reduced by the body effect) gate-to-channel capacitance per unit area and the channel width.
$v_d(E)$ is the drift velocity at some longitudinal channel field E.

In the high-field region the longitudinal electric field and channel potential grow exponentially [2]:

$$E(y) = E_c \cosh\frac{y - L_1}{l_E}\ , \quad V(y) = V_c + E_c l_E \sinh\frac{y - L_1}{l_E}\ . \qquad (3)$$

For technical convenience, we often resort to auxiliary open-circuited drain calculations and then modify the results for the case of short-circuited drain.

The voltage noise $\overline{v_n^2(y)dy}$ that occurs in a small $(y, y + dy)$ portion of the channel results in the proportional noise in the open-circuited drain voltage dV_D:

$$\frac{\overline{dV_D^2}}{\overline{v_n^2(y)}dy} = \begin{cases} \frac{E_D^2}{E^2(y)} & 0 < y < L_c \\ \cosh^2 \frac{L_{tot}-y}{l_E} & L_c < y < L_{tot} \end{cases} \tag{4}$$

The linear density of the voltage noise in the channel per unit bandwidth is given by:

$$\frac{\overline{v_n^2(y)}}{\Delta f} = \frac{4k_B T_n(E)}{\mu_0 C_{eff} V_{GT}} \ , \tag{5}$$

where μ_0 is the low-field mobility, $T_n(E)$ is the *noise* temperature of hot carriers which is higher than the lattice temperature.

Given the dependence $T_n(E)$, the total open-circuited drain voltage noise $\overline{v_{D,\,oc}^2}$ is obtained from (4) and (5). Unfortunately, calculation of $T_n(E)$ is still an open issue; the noise temperature depends on processing, especially on impurity scattering. However, physics-based analysis helped us to narrow down the search and exclude invalid phenomenological models used by some other authors [7].

Once $\overline{v_{D,\,oc}^2}$ is calculated, the short-circuited drain current noise is simply $\overline{i_{D,\,cc}^2} \sim \overline{v_{D,\,oc}^2}/r_o^2$, where r_o is the output resistance approximated in a way *consistent* with calculations of $\overline{v_{D,\,oc}^2}$. In particular, since DIBL effect was negleced in the former, it must not be taken into account in the latter (unlike the approach used in [7]). Then, the calculation of r_o by means of field impedance technique yields

$$r_o = \frac{1}{I_D}\left[E_D \int_0^{L_c} \frac{v_d(y)}{E(y)\mu_d(y)}dy + (V_{GT} - V_c)\sqrt{\frac{E_D^2}{E_c^2} - 1}\right] \ , \tag{6}$$

($\mu_d(y)$ is the differential mobility) so that r_o in strong saturation is roughly proportional to E_D. It is the increase in r_o with a maximum channel field E_D that slows down rise in the drain current noise factor γ in comparison with the gate current noise factor , .

To find channel-induced gate current noise, we divide the channel into *independent* voltage noise sources, and integrate their contributions to the gate current over the channel length.

When we neglect gate leakage, gate current $i_G = j\omega q_G$ is the time derivative of gate charge q_G. Therefore, the analysis of the gate current noise can be reduced to that of gate charge noise.

While in the low-field regime the gate charge fluctuations approximately follow the channel charge fluctuations with negative sign, in the high-field short-channel regime there is an extra significant term in the gate charge fluctuations that results from the strong fluctuations in the near-drain longitudinal field E_D. The fluctuations in this field are caused by excessive voltage noise due to hot electron diffusion. This extra term increases the gate current noise over its low-field value and tends to reverse the sign of the correlation coefficient between gate and drain current noise.

The variations δq_G are evaluated neglecting the variations in the charge of the depletion layer between the channel and the bulk.

Then, the variations of the gate charge are related with those of the mobile channel charge δq_{ch} and near-drain longitudinal field δE_D by the Poisson theorem:

$$\delta q_G = -\delta q_{ch} - \epsilon_{si} w t_{ch} \delta E_D \ , \tag{7}$$

where $t_{ch} = l_E^2/t_{ox}$ is the effective thickness of the mobile charge layer near the drain, in terms of the thickness of gate oxide t_{ox} and the length scale of the longitudinal field in the high field region l_E [2]. The derivation of (7) is similar to the derivation of the potential and field distribution in the high-field region in [2].

Due to only the first term in (7), change in , would be roughly proportional to change in γ:

$$\Delta_1, \sim \left[\frac{V_{GT}}{V_{D\ sat}}\right]^2 \Delta\gamma \ , \tag{8}$$

which shows that their absolute changes would be of the same order. However, the second term results in extra increase in , ,

$$\Delta_2 , \sim \Delta_1 , \left[\frac{l_E}{L-l_E}\frac{\epsilon_{si}}{\epsilon_{ox}}\frac{E_D}{E_c}\right]^2 , \tag{9}$$

so that for short channel length $L \leq 5l_E$ the gate noise factor is a superlinear function of the drain noise factor even in moderate saturation $E_D \geq 2E_c$ given by (2). This result holds as long as the hot electron noise temperature grows faster than the longitudinal channel field squared.

3 Conclusions

To summarize, the theoretical description of the high-frequency drain and gate noise in short-channel MOSFETs is given in a form suitable for circuit simulations, and a comparison with limited existing experimental data is made.

Below, we qualitatively reformulate the results from the perspective of low-noise circuit design:

To keep drain and gate noise factors low, the drain voltage V_D should not exceed the saturation voltage V_{Dsat} by more than a few $l_E E_c \sim 1V$.

It is known that the input-referred voltage noise due to cold electron diffusion is approximately proportional to V_{GT}/I_D and is a decreasing function of V_{GT} in the long-channel regime. However the input-referred voltage noise caused by *hot* electron diffusion is roughly proportional to V_{GT}^2/I_D and is an *increasing* function of V_{GT} in the short-channel regime. Therefore, in the short-channel regime V_{GT} should be kept *low*.

Under certain conditions, low-mobility processes can provide MOSFETs with better noise properties, since the noise temperature for a given channel field is a decreasing function of impurity scattering rate.

4 Appendix

Below is a table comparing data on γ taken in moderate saturation from [4] with calculations for a very crude aproximation of the hot electron noise temperature $T_n(E)$ by a single fitting parameter $T_n \approx 10T_0$.

V_{GT}	4.5	4.5	3.5	2.5	1.5	3.5	2.5
V_D	5	4	4	4	4	3	3
γ_{exp}	3.42	2.55	2.68	3.31	4.78	2.38	2.96
γ_{cald}	2.72	2.39	2.97	3.78	4.69	2.44	2.77
%	-20	-6	11	14	-2	3	-6

Only the moderate saturation regime is considered, since this model neglects "warm electron" effects on noise which are important in weak saturation and in the linear regime, and impact ionization effects which may be important in deep saturation. More advanced models will incorporate those effects.

References

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