

An Equalization Scheme for 10Gb/s 4-PAM Signaling over Long Cables

Ramin Farjad-Rad, Kevin Yu, C.-K. Ken Yang, Bill Ellersick, Mark Horowitz and Thomas H. Lee
Center for Integrated System, Stanford University Stanford, CA 94305

Contact: Ramin Farjad-Rad, Center for Integrated Systems, Stanford University, CA 94305
Phone:(415) 725-4538 Fax: (415) 725-3383 E-mail: farjad@smirc.stanford.edu
Area: Interfaces and Specific Applications

Abstract— In this paper, we present simulation results for a 10Gb/s serial link. The serial link is composed of a transmitter, copper coaxial cable, and a receiver. Multilevel signalling (4-PAM) is used along with transmit pulse shaping and receiver equalization.

Significant performance improvement is afforded by the receiver equalizer. A simple 1-tap equalizer is implemented in conjunction with a 3-tap transmit pulse shaping filter. The transmit filter reduces the effects of inter-symbol interference (ISI) caused by the long tails of the channel impulse response. The 1-tap equalizer acts as a zero-forcing equalizer (ZFE), thus the equalizer is a high pass filter. Both filters' tap weights are derived using the least-squares algorithm. Simulations were performed in HPSICE and Matlab using 0.35 μ m CMOS models.

I. INTRODUCTION

The ability to network high speed computers is becoming a dominant bottleneck in system performance. For distances ranging from 1 to 20 meters, traditional methods of parallel busses which require many wires are costly and power inefficient. Optical fibers are also costly and area inefficient for the distances that we are dealing with. As the demand for higher rate communications over longer distances increases, cheap high speed serial links over copper cables becomes more attractive.

The maximum simulated data rate reported over 6 meter cable has been 4Gb/s [1]. This paper describes a 10Gb/s serial link over a 12 meter coaxial cable (RG55B/U) which has a -3 dB bandwidth of approximately 1GHz. Employing techniques such as channel equalization, pulse shaping, and a carefully designed modulation scheme enables us to achieve the 10Gb/s data rate. Channel equalization is performed by a single tap zero-forcing equalizer in the receiver. Transmitter pulse shaping is implemented by a three tap filter. Speed limitations due to process technology were thoroughly examined when choosing the 4-PAM modulation scheme.

Section II provides some background on the communication theory. Section III describes the system architecture. Section IV presents the circuit implementation of system blocks. Simulation results are given in Section V. Finally, Section VI discusses the conclusion and future work.

II. BACKGROUND

Digital communication involves two key ideas. The first idea is using *orthogonal* analog waveforms (basis function) as building blocks, *e.g.*, square waves. The second idea uses the basis functions to abstract modulation to a vector space. The number of orthogonal basis functions is the dimensionality of the vector space. A geometric arrangement of points in the vector space is called a constellation and represents all possible data symbols. Typical constellations are N -PAM and N -QAM. For a fixed data rate, trade-offs between the symbol rate and constellation size can be made. Optimal detection can be performed by sampled matched filters at the receiver. Channel spectral efficiency is determined by the bandwidth of the basis waveforms. If the basis waveforms are not channel eigenfunctions, inter-symbol interference (ISI) occurs. Symbol rates which are well above the channel bandwidth results in significant ISI. Methods such as equalization help reduce ISI. Coding can also be utilized to improve system symbol error rate. For a more detailed treatment of these subjects, see [2], [3].

III. SYSTEM ARCHITECTURE

Implementing matched filters for optimal detection demands high complexity for high symbol rates. Therefore, trapezoidal pulses are used as the basis waveforms due to their simplicity in generation and the ability to perform level detection with moderate complexity. However, since trapezoidal pulses are not the channel eigenfunctions, ISI occurs.

This design uses a 4 level pulse amplitude modulation (4-PAM) due to circuit limitations such as limited transmitter output swing and minimum signal resolution at high speeds. Reflection ISI of large signals due to imperfect line terminations can overwhelm future low-level signals. Since this design does not attempt to equalize reflection ISI, 4-level PAM is chosen to avoid the signal resolution problem.

The measured 1GHz channel bandwidth is roughly a factor of four less than the bandwidth required to obtain a reasonable eye opening for the 5Gsym/s 4-PAM system using trapezoidal pulses. Larger eye openings result in better noise immunity of the system. Thus, equalization must be used.

This design differs from existing implementations of over

1Gb/s links by the use of a receiver equalizer in combination with a transmitter filter. Existing implementations only use a signal shaping filter at the transmitter [1], [4]. This filter attempts to pre-emphasize the output waveform to invert the effects of the channel. Thus, the received signal should more closely resemble the original basis waveform. Due to limited transmitter output swing, transmitter pulse shaping results in the reduction of usable signal voltage at the receiver. Channel inversion is accomplished by a filter in both the transmitter and receiver. By using two filters, constraints on the individual filters are relaxed and signal amplitude is increased.

To characterize our channel, we have measured the impulse response of the coax line and used the response to design the filters. Pulses sent through long co-axial lines experience a slow transition that corrupts the next symbol. Energy in the tails can also affect the symbols well into the future (Figure 1).

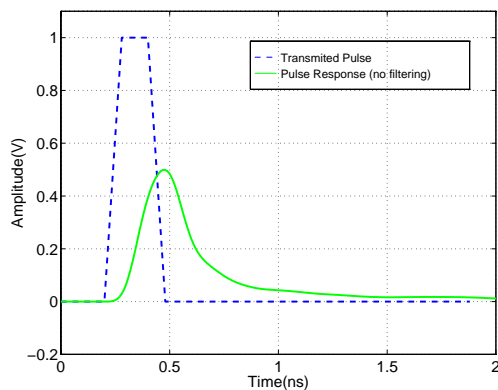


Fig. 1. Pulse response of a 12 meter R55B/U coaxial cable

Simulations show that a 3-tap filter with symbol period tap spacings can reduce the amplitude of the tail to $< 10\%$ of the 4-PAM amplitude spacing (Figure 2). The amplitude spacing, at the receive side, is approximately 0.35 volts due to differential signaling. The Least Square algorithm [5] was used to obtain the filter tap weights which minimize the energy of the difference between the ideal filter response and the real filter response as shown in Figure 2. The 3-tap filter can easily be implemented in the transmitter by generating the “filtered” pulse instead of actually post-filtering an ideal pulse.

Due to the high frequency content of a transition edge, a high bandwidth, short length FIR filter with sub-symbol tap spacing is required. This filter implements a 1-tap zero-forcing equalizer which attempts to invert the channel response regardless of noise characteristics. This filter can easily be implemented in the receiver due to the 3-times oversampling data recovery architecture used [6].

An extra symbol is appended to each block of 4 data symbols. This extra symbol is chosen to guarantee clock recovery by introducing at least one transition in the 5 symbol block. This method is similar to the 8b10b codes used in binary transmission.

Since 4-PAM hard decision decoding is used in the re-

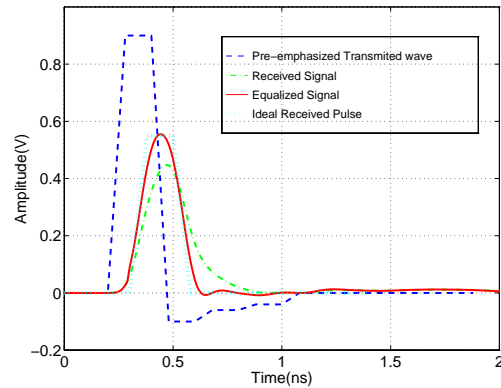


Fig. 2. Pulse shape at different points of the channel

ceiver, a fixed one-to-one mapping of every 2 input bits to a constellation point must be chosen. Six distinct mappings exist for 4-PAM. However, only a Gray code mapping (Figure 3b) guarantees that every nearest neighbor symbol error results in only one bit error. Thus, the expected bit error rate is reduced from $\frac{5}{4}$ to 1 versus the linear mapping (Figure 3a).

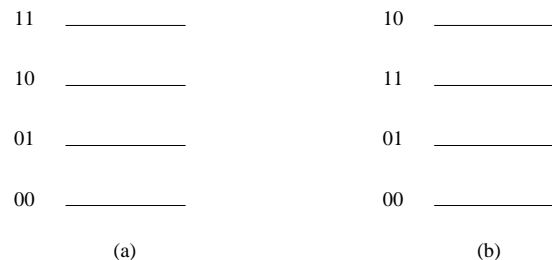


Fig. 3. a) Linear mapping of levels b) Gray code mapping of levels

IV. CIRCUITS IMPLEMENTATION

A. Transmitter

Due to intrinsic process limitations, generating a 5Gsymbol/s stream by a 2.5GHz on-chip oscillator is impractical. Therefore, the serial symbol stream is generated by a 4:1 multiplexer using 4 different clock phases from a 4-stage ring oscillator. Thus, the on-chip frequency is $\frac{1}{4}$ -th the symbol rate ($\frac{1}{8}$ -th the bit rate). The general transmitter architecture is illustrated in Figure 4.

The transmitter consists of 4 differential drivers which are multiplexed onto a 50Ω line. Each driver is composed of four 2-bit DAC differential driving legs as shown in Fig. 5. The main leg drives the coax line with a current proportional to the symbol value. The 3 other legs implement the 3-tap FIR filter. These 3 legs cancel the tail of the main leg’s symbol for the following 3 symbol periods. The current in the pulse-shaping legs (tap weights) is controlled by three 8-bit thermometer-code DACs at the bottom of each leg. Due to the multiplexing of the driver stages, the 8-bit DACs are shared among all the similar filter legs in other drivers (Fig. 5). A 2-bit differential DAC is used to generate the 4-level, trapezoid pulse modulated PAM code.

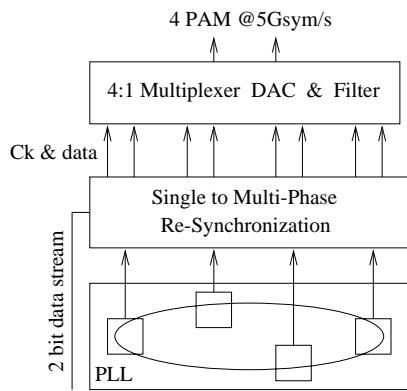


Fig. 4. General Transmitter Architecture

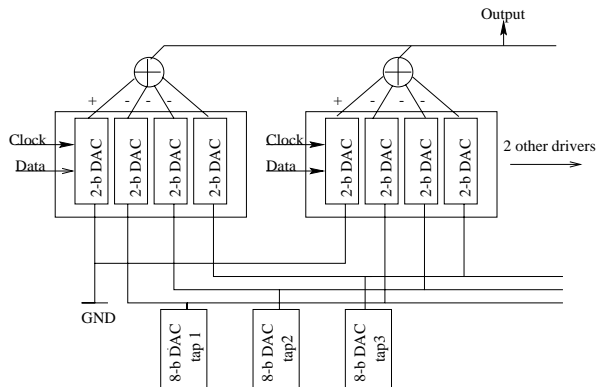


Fig. 5. Transmitter drivers and 3-tap FIR filters

Figure 6 shows the design of the 2-bit DAC module and the differential driving leg circuit. This circuit uses D , \bar{D} , and two clocks which are 200ps out of phase to generate a precise 200ps current pulse [7] with one of the 4 selectable levels. Once the 3 tap weights are determined, no logic is needed to compute the pre-emphasized signal since each driver cancels the tail of its own transmitted symbol.

B. Receiver

The receiver uses 3 times oversampling for data recovery [6] resulting in 67ps sample spacing. Using each sample together with its preceding sample, we can build our 1-tap, 7.5GHz wide, high-pass filter using the circuit shown in Figure 7.

This circuit consists of a main differential buffer with a constant gain and two controllable gain differential stages. The two controllable gain stages perform the following function:

$$V_o(n) = A \cdot V_i(n) + B \cdot (V_i(n) - V_i(n-1)),$$

where n indicates the sample number. Gain is varied in the two stages by changing the gate voltage of the tail transistors. Addition or subtraction of signals is performed by connecting the outputs of the differential pairs with proper polarity. Using cross coupled pairs in the load increases the total gain of the circuit. Increased gain results in decreased input capacitance due to smaller input devices. Since the

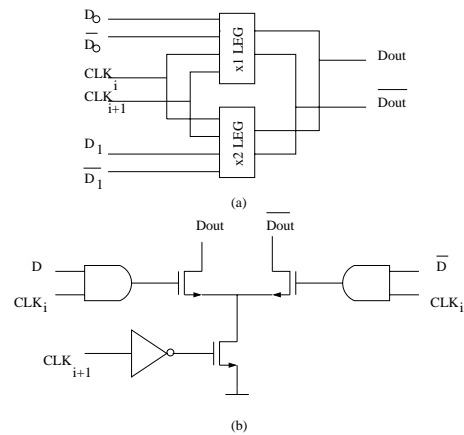


Fig. 6. a) The 2-bit DAC module b) Differential drive leg with clocking logic

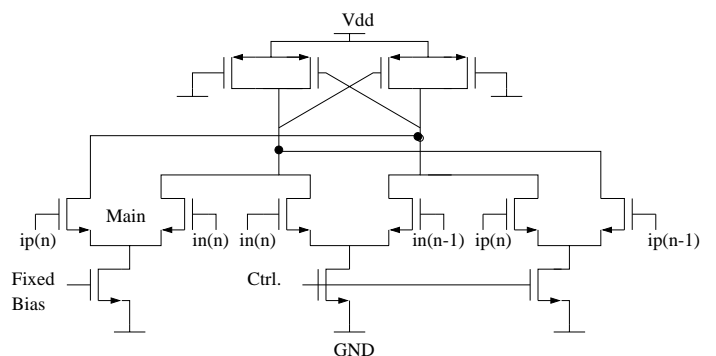


Fig. 7. Receiver Equalizer

oversampling architecture requires 24 input stages, the decrease in input capacitance per stage is greatly beneficial [6]. Another advantage of reducing the input device sizes in the MOS differential pairs is an increased input dynamic range. The increased dynamic range is critical for equalizer operation in the receiver. Due to the parallelization scheme [6] at the receiver, each equalizer stage has half a clock cycle to settle after the data is sampled. Note that the clock cycle is 8 times the symbol period, thus the speed requirements for each equalizer stage are less stringent.

V. SIMULATION RESULTS

The system described in this paper was simulated over all process corners by HSPICE with models for 0.35μ CMOS. To implement the channel, the impulse response of a 12 meter cable was convolved with the transmitter output in the time domain. The resulting waveform was applied to the input filter of the receiver. Figure 8 shows eye-diagrams of several 4-level 5Gsymbol/s signals. Figure 8(a) shows the eye-diagram at the output of an unshaped transmitter. This eye-diagram is used as the reference for comparing receiver eye-diagrams since, under ideal conditions, the two eye-diagrams should be identical. Figure 8(b) shows the eye-diagram for a receiver which does not implement the transmit shaping filter or the equalizer. Observe there is no eye opening in this eye-diagram, thus making data detection impossible. Figure 8(c) shows the eye-diagram for a

receiver which implements the transmit shaping filter *and* the equalizer. Notice, the two filters obtain a large eye opening ($> 250\text{mV}$). Therefore, data detection becomes more immune to noise and is easier to implement. According to previous experimental results [7], an eye opening of 170mV achieves a bit-error rate of $\text{BER} = 10^{-9}$, thus we expect the improved $\text{BER} < 10^{-9}$.

VI. CONCLUSIONS

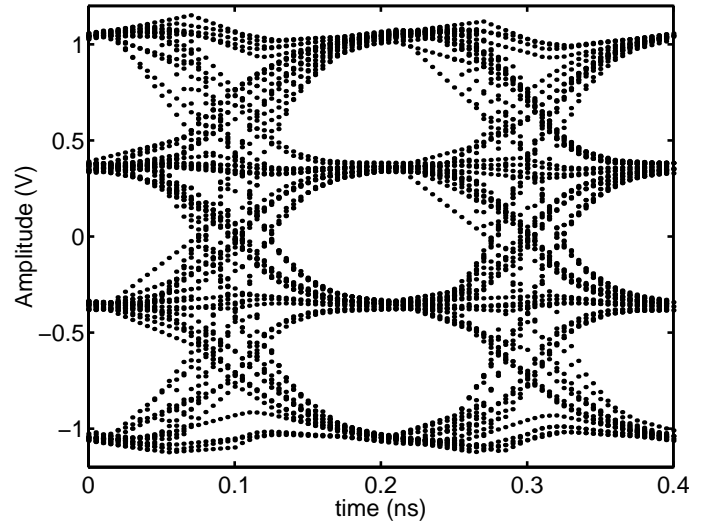
Using transmit pulse shaping, channel equalization, and multi-level modulation enable us to transmit bit rates greater than 10 times the bandwidth of a 12 meter coaxial cable. The equalizer uses a 1-tap, high bandwidth filter at the receiver to sharpen the transition edges. A 3-tap, lower bandwidth filter at the transmitter cancels the long tail of the pulse response. Eye diagrams with wide, large-amplitude openings allow reliable data recovery as demonstrated in both simulation and experiments.

VII. ACKNOWLEDGMENTS

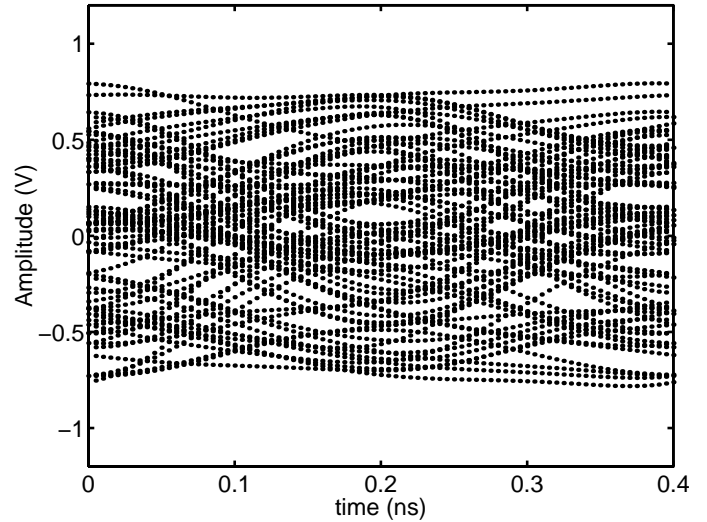
The authors would like to thank Stefanos Sidiropoulos, Maria del Mar Rodriguez-Romero Hershenson, Ali Hajimiri, Hiran Samavati, LSI Logic and MCC for their assistance.

REFERENCES

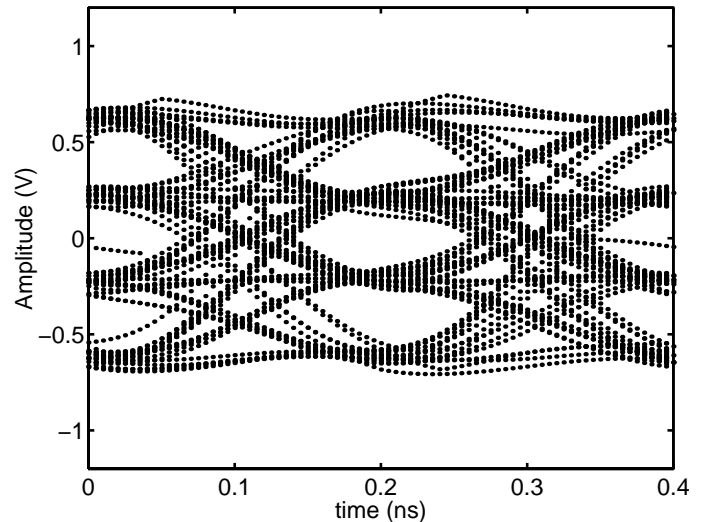
- [1] William J. Dally and John Poulton, "Transmitter Equalization for 4 Gb/s Signaling," Hot Interconnects Symposium, pp. 29-39, August 1996.
- [2] Edward A. Lee and David G. Messerschmitt, "Digital Communications," 2nd Ed, Kluwer Academic Publishers, 1994.
- [3] David A. Johns and Daniel Essig, "Integrated Circuits for Data Transmission Over Twisted-Pair Channels," IEEE JSSC, vol. 32, no. 3, March '97.
- [4] Alan Fiedler, et al., "A 1.0625 Gbps Transceiver with 2X-Oversampling and Transmit Signal Pre-Emphasis," ISSCC Digest of Tech. papers, pp. 238-239, Feb. 1997
- [5] Thomas Kailath, Ali H. Sayed, and Babak Hassibi, "State Space Estimation Theory," course notes, Stanford University, 1997.
- [6] C.-K. Ken Yang and Mark Horowitz, "A 0.8um CMOS 2.5Gb/s Oversampling Receiver and transmitter for Serial Links," IEEE JSSC, vol. 31, no. 12, Dec '96.
- [7] C.-K. Ken Yang, Ramin Farjad-Rad and Mark Horowitz, "A 0.6um CMOS 4Gb/s Transceiver with Data Recovery using Oversampling," VLSI Circuits Symposium, June 1997.



(a)



(b)



(c)

Fig. 8. Eye diagrams for (a) the output of an unshaped transmitter (b) an unshaped transmitter and unequalized receiver after cable (c) a shaped transmitter and equalized receiver