An Equalization Scheme for 10Gb/s 4-PAM Signaling over Long Cables

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Goals

- **Networking high speed computers for 1 to 20 meter distance ranges at lower cost and complexity.**
  - → Parallel buses are costly for long distances.
  - → Optical fibers are also not beneficial for such small ranges.
  - → Serial links on copper cables are an attractive solution for this kind of application.

- **Exploring the bandwidth limitations of CMOS serial links.**
  - → Most commercial multi gigabit transceivers are bipolar or GaAs.
  - → CMOS technology is getting cheaper, faster and more common.

Outline

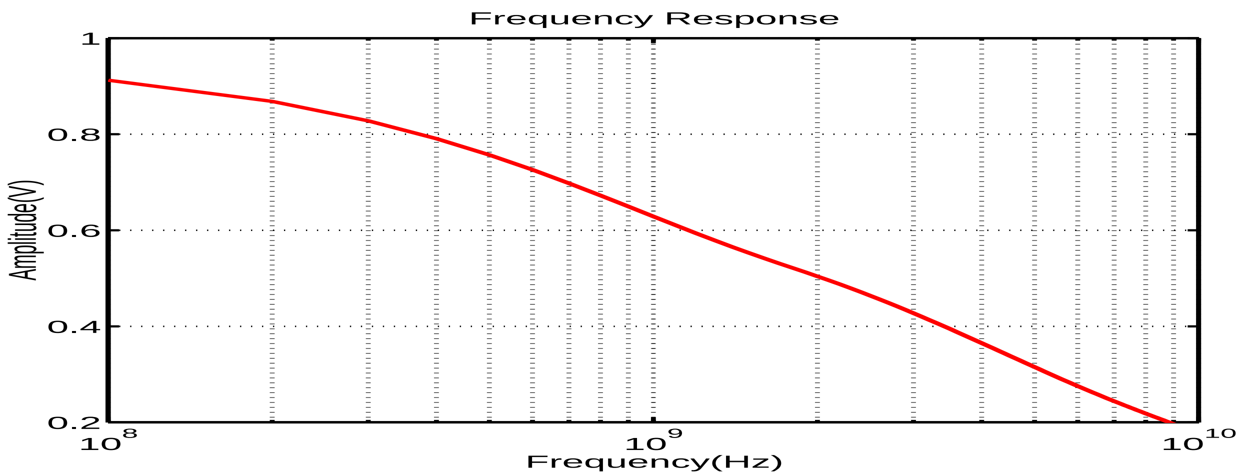
- ✔ *Challenges*
- ❑ System Architecture
- ❑ Circuit Implementation
- ❑ Simulation Results
- ❑ Conclusion

Challenges

- **Circuit issues :**

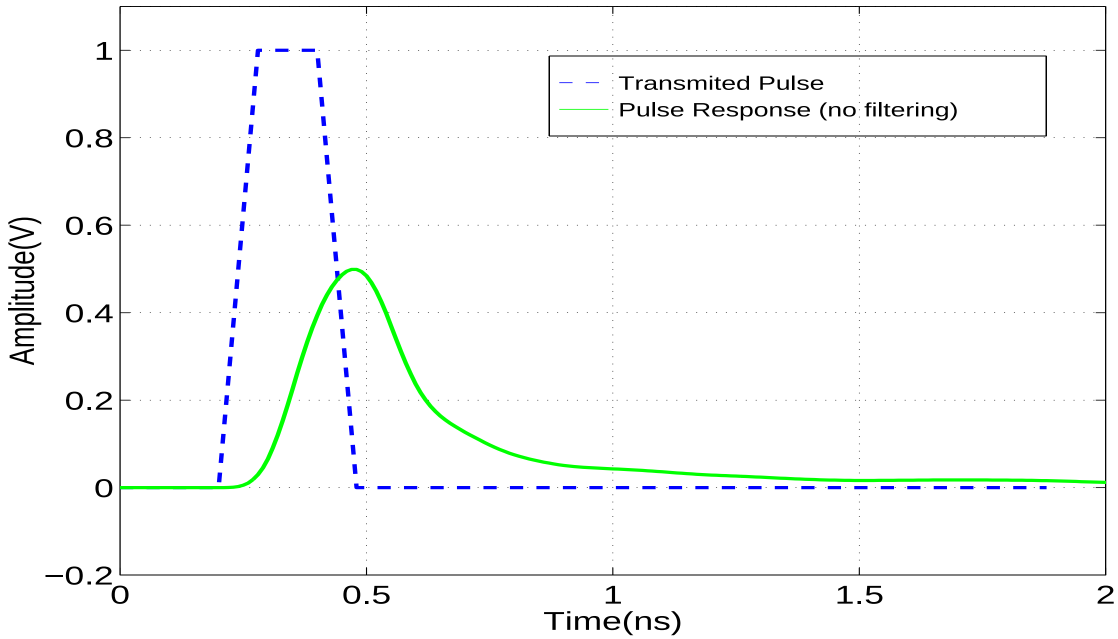
  Noise, limited transistor speed, parasitics, transistor mismatches ...
- **Signal reflection, due to imperfect line terminations, corrupts the received symbol (reflection ISI).**
- **Major Problem : Frequency dependent attenuation in electrical links due to skin effect resistance.**

  → The -3dB BW of 12 meter RG55B/U coax is <1GHz.



Challenges (cont.)

- **Frequency dependent attenuation causes ISI.**
  - → Only channel eigen-waveforms result in no ISI.
  - → Generation and detection of eigen-waveforms is not feasible due to circuit limitations at high frequencies.
  - → Trapezoidal pulses are used as basis waveforms.
  - → Higher symbol rate results in more ISI.



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Proposed Modulation

- **4-PAM is used for data communication in the serial link.**
  - → Symbol rate reduces to half that of the binary transmission.
  - → Lower symbol rate results in less ISI and reduced HF limitations.
  - → Higher level PAM was not used because of :
    limited transmitter swing, minimum detectable signal
    and reflection ISI.
- **4Sym-->5Sym conversion guarantees clock recovery.**
- **Gray code mapping of levels reduces BER by 20% vs. linear mapping.**

Linear	Gray
11	10
10	11
01	01
00	00

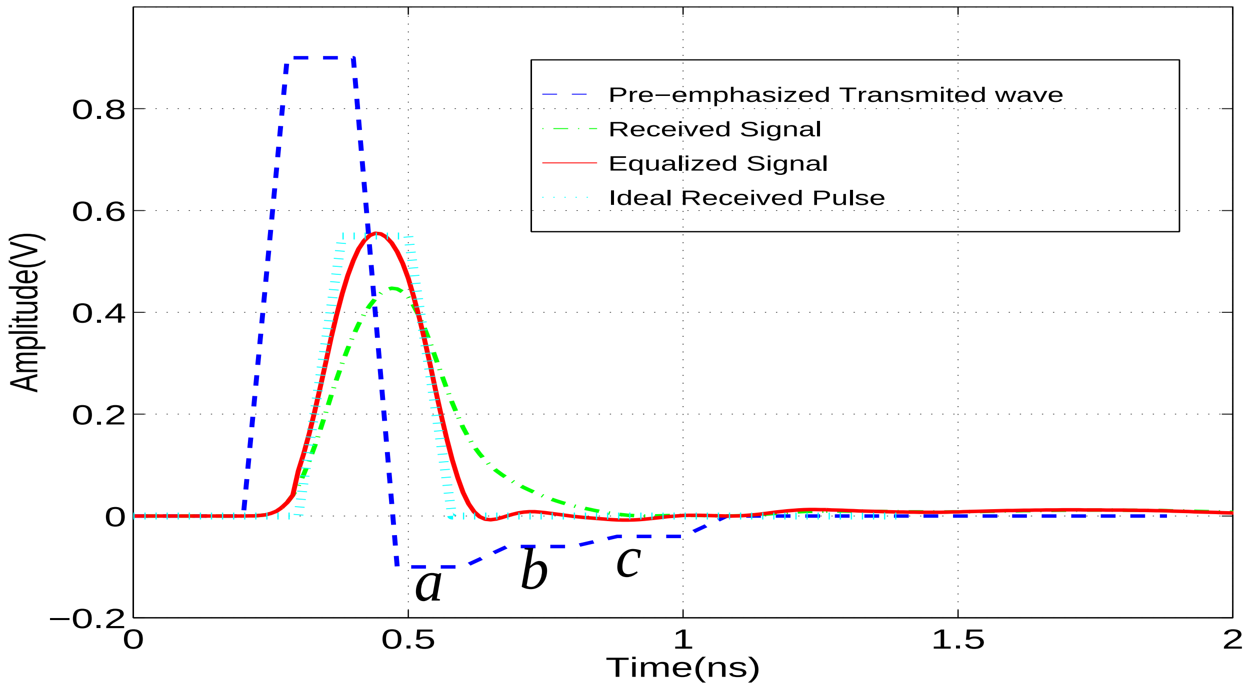
Proposed Architecture to Combat ISI

- **To cancel the long tail of pulse response, a symbol-spaced pre-emphasis 3-tap FIR filter is implemented at the transmitter.**

$$Vo(n) = Vi(n) - a \bullet Vi(n-1) - b \bullet Vi(n-2) - c \bullet Vi(n-3)$$

- **To equalize the high frequency components, a subsymbol-spaced 1-tap high-pass equalizer is implemented at the receiver.**

- **Least square algorithm is used to find the best filter tap weights.**



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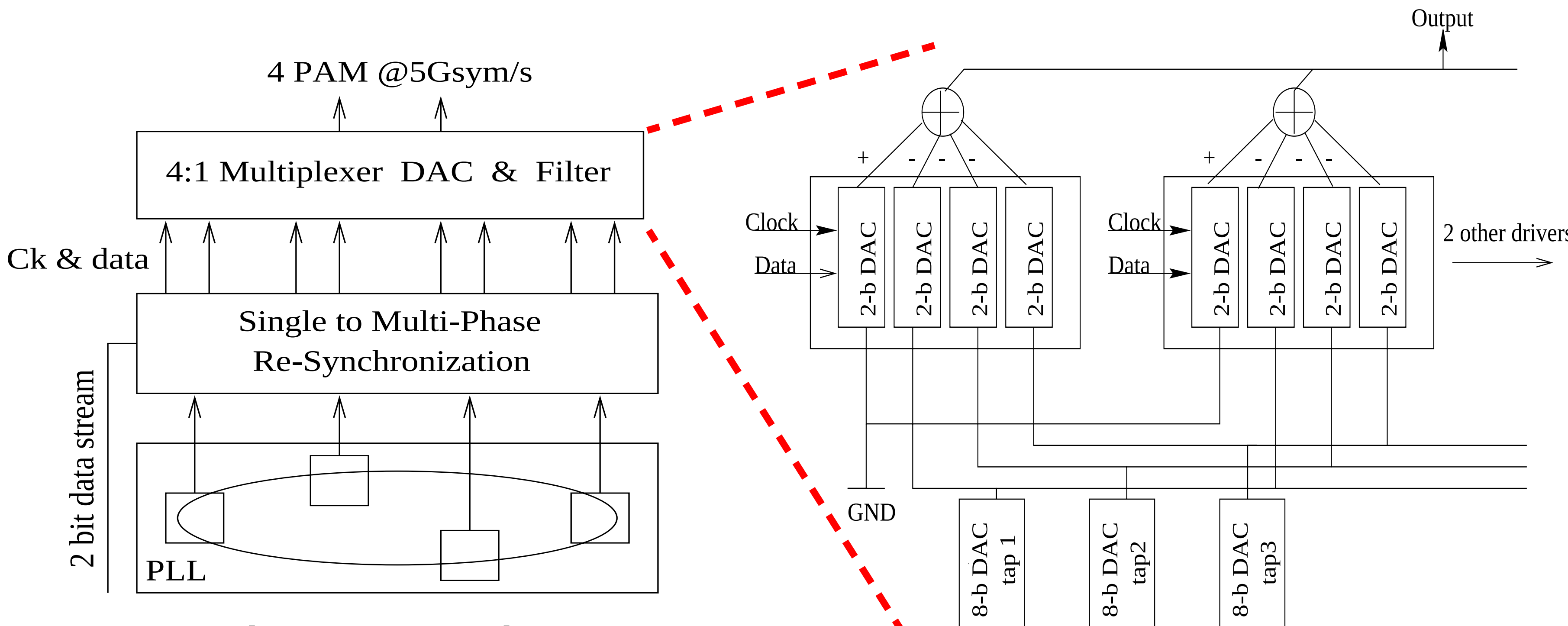
Transmitter Design

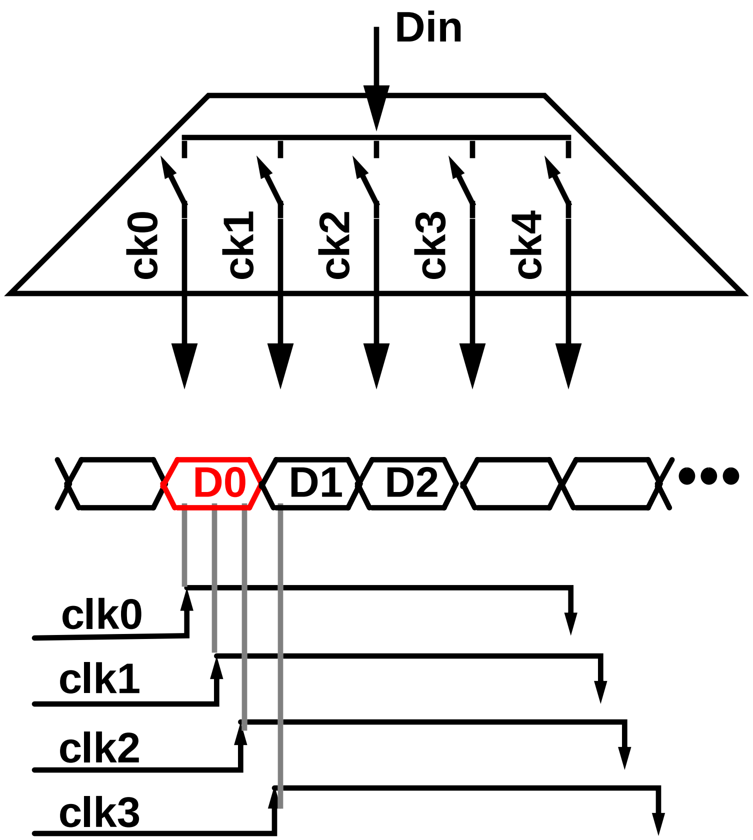


General Transmitter Architecture

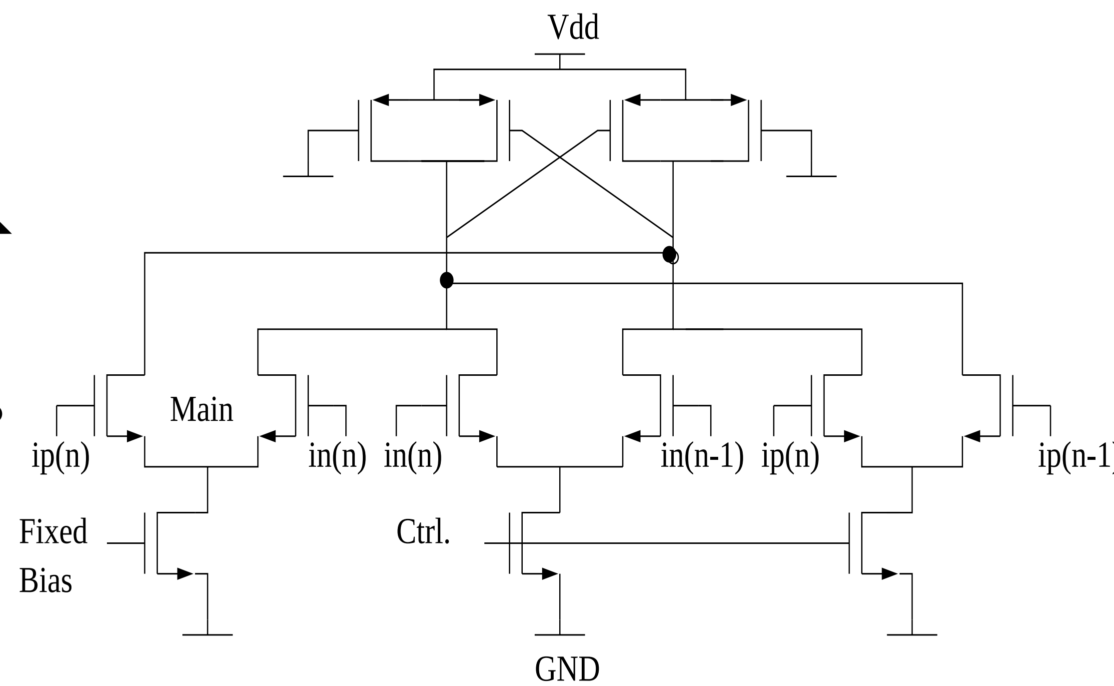
Multiplexer Drivers & 3-Tap Filters

- 2-b DACs generate the 4 levels, 8-b DACs determine the filter tap weights.
- Each driver generates a filtered symbol independent of other drivers.

Receiver Design



3x oversampling shown



$$Vo(n)=A.Vi(n)+B.(Vi(n)-Vi(n-1))$$

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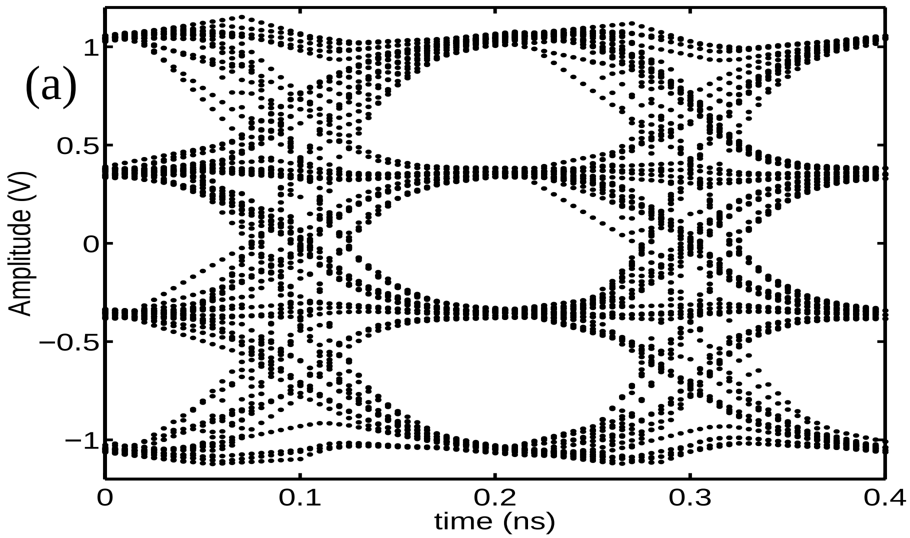
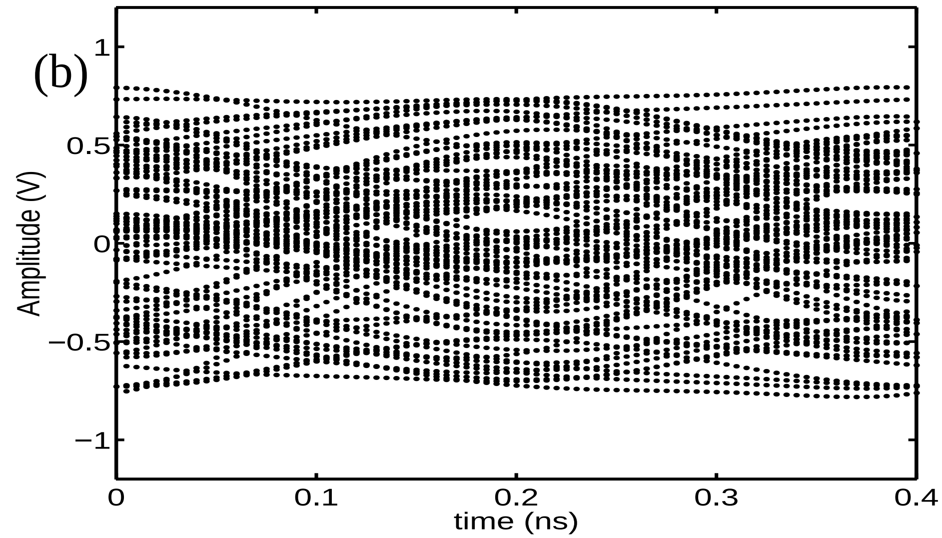
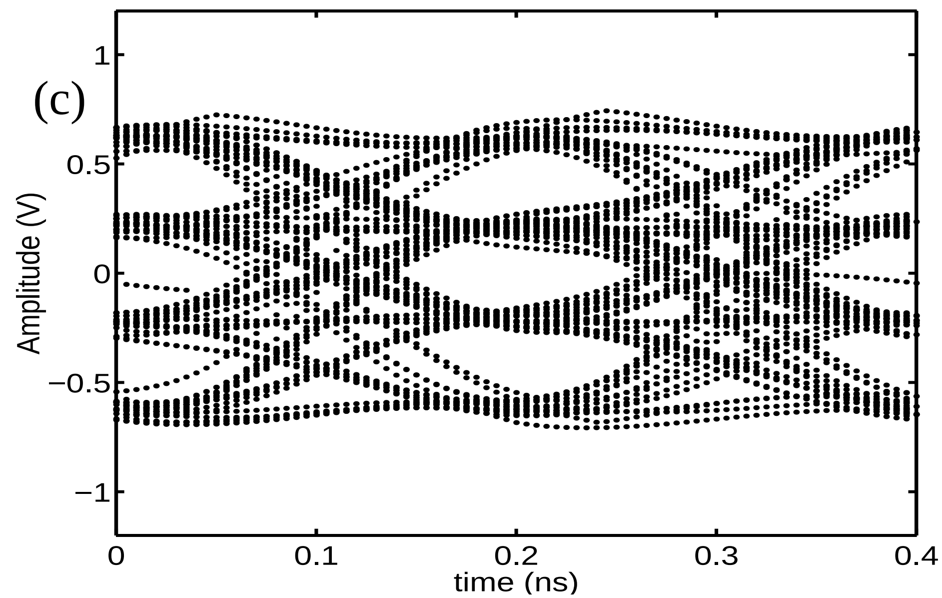
Simulated Eye Diagrams







(a) Eye diagram at source

(b) Eye diagram at end of cable

(c) Equalized eye diagram at end of cable

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Conclusion

- **Main limitation on transmission rate is limited channel bandwidth.**
  - → Limited BW causes ISI on trapezoidal pulses.
  - → Higher symbol rate results in more ISI.
  - → 4-PAM reduces the symbol rate to half that of conventional 2-PAM.
- **Two FIR filters are used to cancel ISI.**
  - → A 3-tap pre-emphasis filter @ transmitter to cancel the long tail.
  - → A 1-tap equalizer @ receiver to sharpen the transition edges.
  - → Receiver equalizer relaxes the swing and frequency constraints on the transmitter.
- **Other approaches to the problem are being investigated.**
- **Using the above techniques, a data rate of 10Gb/s on a 12meter coax with -3dB BW of <1GHz is achieved in 0.35μm CMOS.**

Acknowledgements

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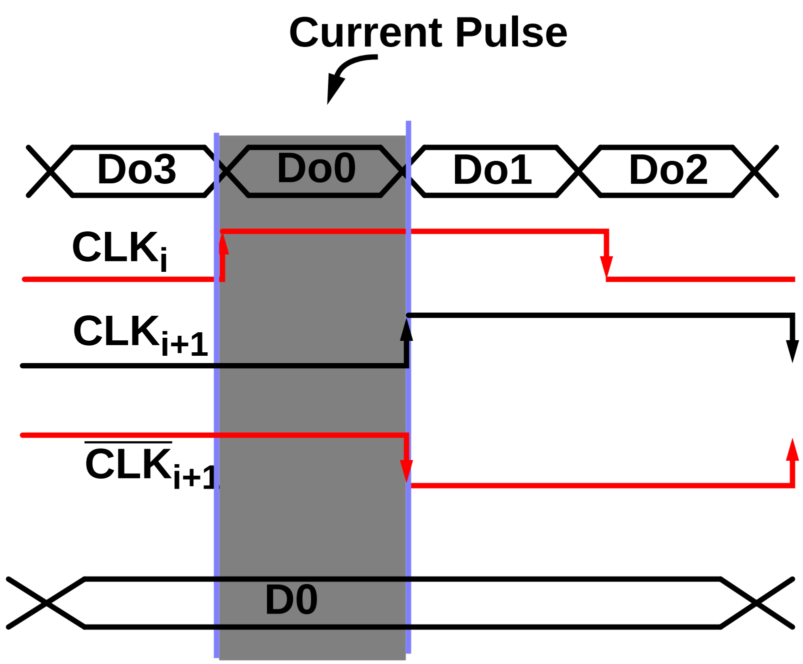
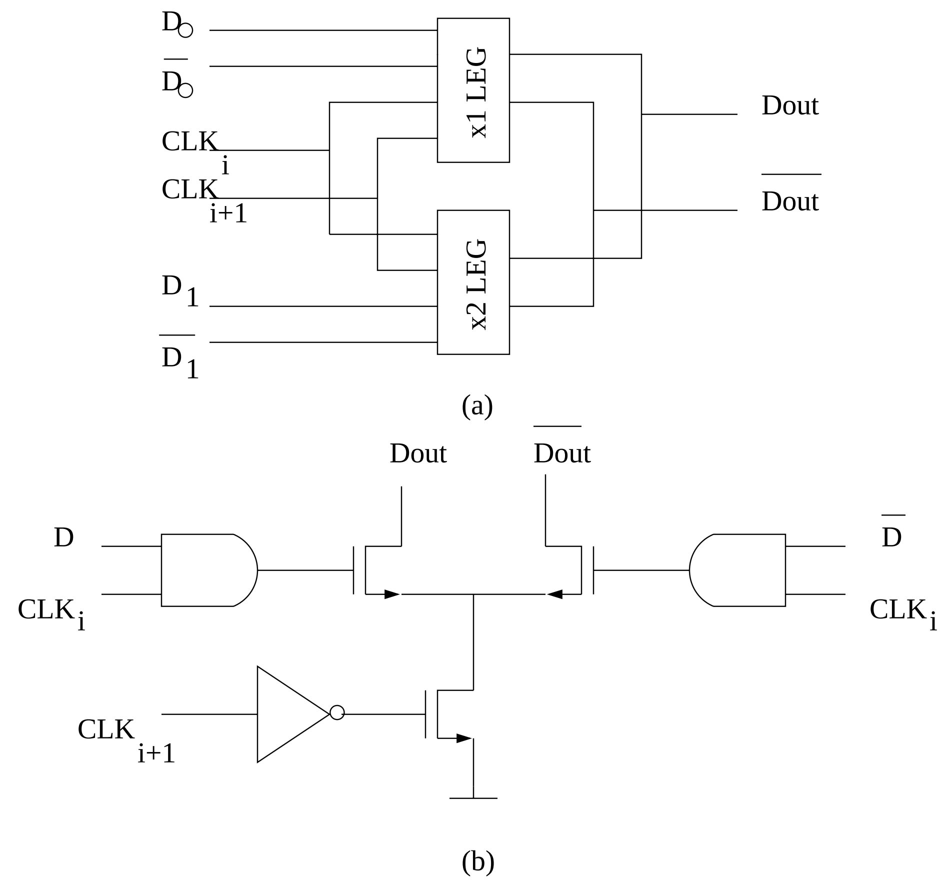
Transmitter Symbol Generation





(a) 2-bit DAC Module

(b)Differential Driver leg