A 1.4-GHz 3-mW CMOS LC Low Phase Noise VCO Using Tapped Bond Wire Inductances

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1. ABSTRACT

A 1.4-GHz LC voltage-controlled oscillator has been implemented in a MOSIS 0.5-μm CMOS process. Complementary cross-coupled PMOS and NMOS transistors enhance single-ended symmetry at each of the resonant nodes, reducing close-in phase noise. Tapped bond wires provide a resonant tank with high Q. At an offset frequency of 100 kHz, the measured phase noise is -107 dBc/Hz with 3 mW power dissipation from a 3.0 V supply. NMOS gate capacitors achieve a 17% tuning range.

2. INTRODUCTION

The popularity of personal communication systems in the GHz range urges circuit designers towards more compact and more cost-effective solutions. The current target is a monolithic RF receiver, where one of the largest hurdles is a fully integrated, low noise, low power voltage-controlled oscillator (VCO). For higher quality receivers, an LC oscillator topology is chosen over a relaxation oscillator because the bandpass nature of the resonant tank in the LC oscillator provides the lowest phase noise for a given amount of power.

However, the Q of the resonator is degraded by the parasitics of the circuitry connected to it. Tapping one of the components, by simply connecting the feedback network across a part of the inductor, will reduce these losses by a factor proportional to the tapping ratio.

In addition, the feedback network can be configured to optimize symmetry, which has also been shown to improve phase noise [1][2]. Not only is it important to maximize the differential symmetry to achieve a low phase-noise oscillator, but also to maximize single-ended symmetry, such as the charging and discharging strength on the output node. This additional single-ended symmetry will minimize the low frequency device noise up-converted into the output frequency spectrum, further lowering the overall phase noise.

In this paper, we present such an LC voltage-controlled oscillator fabricated through MOSIS in a 0.5-μm CMOS process using bond wires to implement the inductors.

3. LC VCO DESIGN

The primary trade-off in the design of an integrated oscillator is between low phase noise and power dissipation. It is well-known that a high Q resonator will filter the output of the oscillator and improve phase noise. Therefore, bond wires are chosen for the inductors for their low series resistance and their flexibility in bonding. For testing purposes, various lengths of bond wires could be appraised, yet once the optimum length is found, the excellent repeatability of automatic die attach equipment ensures precision in value.

There are two additional approaches for minimizing phase noise. One is to use a tapped resonator, as in a Clapp oscillator, recently made by Craninckx and Steyaert [3]. In a tapped configuration, the parasitics associated with any additional circuitry do not appear directly across the LC tank. Instead, they appear solely across a portion of the inductor. Thus, the entire tank is affected by the amount of loss divided by the tapping ratio formed by the inductors. In addition, the tapping allows the voltage swing across the LC resonator to exceed the power supply. Both of these benefits effectively increase the signal-to-noise ratio of the oscillator.

The second approach is to enforce single-ended waveform symmetry, as explored in [2]. Many designers have previously presumed that the $^1/_f3$ phase noise corner coincides with the $^1/_f$ device noise corner. The Hajimiri phase noise model [1] reveals that the $^1/_f3$ phase noise corner is affected by the waveform symmetry of the oscillator, and differs from the device $^1/_f$ corner. The trade-off between low phase noise and power dissipation still exists in the $^1/_f2$ region, but there is room for improvement in the $^1/_f3$ region by exploiting properties of symmetry. This improvement is of great importance for CMOS oscillators, since CMOS transistors exhibit a high $^1/_f$ noise corner. Noise sources in each half circuit are uncorrelated with the noise sources in the other half circuit; thus, the noise cannot be treated simply as a common-mode signal. Therefore, any asymmetry in the

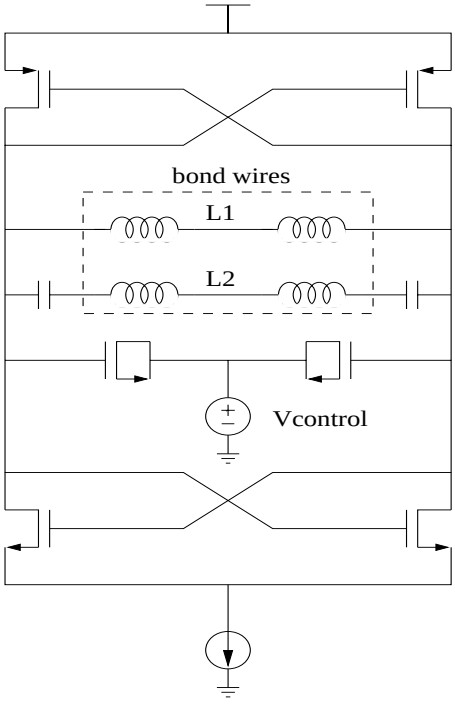

Figure 1. Circuit Diagram

single-ended waveform allows low frequency noise to be upconverted and increase the $^1/_f3$ corner of the phase noise.

In this paper, we focus on combining the benefits of these two methods. For testing the viability of reducing phase noise through the use of single-ended symmetry and the advantages of tapping, we chose the negative-resistance topology shown in Figure 1. The goal of this design was a 1.6-GHz LC VCO with minimum phase noise on 1 mA with a 3.0 V supply.

The cross-coupled NMOS transistors provide the negative resistance to cancel the losses presented by the parallel LC tank at resonance. The cross-coupled PMOS transistors are twice the width of their NMOS counterparts and increase the loop gain. More important, the PMOS devices allow better symmetry to be achieved on each of the resonant nodes by equating the positive and negative drive strength. It is this attention to symmetry on both the full circuit and each half circuit that reduces phase noise.

If the oscillator swing was to become voltage limited, the PMOS and NMOS transistors would no longer remain in the saturation region for the entire oscillation cycle. For the period of time that they entered the linear region, they would no longer present a negative resistance to the LC tank. This periodic loading would degrade the phase noise. In this design, however, the interconnects limit the amount of power the system can handle, and in its entire operating region, the oscillator swing is current limited. Therefore, as the power increases, the phase noise decreases by a proportional amount.

Four bond wires comprise the tank inductance. For each inductor, one traverses from the bond pad on the die to the package, and the other follows the return path. This method maintains symmetry between the differential output nodes. About 9 nH of inductance is supplied by 9 mm of bond wires. The extra capacitance of the package at the center of the two inductors is unimportant since this node is a differential-mode ground. The negative-resistance circuitry is connected across L1, which is approximately 5nH. Since L2 is approximately 4nH, the tapping ratio becomes 1.8.

The varactors are implemented by standard NMOS gate capacitors operated near threshold. There are two capacitors, each with the gate connection to the resonant nodes. Using two capacitors easily preserves symmetry, while the shared drain/source node is driven by the control voltage. The losses in this type of capacitor are large, though, leading to a lower Q value and degradation of phase noise. Therefore, its magnitude was chosen to be a small percentage of the total effective tank capacitance, while remaining large enough to provide adequate tuning range.

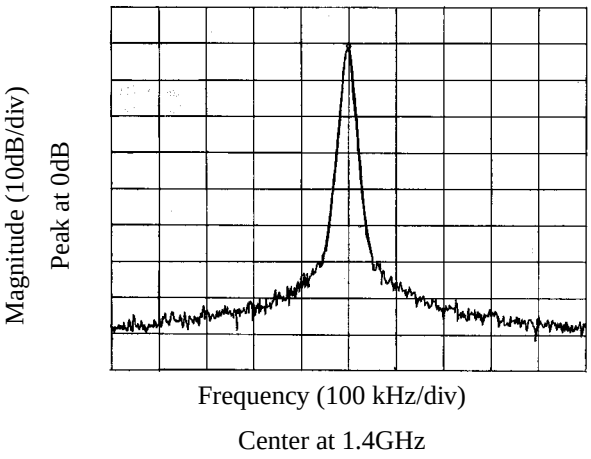

Figure 2. Output Spectrum of Oscillator

4. EXPERIMENTAL RESULTS

The output of the oscillator is connected to the gates of an open-drain differential pair, once again preserving the symmetry of the resonant nodes. One of these open drain transistors drives the spectrum analyzer and the other is simply connected to the power supply. Both are terminated with 50 ohms. The 1.4GHz output spectrum of the oscillator is shown in Figure 2.

Due to a lay-out error, the varactor is twice the desired size. This results in a lower maximum frequency, 1.4GHz, instead of the designed target frequency of 1.6GHz. This error can be corrected through an adjustment of the bondwire lengths since there is ample loop gain to sustainthe oscillation in the presence of the extra losses associated. with the larger varactor capacitor.

	Tech	Inductor	Method	Frequency	Power	Phase Noise at Δ100kHz	Figure of Merit
This Work	CMOS	bond wires	tapping/ symmetry	1.4 GHz	3 mW	-107 dBc/Hz	315 dBF
Ref [2]	CMOS	bond wires	symmetry	1.6 GHz	0.5 mW	-95 dBc/Hz	312 dBF
Ref [3]	CMOS	bond wires	tapping	1.8 GHz	24 mW	-109 dBc/Hz	310 dBF
Ref [4]	BJT	bond wires	-	1.1 GHz	2 mW	-105 dBc/Hz	312 dBF
Ref [5]	BiCMOS	spiral	-	1.8 GHz	70 mW	-88 dBc/Hz	285 dBF
Ref [6]	CMOS	active	-	1.8 GHz	6 mW	-105 dBc/Hz	312 dBF
Ref [7]	BJT	off-chip	-	1.6 GHz	3 mW	-95 dBc/Hz	304 dBF

Table 1: Comparison of various LC oscillators

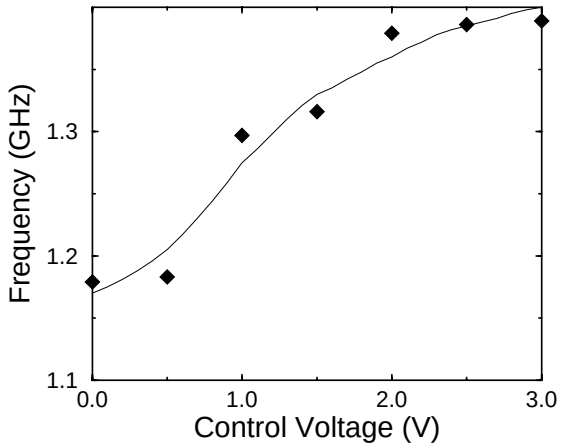

Figure 3. Output Frequency VersusCcontrol Voltage

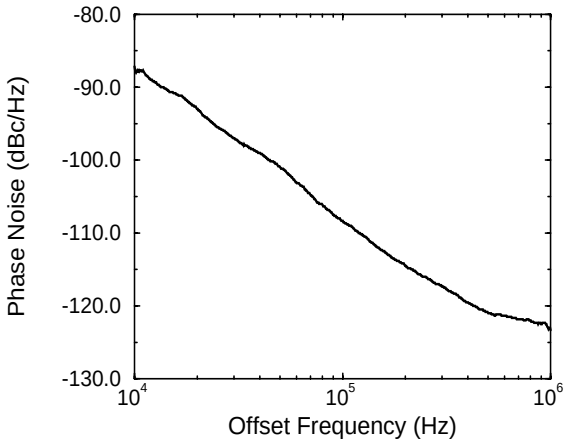

Figure 4. Phase Noise Versus Offset Frequency

However, instead of the designed 10% tuning range, the varactor adjusts the oscillating frequency from 1.18 GHz to 1.40 GHz, representing a 17% tuning range. Figure 3 shows the VCO's frequency versus voltage characteristic.

The phase noise, measured on an HP 8563E spectrum analyzer, is -107 dBc/Hz at 100 kHz offset for the 1.4-GHz signal. At 10kHz offset, the phase noise is -83dBc/Hz for the same 1.4-GHz signal. A graph of the phase noise versus offset frequency is presented in Figure 4.

The phase noise, when tested over the entire tuning range, shows less than 0.5 dBc/Hz fluctuation. Even with power variations of a factor of 2, the phase noise is within 1.0 dBc/Hz over its respective tuning range.

Comparison with previous work is difficult since many other LC oscillators operate at different frequencies and power levels. We offer this simple figure of merit (FOM) to examine various results:

FOM(dBF) = 20 log (freq) - phase noise - 10 log (power)

Since the phase noise improves in proportion to an increase in power, logarithmic value of these quantities can be subtracted. Phase noise is reported as a negative quantity, so it must also be subtracted. Lastly, phase noise degrades in proportion to frequency squared [1], so that is taken into account outside the logarithm

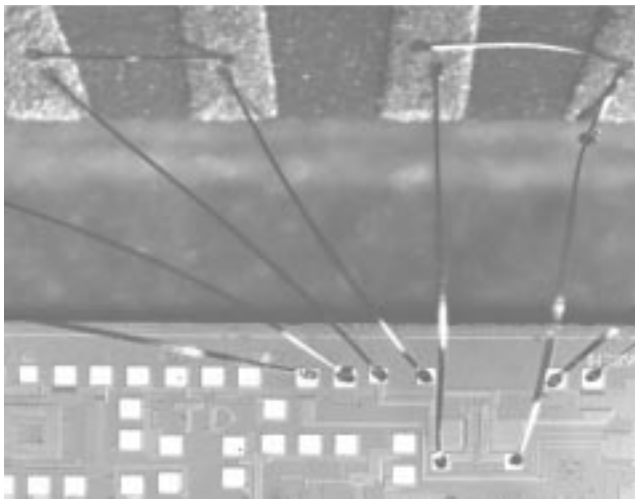

Figure 5. Die Photo of Oscillator and Bond Wire Inductors

Table 1 displays a list of various LC oscillator topologies and their subsequent figures of merit. While an oscillator design that utilizes single-ended symmetry excels, so does one exploiting a tapped inductive structure. To the authors' knowledge, this work is the first to combine these methods of minimizing phase noise, resulting in at least a 3dBF improvement over any other LC oscillator in the table.

A summary of the experimental results for the tapped and symmetrically-enhanced design is provided in Table 2. In addition, Figure 5 is provided to show the bond wire configuration used.

5. CONCLUSION

We have demonstrated the viability and performance of tapped bond wire inductance in a 1.4-GHz LC VCO fabricated in a standard 0.5-µm CMOS process. The design yields -107 dBc/Hz phase noise at an offset frequency of 100 kHz on 3.0 mW. This achievement is a result of lowering the $^{1}/_{f}3$ corner by enforcing a previously unappreciated symmetry constraint on each of the two differential output nodes of the oscillator while tapping the resonant tank to reduce the effects of parasitics.

6. ACKNOWLEDGEMENTS

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Frequency	1.4 GHz
Supply Voltage	3.0 volts
Power Consumption	3.0 mW
Tuning Range	220 MHz
Phase Noise @ 10kHz	-83 dBc/Hz
Phase Noise @ 100 kHz	-107 dBc/Hz
Phase Noise @ 600 kHz	-122 dBc/Hz
Process Technology	0.5-µm standard CMOS

Table 2: Summary of Results

7. REFERENCES

[1] Hajimiri, A. and Lee, T., "A general theory of phase-noise in electrical oscillators," *IEEE Journal of Solid-State Circuits* (Feb. 1998)

[2] Ahrens, T., Hajimiri, A., and Lee, T., "A 1.6GHz 0.5mW CMOS LC low phase noise VCO using bond wire inductance," International Workshop on Design of Mixed-Mode Integrated Circuits and Applications (July 1997), pp. 69-71.

[3] Craninckx, J. and Steyaert, M., "A 1.8GHz CMOS low-phase-noise voltage controlled oscillator with prescaler." *IEEE Journal of Solid-State Circuits* (Dec. 1995) vol.30, no.12, pp.1474-82.

[4] Steyaert, M. and Craninckx, J., "1.1GHz oscillator using bondwire inductance," *Electronics Letters* (3 Feb. 1994) vol. 30, no.3, pp.244-5.

[5] Nguyen, N.M. and Meyer, R., "A 1.8GHz monolithic LC voltage-controlled oscillator," *IEEE Journal of Solid-State Circuits* (March 1992) vol.27, no.3, pp.444-50.

[6] Craninckx, J. and Steyaert, M., "Low-noise voltage-controlled oscillators using enhanced LC-tanks," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing* (Dec. 1995) vol.42, no.12, pp.794-804.

[7] Piazza, F. and Huang, Q., "A 12mA triple-conversion receiver for GPS," *ISSCC Dig. of Tech. Papers*, 1996, pp. 286-287.