CMOS VCOs for Frequency Synthesis in Wireless Biotelemetry

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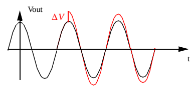
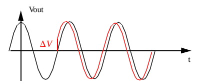
Phase Noise Theory

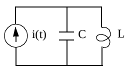
Oscillators are Time-Variant Systems



- Current impulse injected at the peak changes the amplitude and has no effect on the phase.



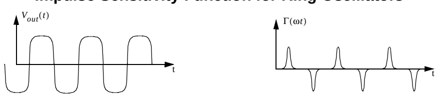
- Current impulse injected at zero-crossing changes the phase and has minimal effect on the amplitude.



$$h_\phi(t,\tau) = \frac{\Gamma(\omega_0\tau)}{q_{max}}u(t-\tau)$$

- Impulse Sensitivity Function $\Gamma(x)$ is periodic.
- q_{max} is the maximum charge displacement in the tank.

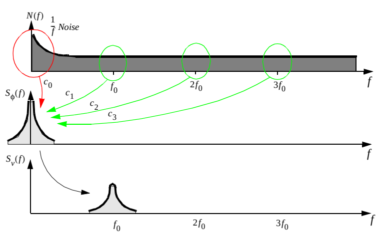
Impulse Sensitivity Function for Ring Oscillators



$$\phi(t) = \frac{1}{q_{max}}\left[\frac{c_o}{2}\int_{-\infty}^{t} i(\tau)d\tau + \sum_{n=1}^{\infty} c_n \int_{-\infty}^{t} i_n(\tau)\cos(n\omega\tau)d\tau\right]$$

- $\Gamma(x)$ is calculated from the output waveform.
- $\Gamma(x)$ is expressed as a Fourier series and used to determine the phase noise resulting from noise sources.
- High sensitivity to noise at the transitions of the output waveform

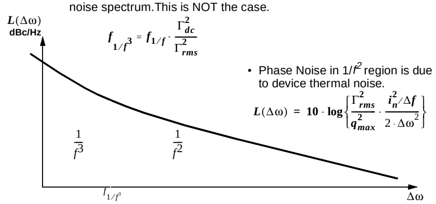
Upconversion of Device *1/f* Noise



- Phase noise close to the carrier results from the folding of device noise centered at integer multiples of the carrier frequency.
- Upconversion of device 1/*f* noise occurs through Γ_{dc}, the DC value of the ISF.
- Γ_{dc} is governed by the symmetry properties of the waveform.

Hajimiri Phase Noise Model

- Phase Noise in $1/f^3$ region is due to device 1/*f* noise.
- It is commonly assumed that the $1/f^3$ corner of phase noise is the same as the *1/f* corner of the device noise spectrum.This is NOT the case.

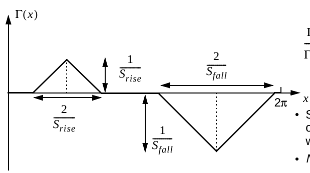


$$f_{1/f^3} = f_{1/f}\cdot\frac{\Gamma_{dc}^2}{\Gamma_{rms}^2}$$

- Phase Noise in $1/f^2$ region is due to device thermal noise.

$$L(\Delta\omega) = 10\cdot\log\left\{\frac{\Gamma_{rms}^2}{q_{max}^2}\cdot\frac{\overline{i_n^2}/\Delta f}{2\cdot\Delta\omega^2}\right\}$$

Calculation of Γ_{rms} and Γ_{dc} for Ring Oscillators



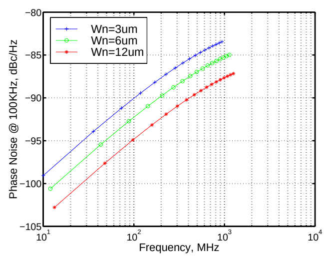
$$\frac{\Gamma_{dc}^2}{\Gamma_{rms}^2} = \frac{3}{2N}\cdot\frac{(1-\beta)^2}{(1-\beta+\beta^2)}$$

$$\beta = \frac{S_{rise}}{S_{fall}}$$

- S is the maximum slope of the normalized output waveform
- *N* is the number of stages

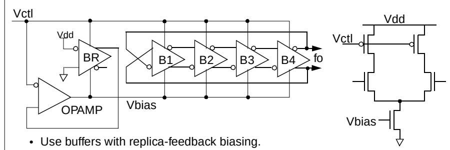
Phase Noise of Differential Ring Oscillator ($1/f^2$ region)

$$L\{\Delta f\} \geq \frac{18kTV_{dd}}{\pi^2 P}\cdot\left(\frac{2.5}{E_C L_{eff}}+1\right)\cdot\left(\frac{f_o}{\Delta f}\right)^2\cdot N \quad \textbf{(Lower bound)}$$



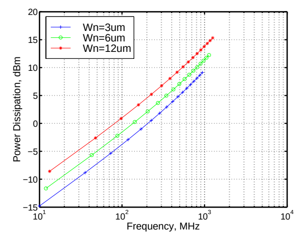
- *N* is number of stages
- Minimum length short-channel differential pair devices
- L_{eff} = 0.5µm
- E_c = 5.6x10^{6}V/m

Voltage-controlled Oscillator Design



- Use buffers with replica-feedback biasing.
- NMOS differential pairs with linear PMOS loads.
- V_{ctl} changes the bias I_{dd} of the buffers.
- Replica bias ensures loads are mostly in their linear region by forcing the maximum single-ended swing $V_s = V_{dd} - V_{ctl}$
- Frequency is controlled by changing the bias of the buffers and hence the delay through each cell.
- Power dissipation is determined by frequency and phase noise required.

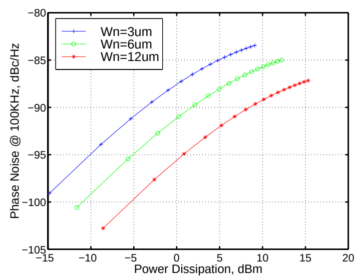
Power Dissipation of Differential Ring Oscillator



$$P \cong 2N^2 C_L V_{dd} V_s f$$

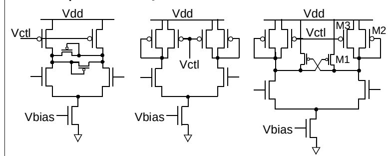
- *N* is number of stages
- C_L is total load capacitance at each buffer
- V_s is maximum single-ended swing
- V_{dd} is 3.3V

Phase Noise vs. Power Dissipation

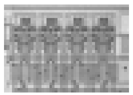


***Selected W_n=6µm* for 200MHz at 2.1dBm (1.6mW), -90dBc/Hz @ 100KHz**

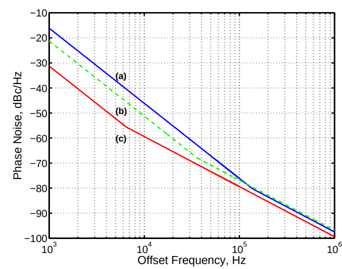
Differential Buffer Topology



- Sweep width of cross-coupling devices with fixed total width ($W_1+W_2=W_3=6\mu m$) of the loads.
- Maximum symmetry for $W_1=W_2=0.5W_3$



Comparison of Phase Noise



Oscillator	$1/f^3$ corner	L{100KHz}
(a) Clamped Load	137KHz	-75dBc/Hz
(b) Symmetric Load	36KHz	-77dBc/Hz
(c) Cross-coupled Load	6.5KHz	-80dBc/Hz

- *Assumed* $f_{1/f}$ = 3MHz
- $1/f^2$ regions are within 2.6dB as expected for similarly sized noise sources.
- $1/f^3$ corner for cross-coupled load buffer is 20 times lower than that of the clamped load.
- Good agreement with measurements previously reported for clamped load buffer.

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