SP 22.3: A 12mW Wide Dynamic Range CMOS Front-End for a Portable GPS Receiver

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At submicron channel lengths, CMOS is an attractive alternative to silicon bipolar and GaAs MESFET technologies for use in wireless receivers. A 12mW global positioning system (GPS) receiver front-end, comprising a low noise amplifier (LNA) and mixer implemented in a standard 0.35µm digital CMOS process, demonstrates the aptitude of CMOS for portable wireless applications.

A block diagram of the receiver front-end test is shown in Figure 1. The system consists of a LNA, mixer, buffer (for testing purposes only), and associated bias circuitry. Note that the LNA output and mixer input are taken off-chip to facilitate testing of each block individually.

To achieve a wide dynamic range, the noise figure of the LNA and linearity of the mixer are of primary concern. Figure 2 shows the circuit schematic of the LNA. A differential architecture is chosen in anticipation of eventual integration of a complete GPS receiver. Its common mode rejection eases the task of rejecting interference from other on-chip elements, such as a DSP core. This choice results in increased amplifier noise for a given power dissipation compared to a single-ended implementation. This increase is mitigated by the high ω_t of the process, that permits acceptable noise performance despite a differential implementation.

The input stage, consisting of $M_{1,2}$ and $L_{1,2}$, uses inductive source degeneration to generate a real term in the differential input impedance equal to $\omega_t(L_1+L_2)$ that can be matched to the off-chip transmission lines from the image-reject filter. By resonating the input capacitance of the amplifier, the minimum possible noise figure can also be achieved [1]. A minimum exists due to the presence of induced gate noise in MOS devices, as described in Reference 2. The source degeneration inductors, $L_{1,2}$, are implemented as on-chip spiral inductors.

The output signal from $M_{1,2}$ flows through cascoding devices $M_{3,4}$ and on to a parallel-tuned output stage formed by $M_{7,8}$. The tuning inductors, $L_{3,4}$, are 3nH on-chip spirals. They serve the additional purpose of sharing the bias current between the first and second stages, leading to reduced power consumption. $M_{5,6}$ are ac coupling capacitors, while R_6 and R_9 provide simple pull-up biasing for the gates of $M_{7,8}$. This arrangement allows signal voltages at the gates of the output stage to swing above the supply, which is advantageous for low-voltage operation. Note that resistors $R_{7,8}$ are off-chip 50Ω loads.

To bias devices M_1-M_4, an active common-mode feedback maximizes the use of limited supply headroom. Through the action of a simple operational amplifier, formed by M_{12}-M_{16}, the V_{gs} of the input devices is used as a reference for biasing the cascode stack. This permits the amplifier to operate reliably on a 1.5V supply, independent of process, supply, and temperature variations.

The forward gain (S21) and noise figure of the LNA are plotted in Figure 3. The LNA exhibits an S21 of 17.7dB and a noise figure of 3.8dB at 1.575GHz. This is achieved with 12mW dissipation from a 1.5V supply. Note that a single-ended implementation of the amplifier would have a 2.3dB noise figure. Although suffering increased noise, the differential architecture permits a reverse isolation of -52dB, unattainable in a single-ended version.

A simplified mixer schematic is shown in Figure 4. Note that some of the biasing details have been omitted. The local oscillator and its inverse, $\overline{LO}$, control which pair of transistors M_1-M_4 is on, and thus the polarity with which the load is presented to the RF port. It is this switching of polarity that establishes mixing. A unique feature of this mixer is the reactive termination of both the RF and IF ports. A capacitive IF termination offers the advantage that it contributes no noise to the mixing process. At the RF port, a reactive tank is used to filter broadband noise from the source resistance and parasitic tank resistance, as well as the switches. Bond wires are used to achieve a good Q in addition to an innovative capacitor layout described in the next paragraph. A further improvement is the addition of inductors in series with the input source resistance to form an L-match together with part of the tank capacitance. This boosts the signal voltage and enhances filtering by increasing the effective source resistance.

Area-efficient linear capacitors are generally unavailable in standard digital process technologies (such as the one used here). However, deep submicron processes do allow small spacing between metal lines on any given interconnect layer, leading to high coupling capacitance. While this property is normally considered undesirable, it is exploited in this design to augment the ordinary parallel plate capacitance.

By operating the transistors in the linear region, good mixer linearity is achieved. The high impedance at the mixer IF port afforded by the on-chip environment improves linearity by reducing the signal currents in the MOS switches. Additionally, a large linear tank capacitor dominates the transistor non-linear parasitic capacitances.

The results of a two-tone IP3 measurement on the mixer are shown in Figure 5. Note that the impedance level at the mixer output is not 50Ω. Indeed, the impedance is complex, so the mixer output quantities are expressed in dBV rather than dBm. The mixer has a -3.6dB voltage conversion gain, with an input-referred IP3 of +10dBm and an input 1dB compression point of -5dBm. Measured mixer SSB noise figure is 10dB. For these measurements, the LO drive amplitude is equivalent to the voltage swing associated with -3.5dBm into 100Ω. However, the LO port presents a nearly capacitive reactance, and hence actually dissipates little power.

The results of experimental measurements are summarized in Table 1. The LNA-mixer combination exhibits the best performance achieved to date of any CMOS implementation in this frequency range at this power level.

Acknowledgments:

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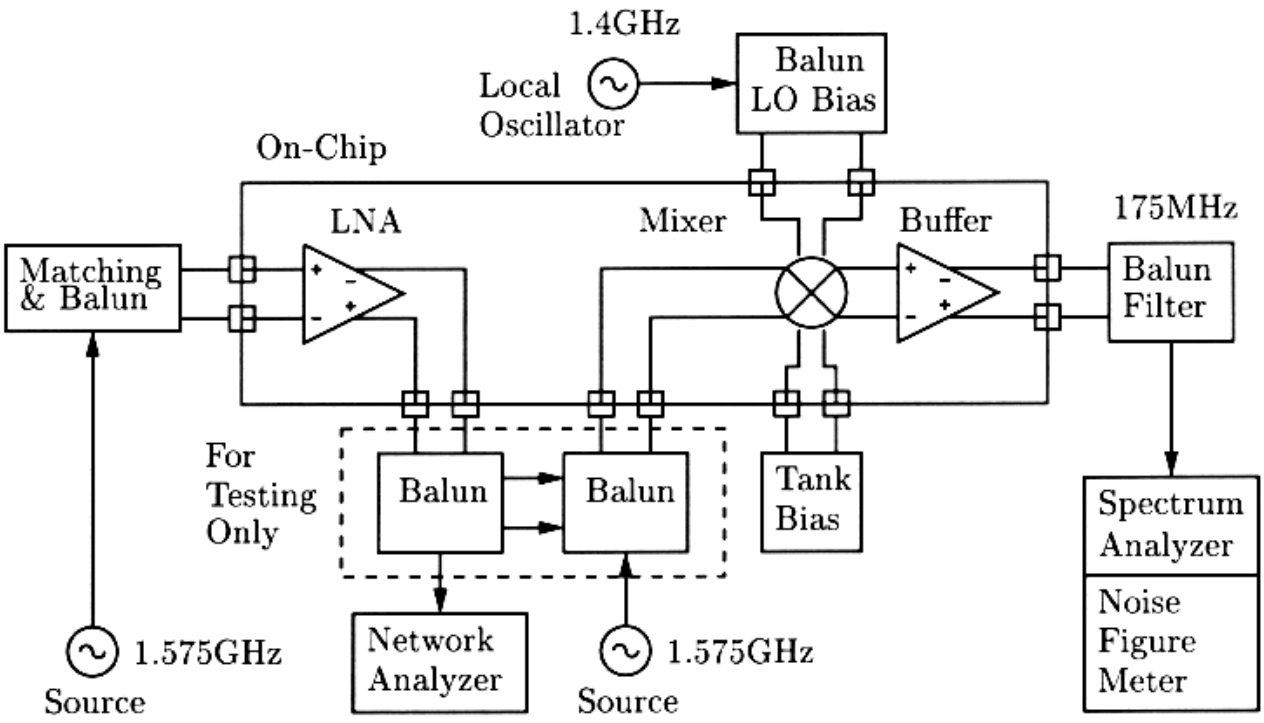
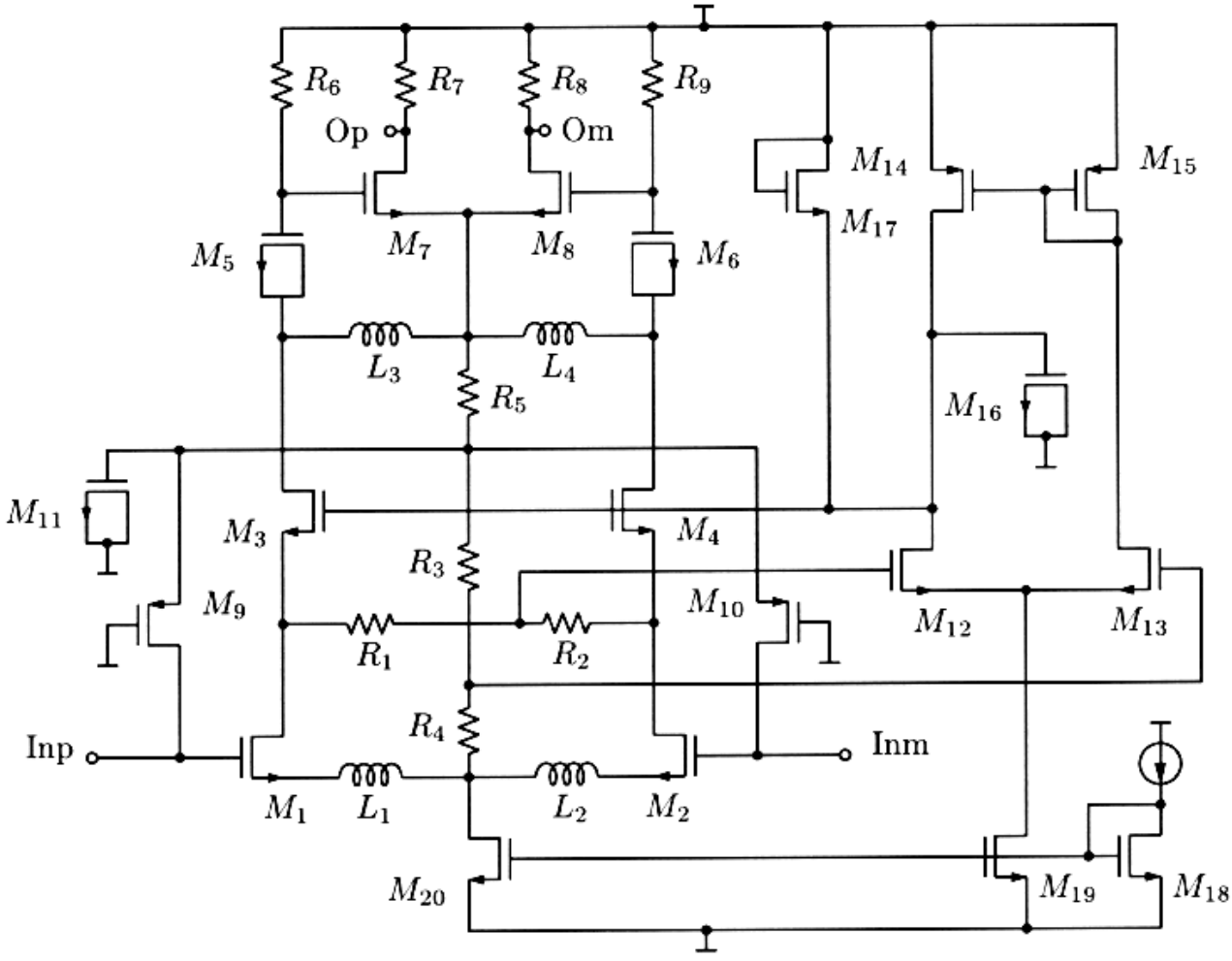
References:

[1] Shaeffer, D. K., T. H. Lee, "A 1.5V, 1.5GHz CMOS low noise amplifier," Symposium on VLSI Circuits Digest of Technical Papers, 1996, pp. 32-33.

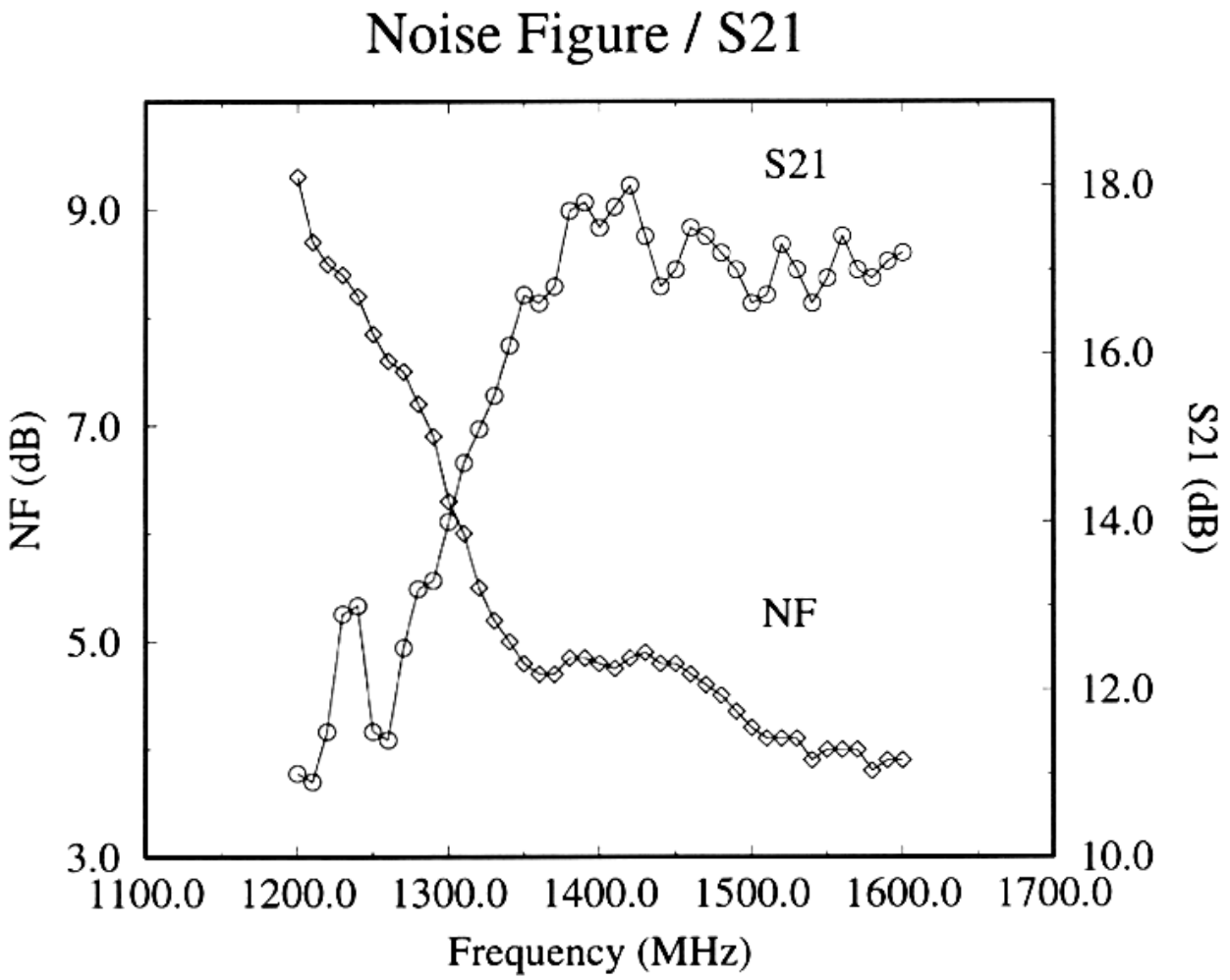
[2] van der Ziel, A., *Noise in Solid State Devices and Circuits*, John Wiley & Sons, New York, 1986.



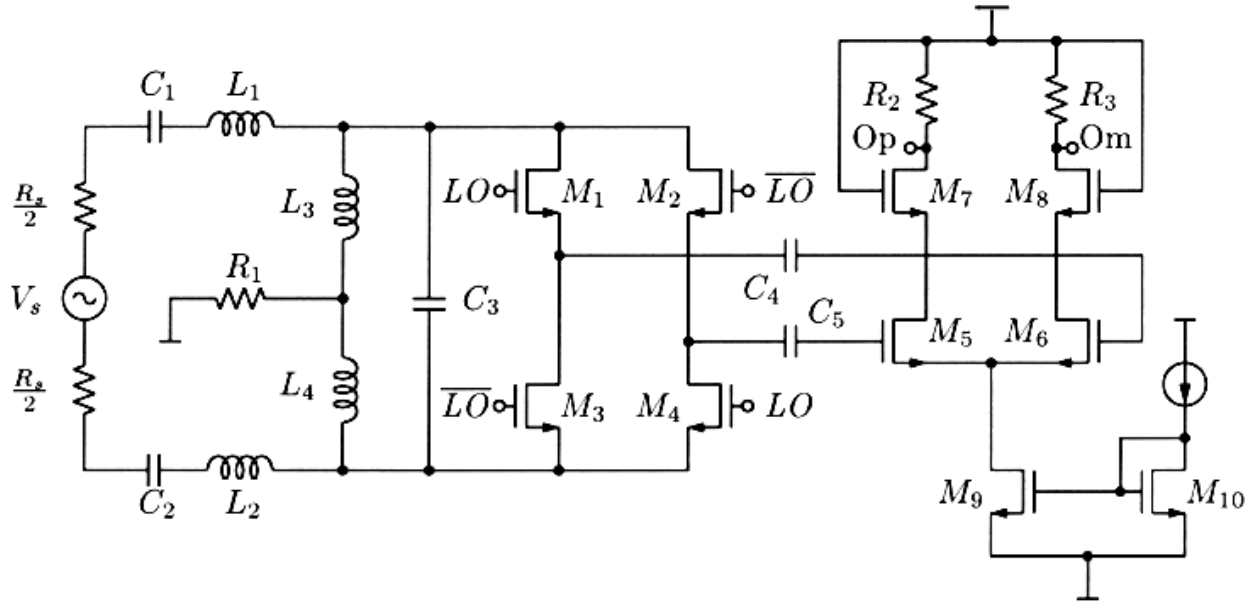
22-3-1: Block diagram of the GPS front-end test setup.



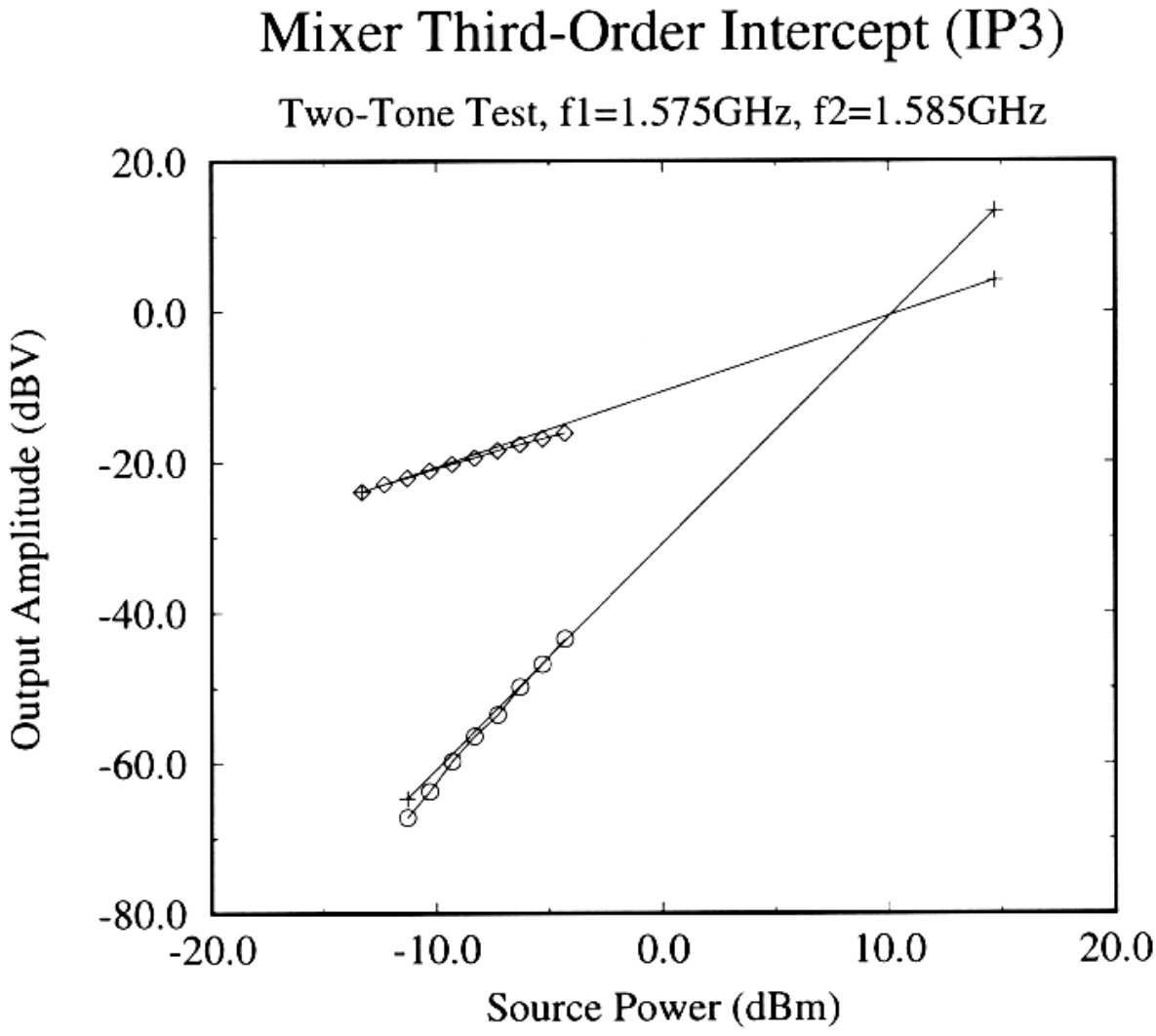
22-3-2: LNA circuit schematic.



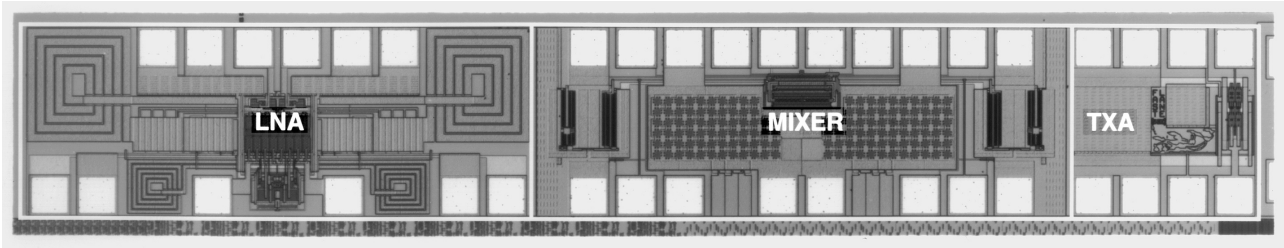
22-3-3: LNA forward gain (S21) and noise figure.



22-3-4: Schematic of mixer circuit with test buffer.



22-3-5: Mixer two-tone IP3 measurement.



22-3-6: Chip micrograph.

Low-noise amplifier	
Frequency	1.575GHz
Noise figure	3.8dB
S21	17.7dB
S12	≤ -52dB
IP3 (input)	-6dBm
1dB compression (input)	-20dBm
Power dissipation	12mW
Mixer	
LO frequency	1.4GHz
LO amplitude	300mV (≈3.5dBm in 100Ω)
Voltage conversion gain	-3.6dB
IP3 (input)	10dBm
1dB compression (input)	-5dBm
Noise figure (SSB)	10dB
Supply voltage	1.5V
Technology	0.35µm CMOS
Die area	0.84mm²

22-3-Table 1: GPS front-end performance summary.