SP 22.3: A 12mW Wide Dynamic Range GPS Receiver Front-End

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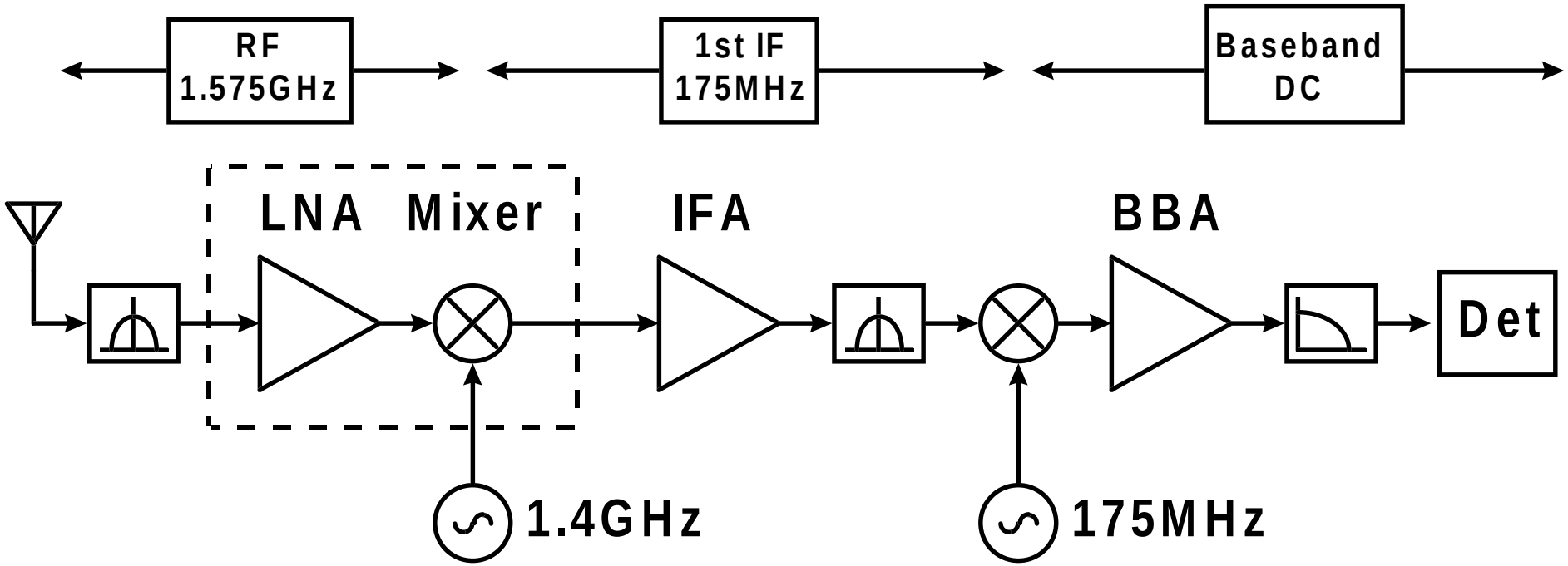
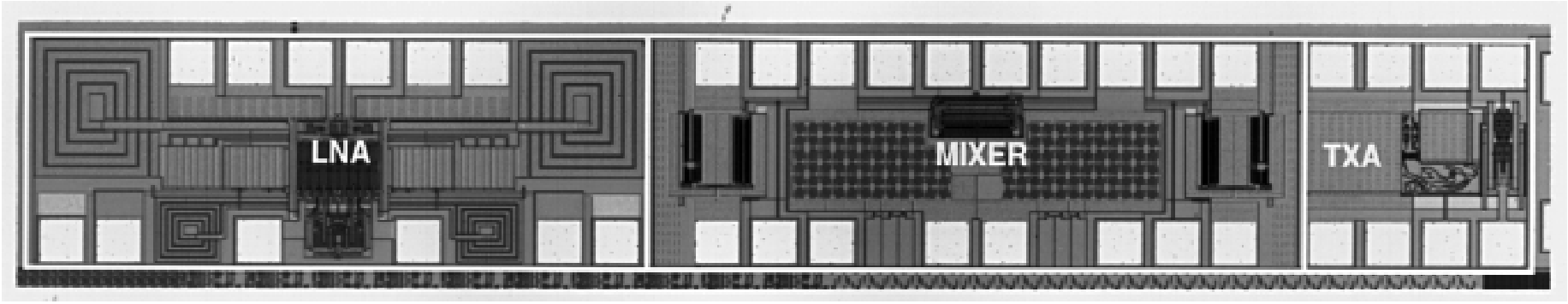
Typical GPS Receiver

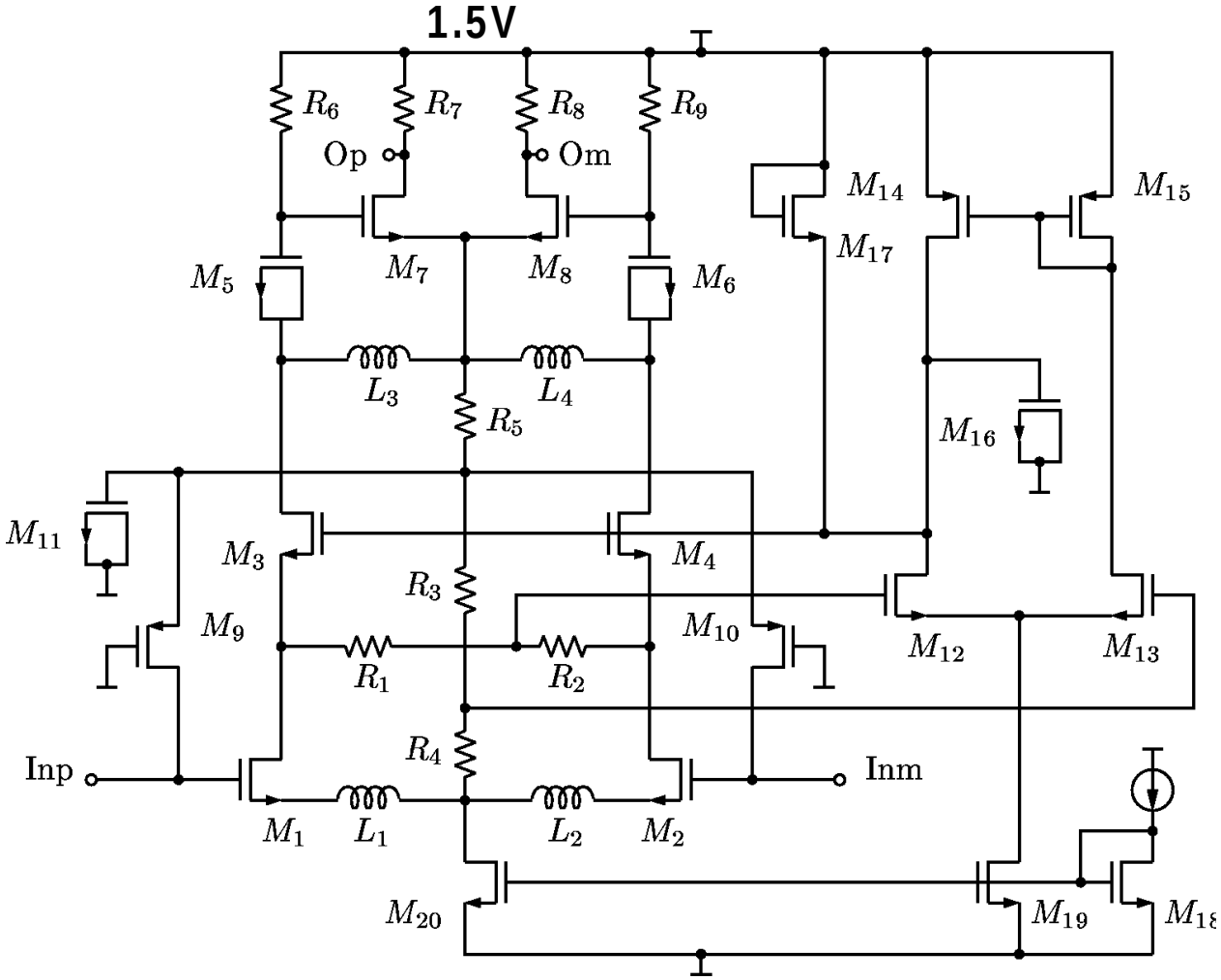


Die Photo

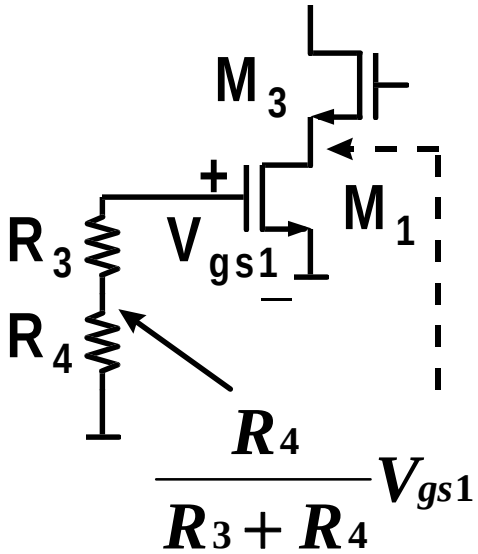


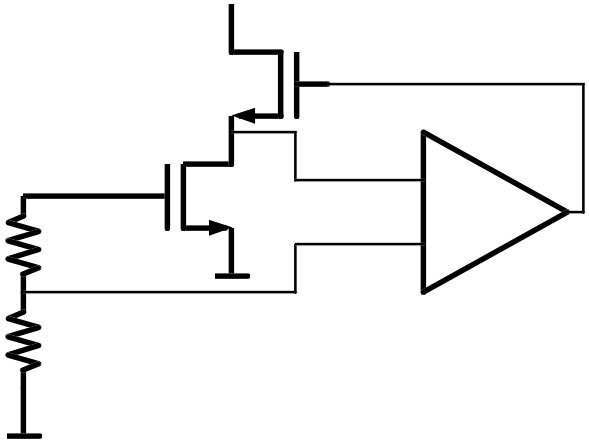
The LNA

LNA Schematic

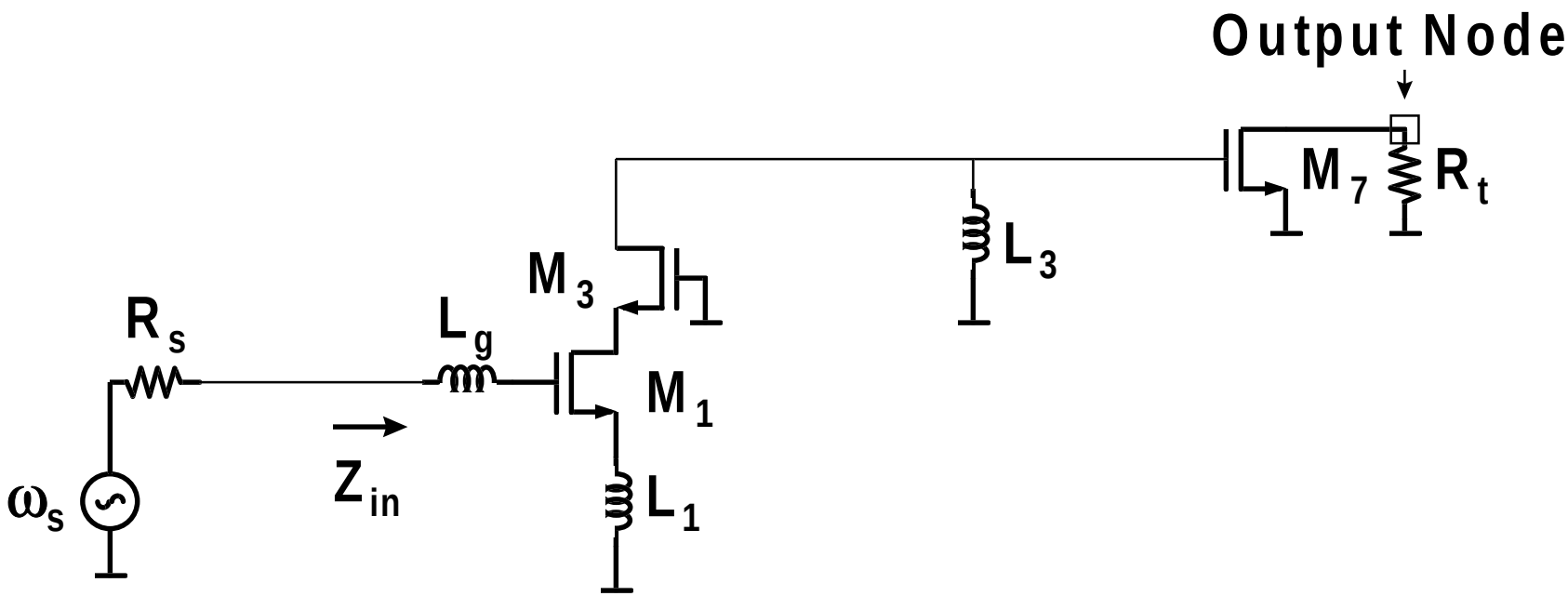


DC Biasing





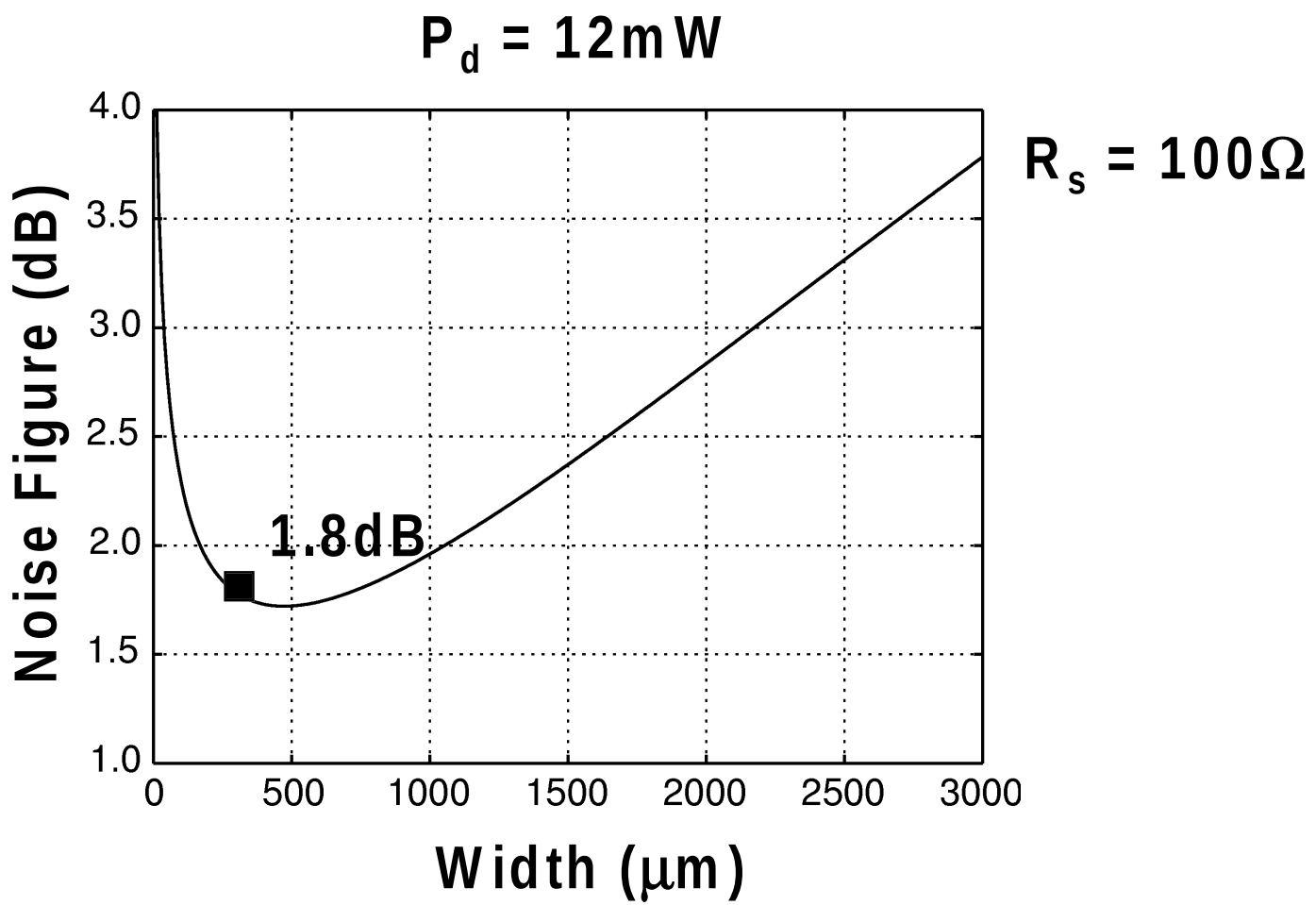
LNA Half-Circuit



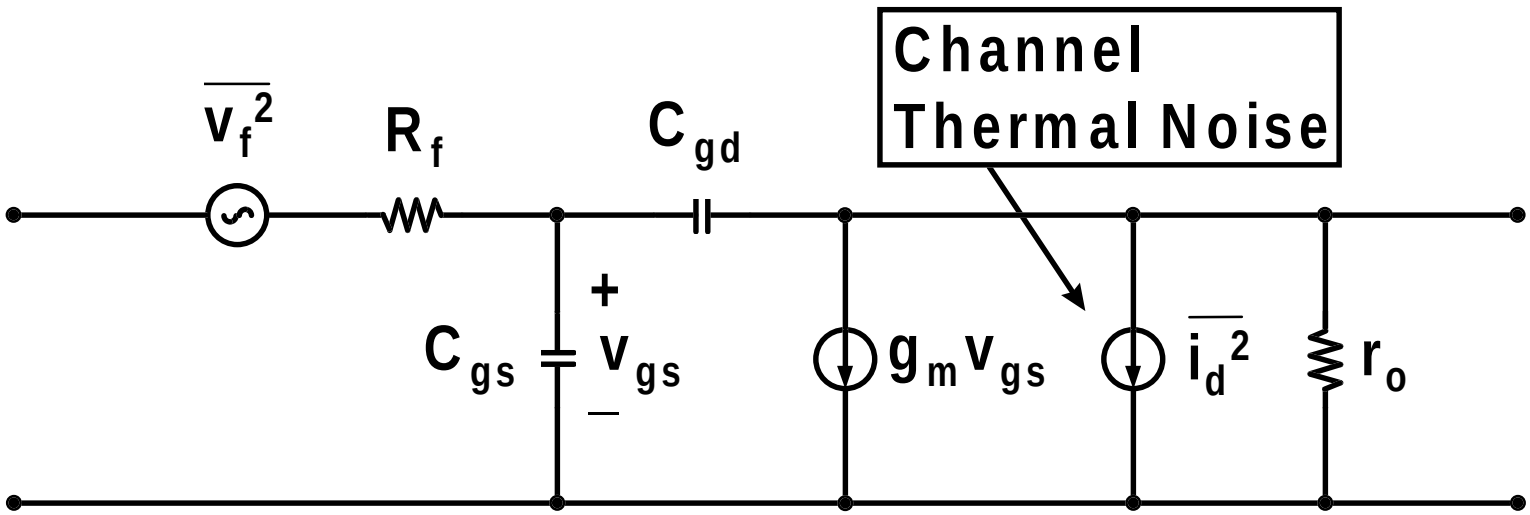
$$\mathrm{Re}\{Z_{in}\} = \left(\frac{g_{m1}}{C_{gs1}}\right) L_1 \approx \omega_T L_1$$

$$g_{m\,\text{input stage}} = \frac{1}{2\omega_s L_1}$$; for GPS ω_s = 10Grad/s

Minimum Noise Figure



Traditional CMOS Noise Model

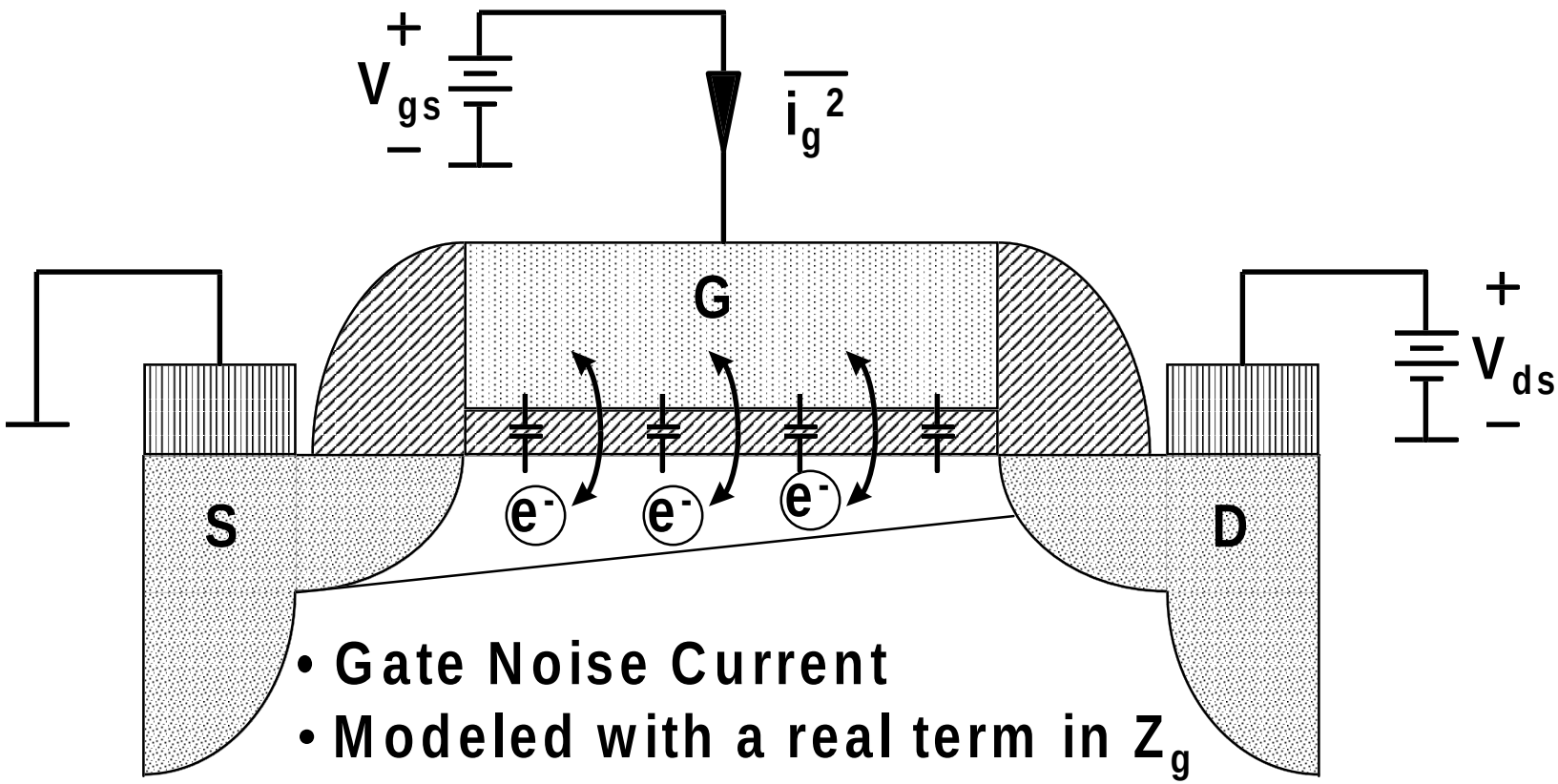


- Channel thermal noise is dominant

$$\overline{i_d^2} = 4kTB\gamma g_{d0}$$

- Gate resistance minimized by good layout

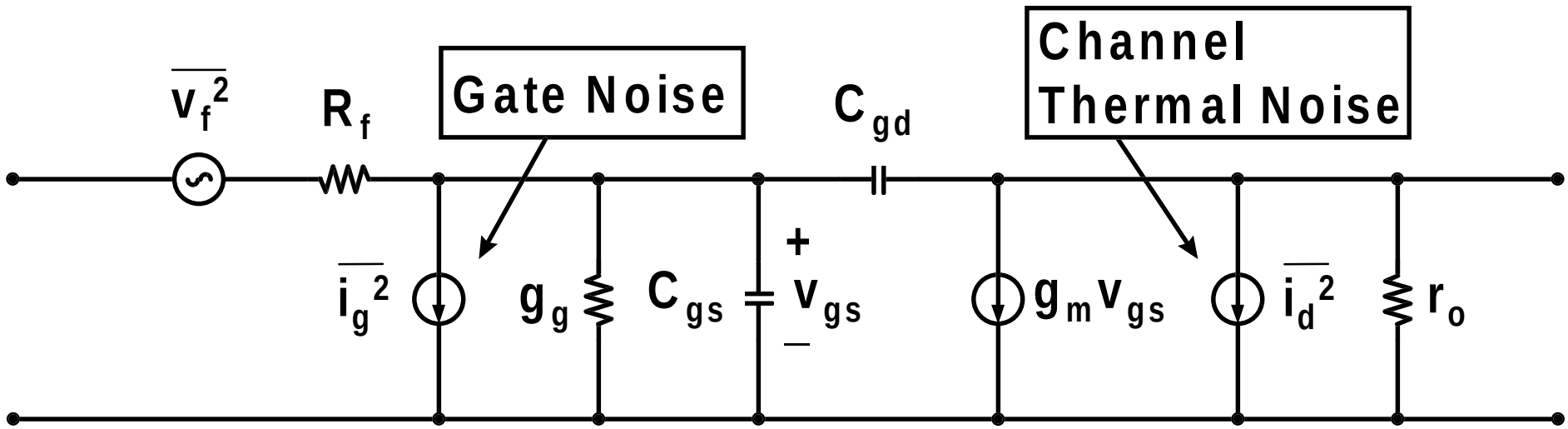
Induced Gate Effects



- Gate Noise Current
- Modeled with a real term in Z_g

[Aldert van der Ziel, *Noise in Solid State Devices and Circuits*, John Wiley & Sons, New York, 1986]

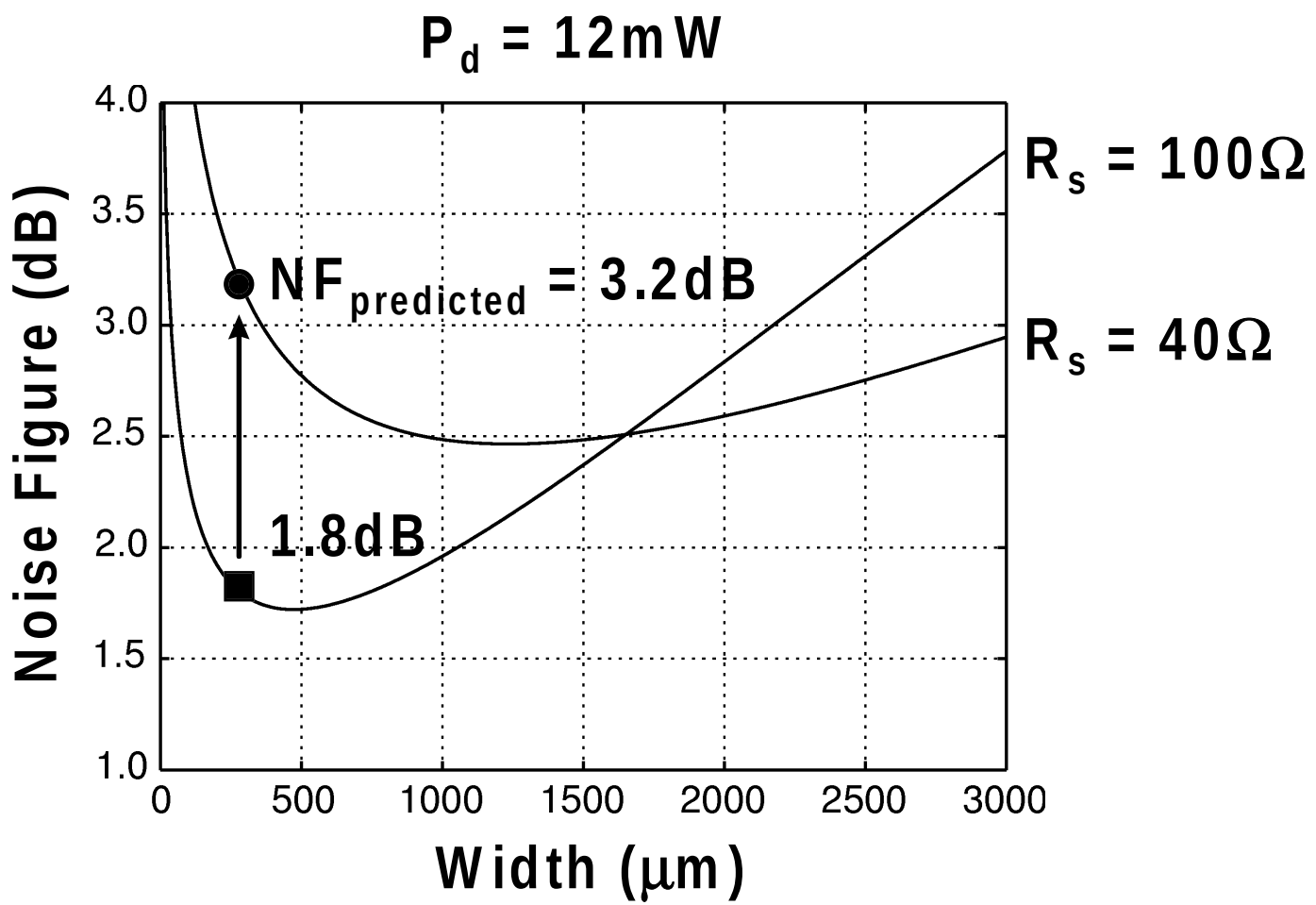
Augmented CMOS Noise Model



- $g_g = \dfrac{\omega^2 C_{gs}^2}{5 g_{d0}}$

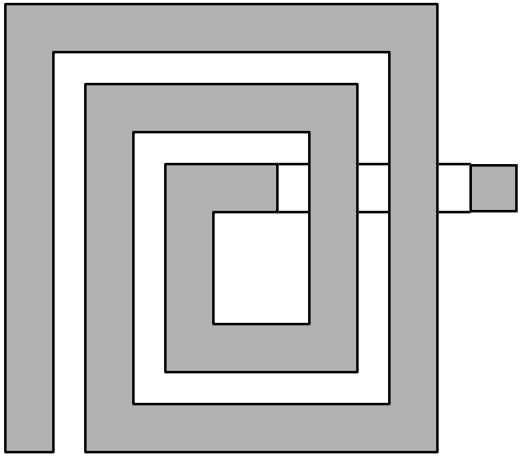
- Short channel effects are accounted for by δ ➡ $\overline{i_g^2} = 4kTB\delta g_g$

Minimum Noise Figure



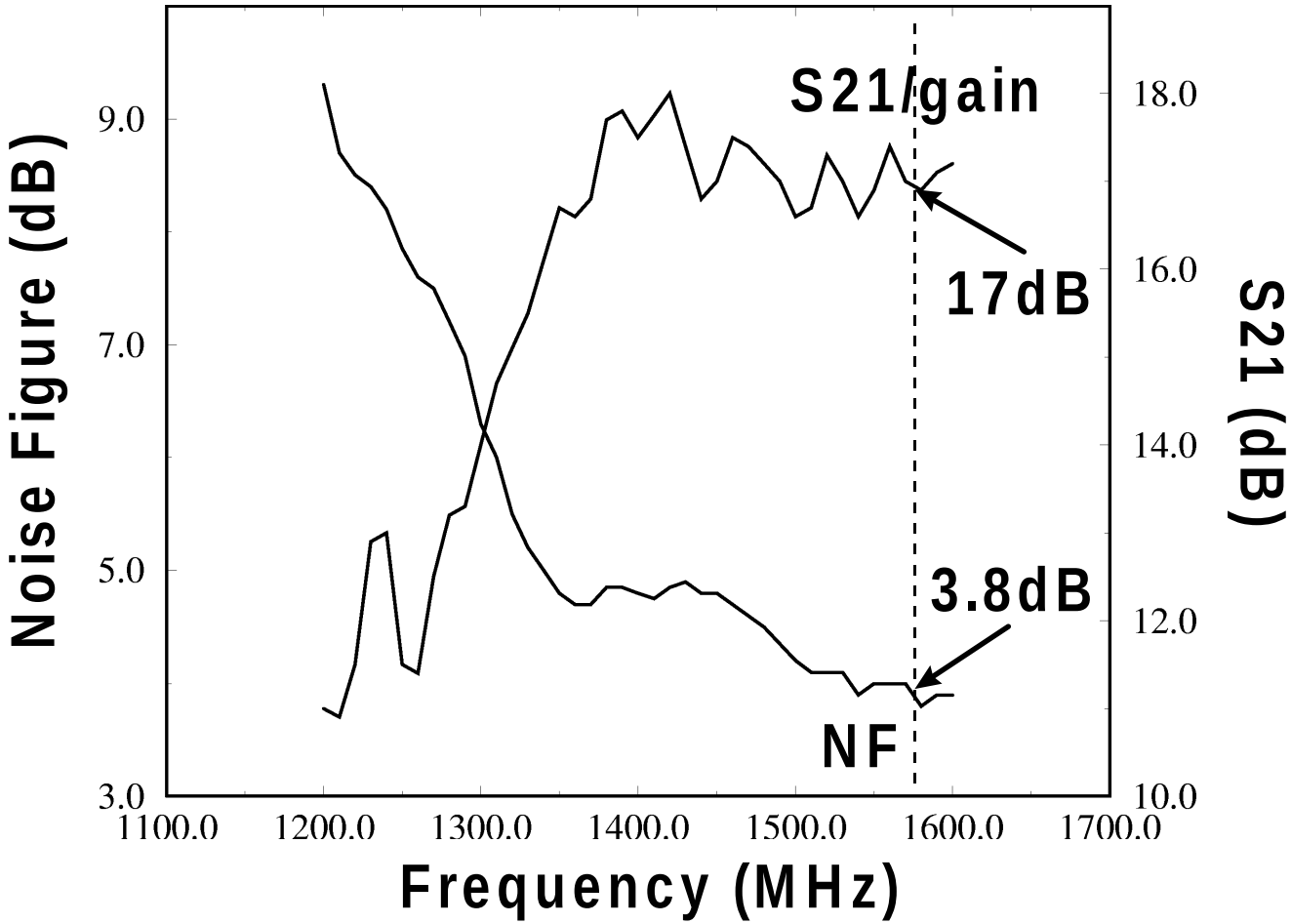
On-Chip Spiral Inductors

- **Constraints**
  - Only M1 / M2 available ➡ Low Q
    Low SRF
- **Bandages**
  - Strap M1 to M2 throughout
  - Segment substrate with n-well



* Want at least 3 metal layers!

LNA Measurement Results

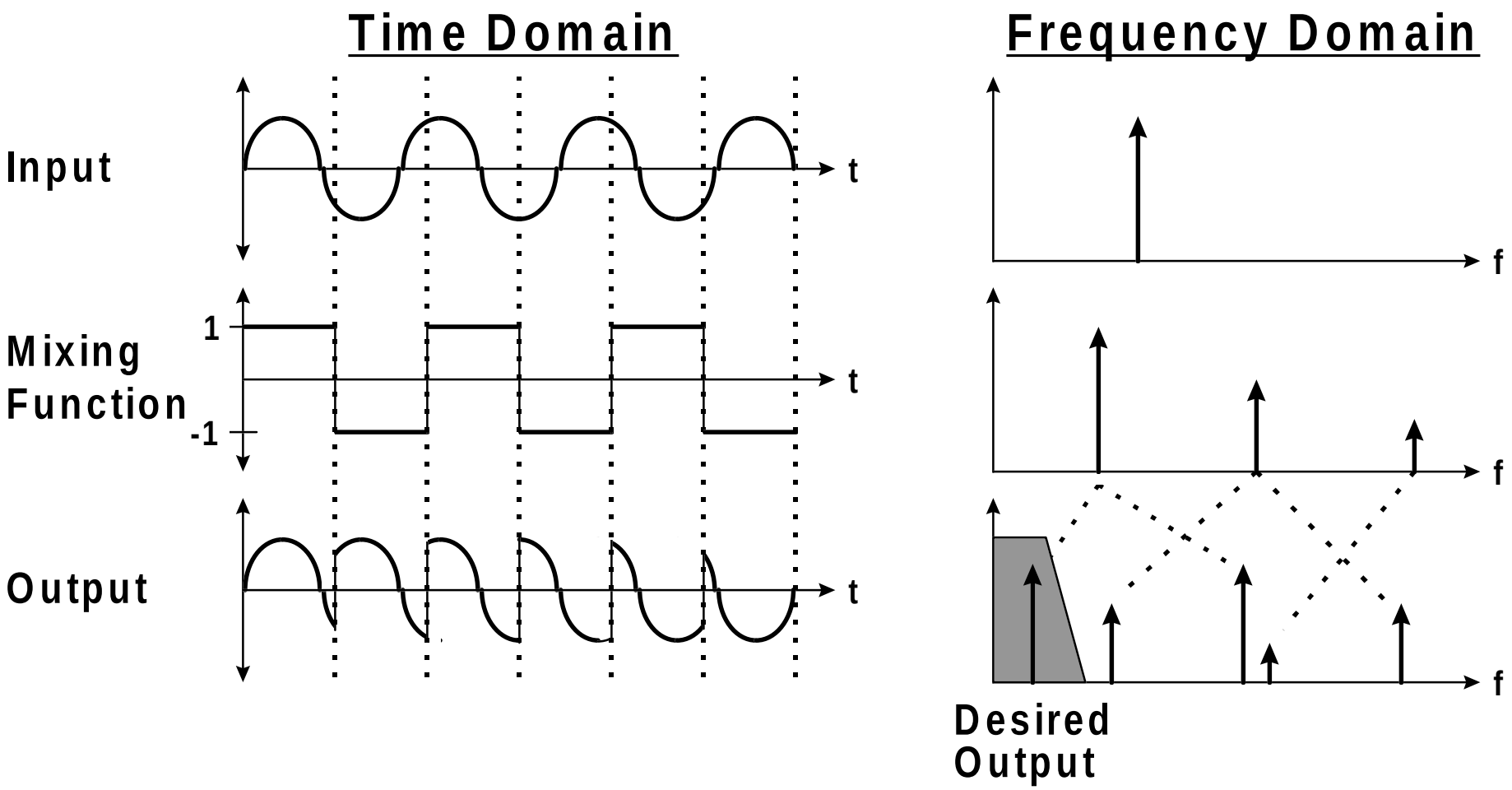


LNA Big Picture

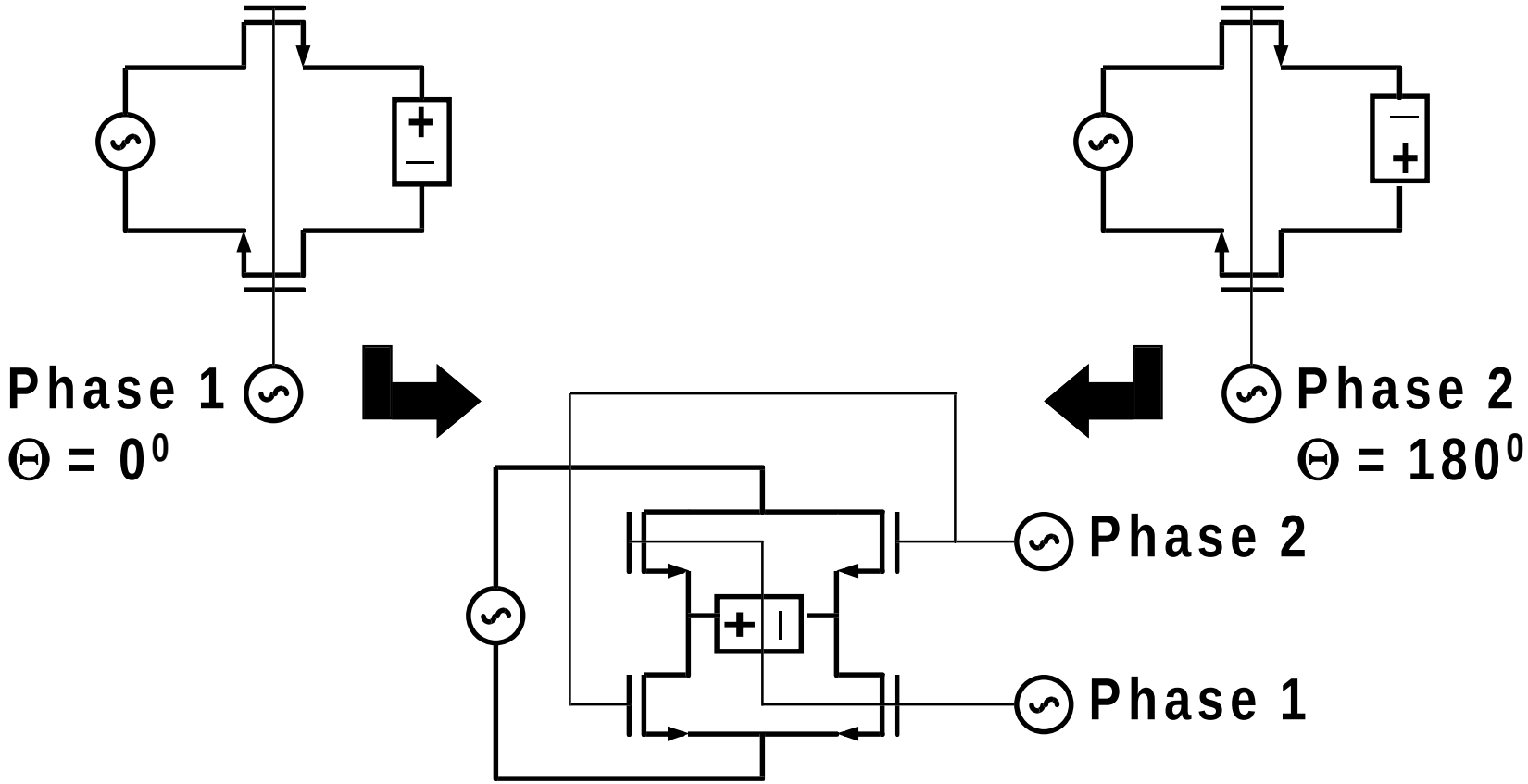
- Must include gate noise
- An optimum device exists for a fixed power dissipation in the inductively degenerated common source LNA
- Performance of CMOS LNA is satisfactory for a GPS receiver

The Mixer

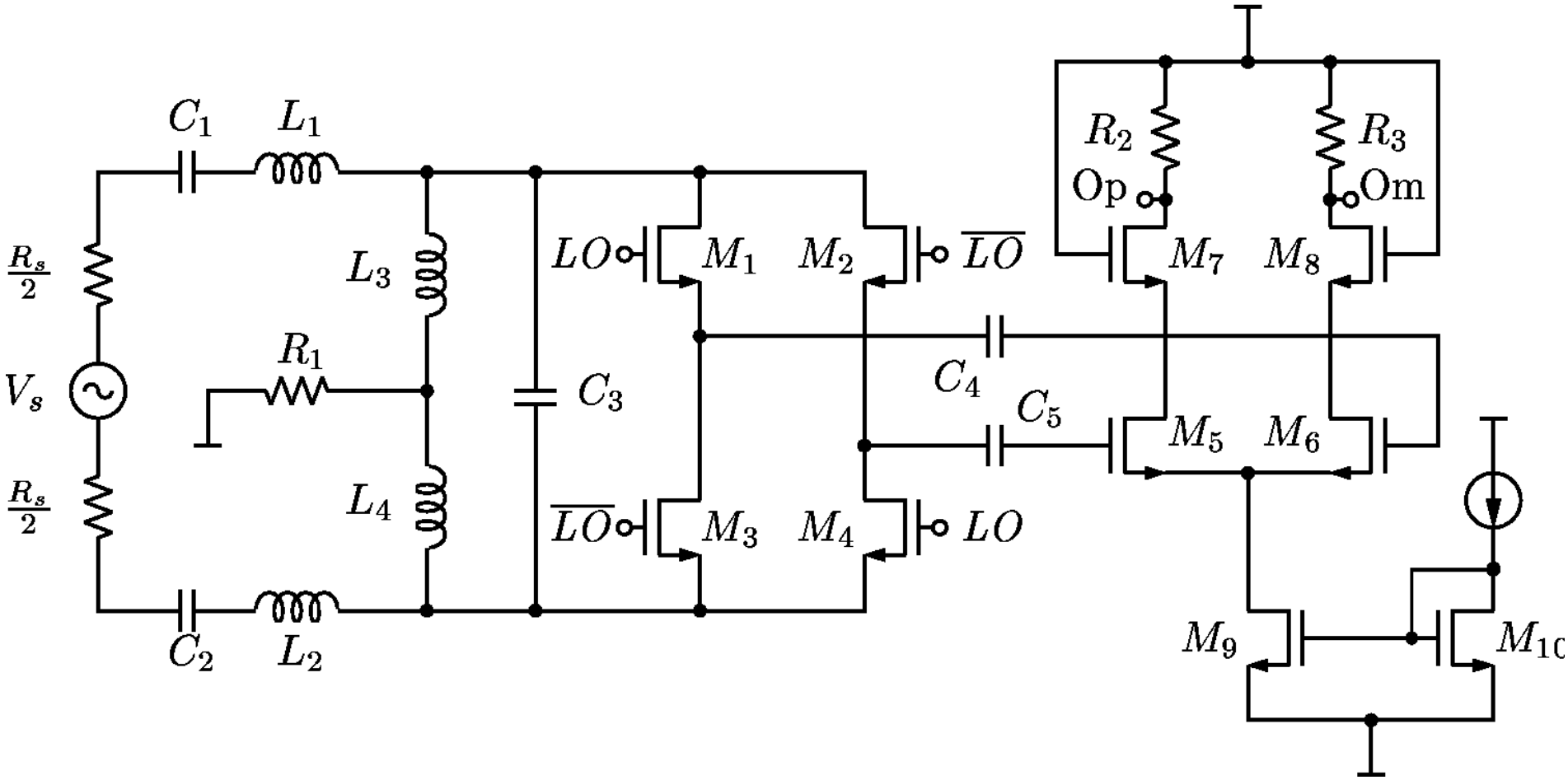
Principle of Operation



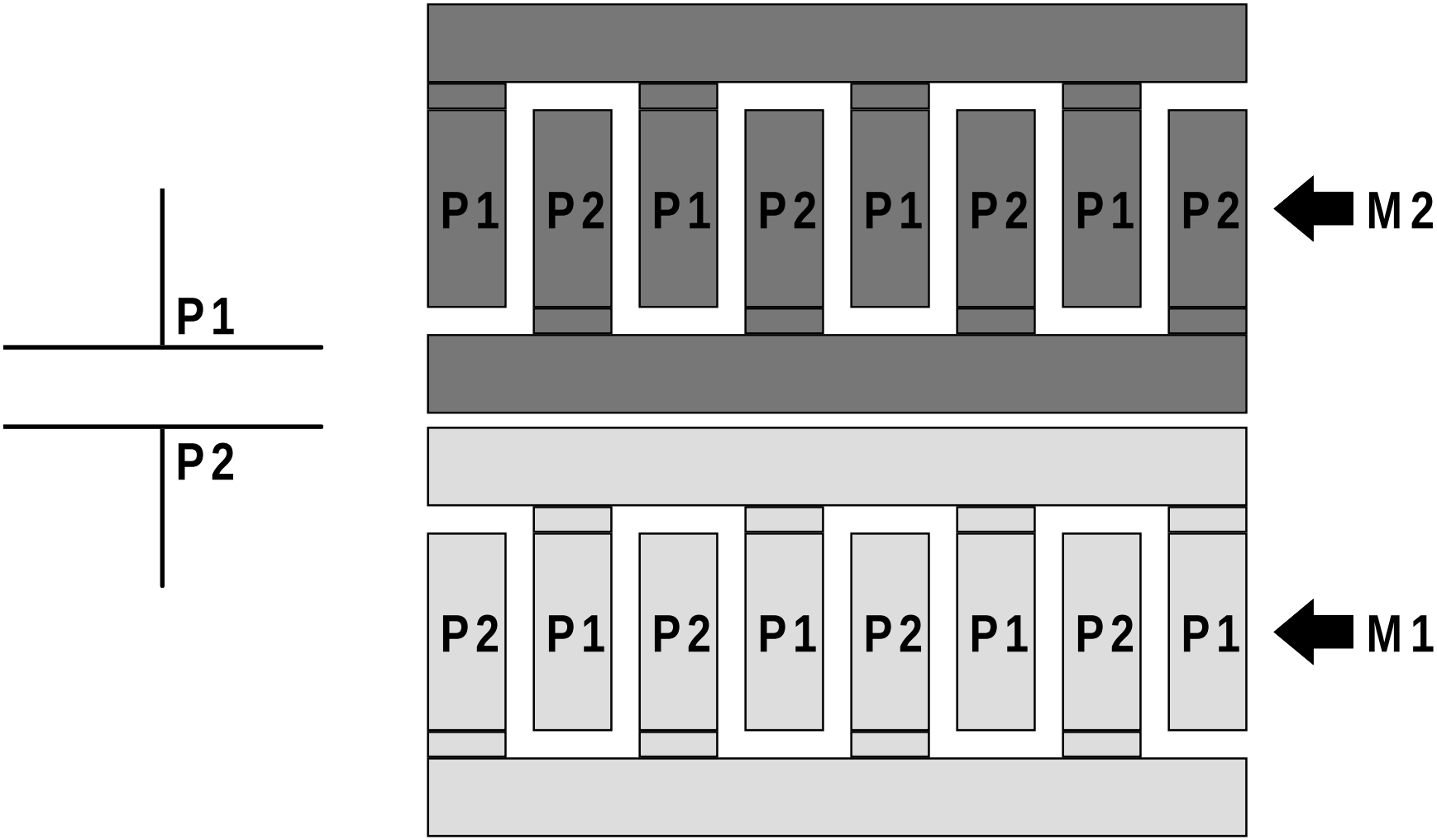
Transistor Switches



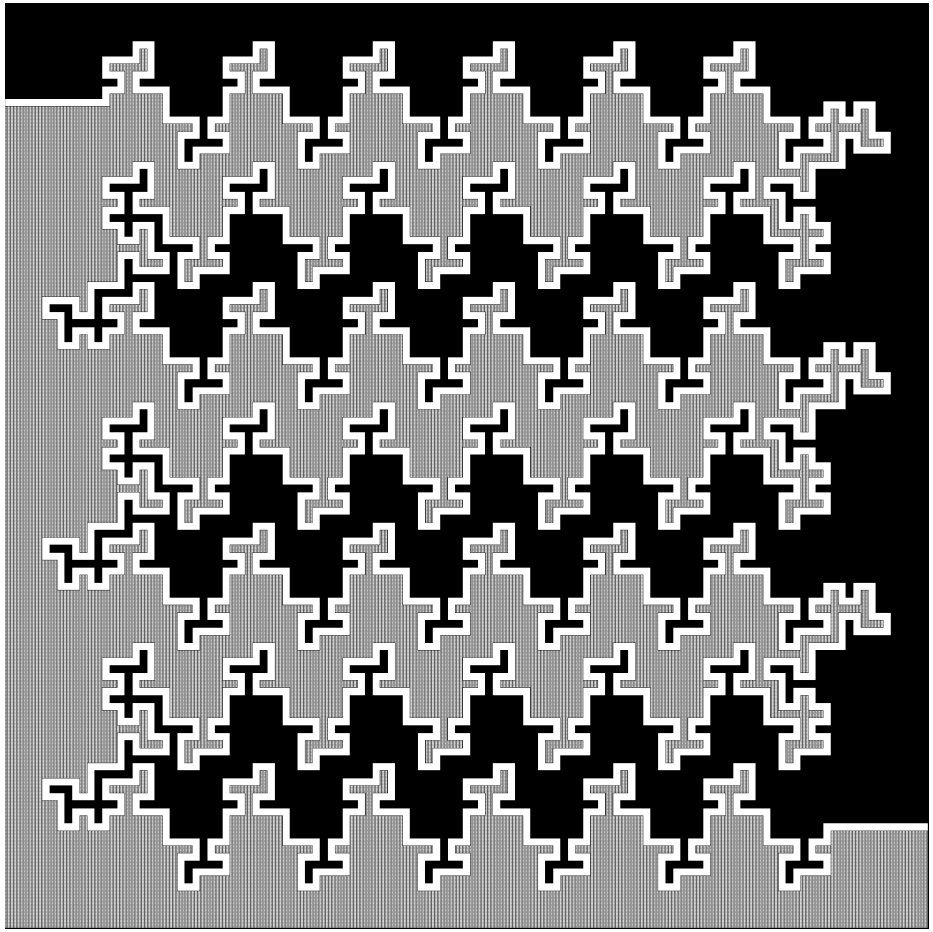
Mixer Schematic



Lateral-Flux Capacitor (LFC)



Fractal Capacitor



Simulated and Extracted C

- Parallel plate capacitance

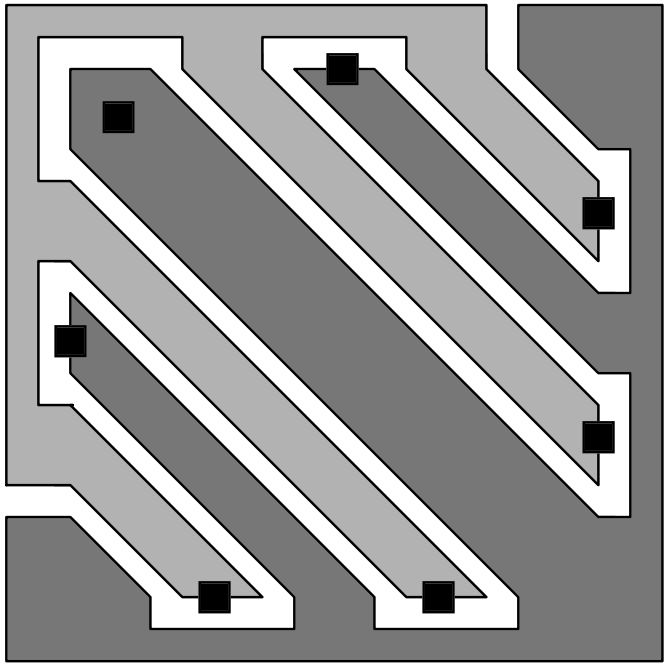
  $C_{PP} = 20fF$

- Maxwell simulation of unit cell

  $C_{P1/P2} = 37fF = 1.85*C_{PP}$

- Extraction of unit cell

  $C_{EX} = 45fF = 2.25*C_{PP}$



LFC Summary

- **Area efficient**

  (extracted different pattern which has $C_{P1/P2} = 5*C_{PP}$)

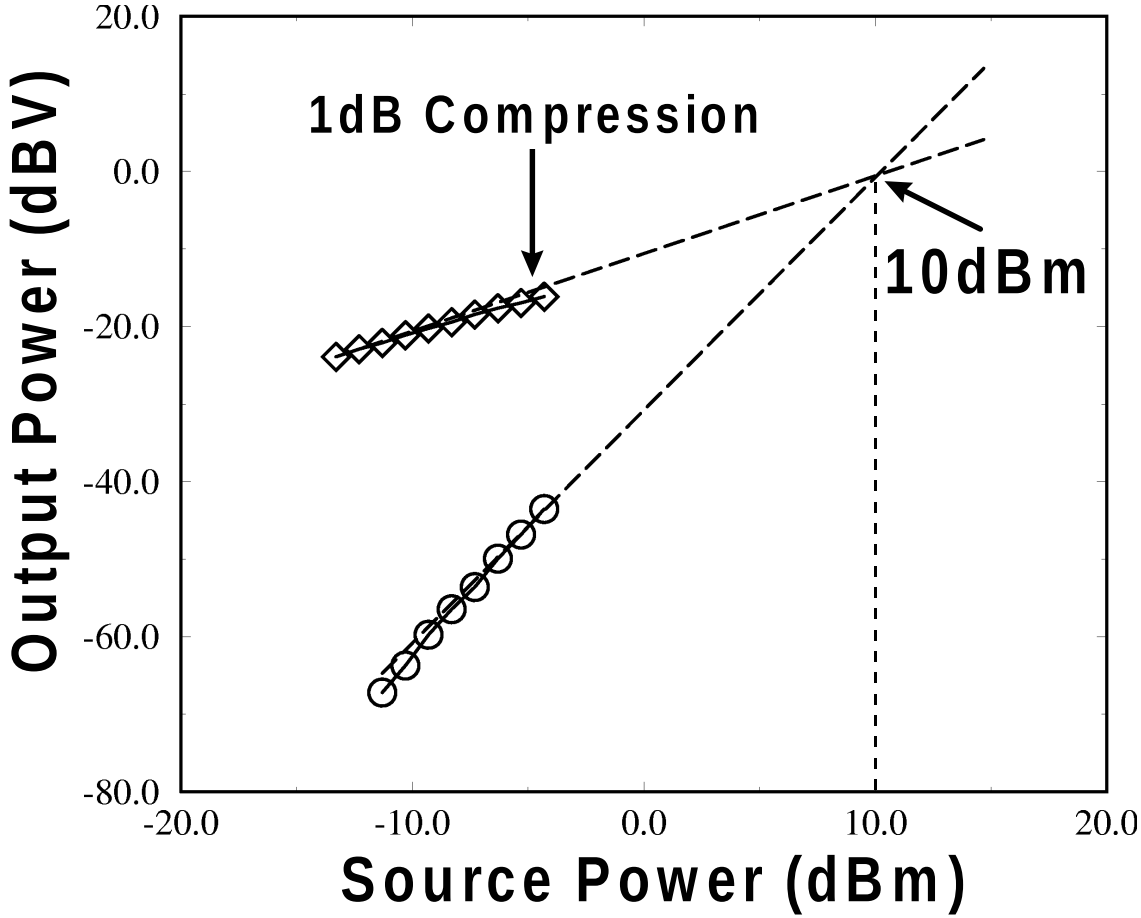
- **Linear**

  (metal to metal capacitor)

- **Matched top and bottom plate parasitic capacitance**

Mixer Measurement Results

f1 = 1.575GHz, f2 = 1.585GHz



G_V = -3.6dB

Mixer Big Picture

- Downconversion is achieved on very low power
- Excellent linearity allowing the LNA/mixer combination to have well matched dynamic ranges

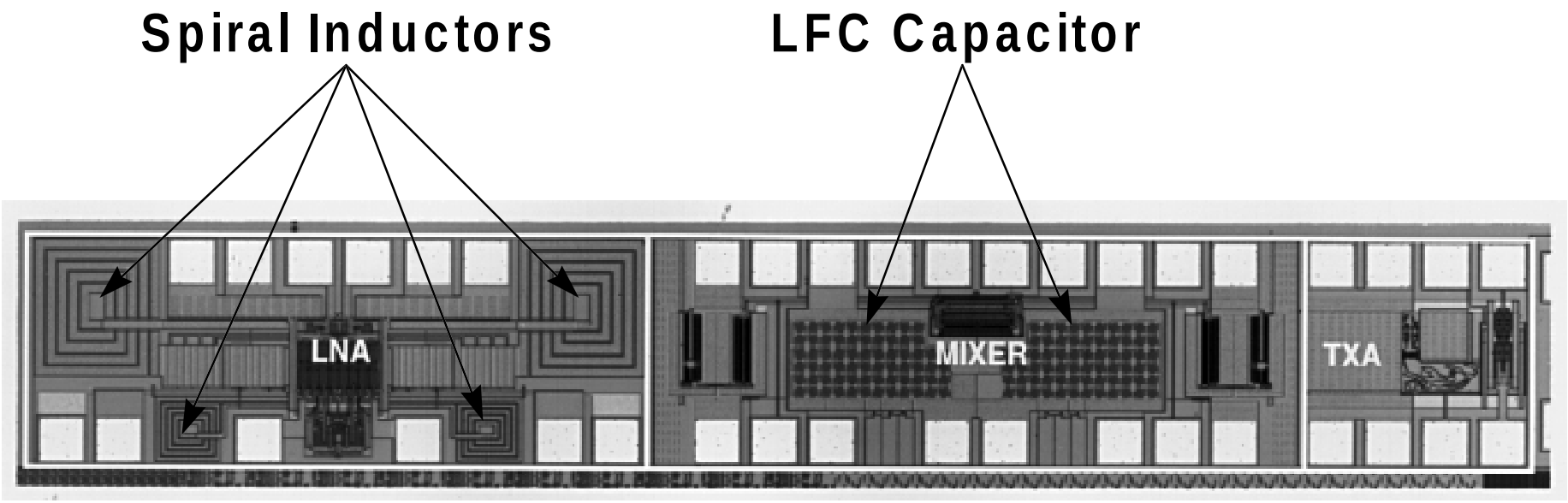
Performance Summary

Low-Noise Amplifier	
Frequency	1.575GHz
Noise Figure	3.8dB
S21	17dB
S12	< -52dB
IP3 (Input)	-6dBm
1dB Compression (Input)	-20dBm

Mixer	
LO Frequency	1.4GHz
LO Amplitude	300mV
Voltage Conversion Gain	-3.6dB
IP3 (Input)	10dBm
1dB Compression (Input)	-5dBm
Noise Figure (SSB)	~10dB

Power Dissipation	12mW
Supply Voltage	1.5V
Technology	0.35μm CMOS, 2-metal, 1-poly
Die Area	$0.84mm^2$

Die Photo



Conclusions

- Differential LNA exhibits significantly better reverse isolation compared to single-ended version (important for system integration)
- CMOS is viable for communications systems operating in the 1-3GHz range

Acknowledgements

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