SP 22.3: A 12mW Wide Dynamic Range GPS Receiver Front-End

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Typical GPS Receiver

RF 1.575GHz

LNA 1.4GHz

Mixer

IFA

BBA 175MHz

Baseband DC

Det
Die Photo
The LNA
LNA Schematic

1.5V

M1, M2, M3, M4, M5, M6, M7, M8, M9, M10, M11, M12, M13, M14, M15, M16, M17, M18, M19, M20

R1, R2, R3, R4, R5, R6, R7, R8, R9

L1, L2, L3, L4
DC Biasing

\[ R_3 + R_4 \]

\[ V_{gs1} \]

\[ M_1 \]

\[ M_3 \]
LNA Half-Circuit

\[ \text{Re}\{Z_{in}\} = \left( \frac{g_{m1}}{C_{gs1}} \right) L_1 \approx \omega t L_1 \]

\[ g_{m \text{ input stage}} = \frac{1}{2 \omega_s L_1} \text{; for GPS } \omega_s = 10 \text{Grad/s} \]
Minimum Noise Figure

$P_d = 12\text{mW}$

$R_s = 100\Omega$

Noise Figure (dB)

Width ($\mu$m)

1.8 dB
Traditional CMOS Noise Model

- Channel thermal noise is dominant
  \[ \overline{i_d^2} = 4kTB \gamma g_{d0} \]
- Gate resistance minimized by good layout
Induced Gate Effects

- Gate Noise Current
- Modeled with a real term in $Z_g$

Augmented CMOS Noise Model

\[ g_g = \frac{\omega^2 C_{gs}^2}{5 g_{d0}} \]

- **Short channel effects** are accounted for by \( \delta \rightarrow i_g^2 = 4kTB\delta g_g \)

\[ \begin{align*} v_f^2 & \quad R_f \\
\overline{i_g^2} & \quad g_g \quad C_{gs} \quad + \quad v_{gs} \quad g_m v_{gs} \quad \overline{i_d^2} \quad r_o \end{align*} \]
Minimum Noise Figure

\[ P_d = 12 \text{mW} \]

- \( R_s = 40 \Omega \)
- \( R_s = 100 \Omega \)

\( \text{NF}_{\text{predicted}} = 3.2 \text{dB} \)

\( 1.8 \text{dB} \)

\( \text{Width (\( \mu \text{m} \))} \)

\( \text{Noise Figure (dB)} \)
On-Chip Spiral Inductors

- **Constraints**
  - Only M1 / M2 available → Low Q
  - Low SRF

- **Bandages**
  - Strap M1 to M2 throughout
  - Segment substrate with n-well

* Want at least 3 metal layers!
LNA Measurement Results

<table>
<thead>
<tr>
<th>Frequency (MHz)</th>
<th>Noise Figure (dB)</th>
<th>S21/gain (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>3.8</td>
<td>17</td>
</tr>
</tbody>
</table>
LNA Big Picture

- Must include gate noise

- An optimum device exists for a fixed power dissipation in the inductively degenerated common source LNA

- Performance of CMOS LNA is satisfactory for a GPS receiver
The Mixer
Principle of Operation

**Time Domain**
- Input
- Mixing Function
- Output

**Frequency Domain**
- Desired Output

The diagram illustrates the relationship between the time domain and the frequency domain, showing how input signals are transformed through a mixing function to produce an output signal in the frequency domain.
Transistor Switches

Phase 1
Θ = 0°

Phase 2
Θ = 180°
Lateral-Flux Capacitor (LFC)
Fractal Capacitor
Simulated and Extracted C

- Parallel plate capacitance
  \[ C_{PP} = 20 \text{fF} \]
- Maxwell simulation of unit cell
  \[ C_{P1/P2} = 37 \text{fF} = 1.85 \times C_{PP} \]
- Extraction of unit cell
  \[ C_{EX} = 45 \text{fF} = 2.25 \times C_{PP} \]
LFC Summary

• Area efficient
  (extracted different pattern which has \( C_{P1/P2} = 5*C_{PP} \))

• Linear
  (metal to metal capacitor)

• Matched top and bottom plate parasitic capacitance
Mixer Measurement Results

\[ f_1 = 1.575\text{GHz}, \quad f_2 = 1.585\text{GHz} \]

\[ G_V = -3.6\text{dB} \]

1dB Compression

10dBm

Source Power (dBm)

Output Power (dBV)
Mixer Big Picture

• Downconversion is achieved on very low power

• Excellent linearity allowing the LNA/mixer combination to have well matched dynamic ranges
# Performance Summary

<table>
<thead>
<tr>
<th><strong>Low-Noise Amplifier</strong></th>
<th><strong>Mixer</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency</td>
<td>1.575GHz</td>
</tr>
<tr>
<td>Noise Figure</td>
<td>3.8dB</td>
</tr>
<tr>
<td>S21</td>
<td>17dB</td>
</tr>
<tr>
<td>S12</td>
<td>&lt; -52dB</td>
</tr>
<tr>
<td>IP3 (Input)</td>
<td>-6dBm</td>
</tr>
<tr>
<td>1dB Compression (Input)</td>
<td>-20dBm</td>
</tr>
<tr>
<td>LO Frequency</td>
<td>1.4GHz</td>
</tr>
<tr>
<td>LO Amplitude</td>
<td>300mV</td>
</tr>
<tr>
<td>Voltage Conversion Gain</td>
<td>-3.6dB</td>
</tr>
<tr>
<td>IP3 (Input)</td>
<td>10dBm</td>
</tr>
<tr>
<td>1dB Compression (Input)</td>
<td>-5dBm</td>
</tr>
<tr>
<td>Noise Figure (SSB)</td>
<td>~10dB</td>
</tr>
</tbody>
</table>

- Power Dissipation: 12mW
- Supply Voltage: 1.5V
- Technology: 0.35µm CMOS, 2-metal, 1-poly
- Die Area: 0.84mm$^2$
Die Photo

Spiral Inductors

LFC Capacitor

LNA

MIXER

TXA
Conclusions

- Differential LNA exhibits significantly better reverse isolation compared to single-ended version (important for system integration)

- CMOS is viable for communications systems operating in the 1-3GHz range
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