16.6: Fractal Capacitors

Hirad Samavati, Ali Hajimiri, Arvin Shahani, Gitty Nasserbakht[1], Thomas Lee

Stanford University, Stanford, CA
[1]Texas Instruments, Dallas, TX

This paper introduces a high-density linear capacitor structure with low bottom-plate parasitics. The density of such a structure improves as process technologies scale.

The metal-to-metal and metal-to-poly capacitors that have the highest linearity and quality factor, *Q*, have the lowest capacitance per unit area in comparison with other types such as MOS and junction capacitors. This usually limits their applications due to the large cost overhead imposed by the excess area used. The vertical spacing and the thickness of metal layers do not scale proportionally as the minimum horizontal spacing between metal lines in modern scaled technologies. This is a disadvantage for parallel plate capacitors since they will consume a larger percentage of the die area. In addition, these capacitors suffer from a large bottom-plate capacitance, due to their large area.

The continued scaling of process technologies can be exploited to achieve higher capacitance per area by using lateral fringing fields [1]. The amount of increase in capacitance, due to the lateral fringing, is proportional to the periphery. Therefore a structure with larger periphery per unit area is desirable.

Ideal fractals demonstrate infinite periphery with finite area [2]. An image of such a structure with limited resolution is shown in Figure 1. Although lithography limitations prevent fabricating a real fractal, one can use quasi-fractal structures with minimum dimensions limited by lithography. These structures have a very long periphery and therefore result in large capacitances for the given area. One can further augment the capacitance by using cross-coupled multiple metal layers to exploit both vertical and lateral fields as shown in Figure 2. Depending on the vertical spacing of metal layers and density of the fractal used, electromagnetic field-solver simulations show up to 6 times larger capacitance per area at horizontal metal spacing of 0.5µm. This boost factor increases as the technology scales, unlike conventional parallel-plate structures.

Fractal capacitors retain the linearity of metal-to-metal capacitors with limited degradation of *Q*. The structures automatically limit the length of the thin metal sections to a few microns, keeping the series resistance reasonably small. Another advantage is the reduction of bottom-plate capacitance because of the smaller area. In addition, some of the field lines terminate on the adjacent plate instead of the substrate which implies further reduction of bottom-plate capacitance as shown in Figure 2. Furthermore, the pseudo-random nature of the structure can also reduce any systematic offset due to misalignment during the lithography process. Finally, lateral flux capacitors shift the burden of repeatability and accuracy away from oxide thickness to lithography.

One problem in the usage of fractal structures is their generation and predictability. A program called Layout Generator for Fractal Capacitors (LGFC) was written which uses the technology file and a fractal library to generate customized layout of fractal capacitors. LGFC also generates the three-dimensional description of the fractal structures in various field-solver formats (*e.g.* Maxwell [2]). This allows accurate design of capacitors with desired values. An example of a layout generated by LGFC is shown in Figure 3.

To demonstrate its feasibility and verify some of its characteristics, a fractal capacitor was implemented in a five-metal layer process. This fractal is based on a family of fractals known as Koch Islands [3] and is shown in Figure 4. Although this structure may not be the most efficient choice, the overall improvement over a standard parallel plate capacitor with the same metal area is a factor of 2.3. In each metal layer, there is an inner and an outer conductor and a fractal border. The lateral metal spacing is 0.6µm and the vertical spacing is 0.8µm. There are four cross-coupled metal layers. The fifth metal layer is solely used to make connections to the capacitor terminals. The need for an additional metal layer to make contacts to capacitor terminals is not an inherent characteristic of fractal structures and is only a property of this particular fractal.

The results of high-frequency two-port network measurements are shown in Figure 5, which depicts the magnitude of Y_{12} as a function of frequency. It also shows the equivalent RLC model together with the best-fit parameters. The structure exhibits a self-resonant frequency of 3.7GHz. Field solver simulations predict a capacitance of 5.4pF compared to the mean measured value of 5.5pF. The series inductance of the lines connecting the pads to the capacitor terminals is simulated to be 0.3nH, which accounts for 90% of the measured series inductance. About 80% of the series resistance can be attributed to vias and connecting stubs. Since both r_s and L_s are dominated by non-fundamental mechanisms, *Q* and the self-resonance frequency can be significantly improved.

The above measurements were repeated for 15 sites across an 8-inch wafer and the results are shown in Figure 6. The distribution has a mean value of 5.5pF and a standard deviation of 83fF. It is noteworthy that the five points with the value of 5.4pF in the histogram correspond to the central sites which show a much smaller standard deviation of 9.4fF. These five sites are spread over an area of 60x60 mm^2, yet the mismatch is less than 0.2%. The capacitance increases with distance from the center of the wafer which suggests the mismatch is mostly due to systematic variations in oxide thickness across the wafer.

Acknowledgments:

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References:

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2. Ansoft Corporation, *Maxwell 3D Parameter Extractor*, 1997.

3. B. B. Mandelbrot, *The Fractal Geometry of Natur*e, W. H. Freeman, New York 1983.

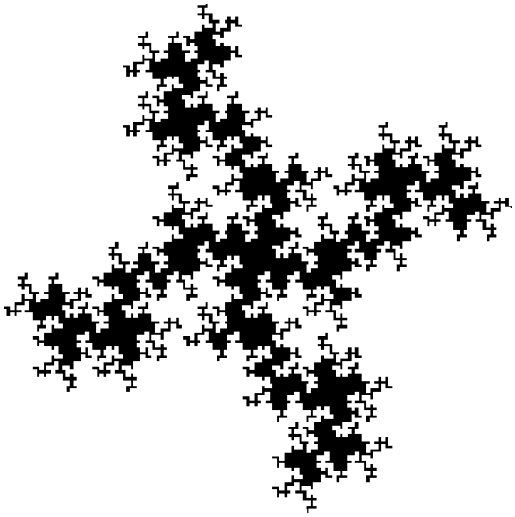

Figure 1: A fractal structure.

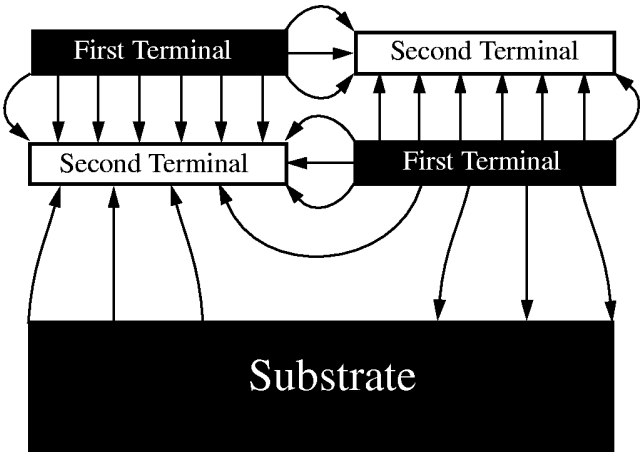

Figure 2: Simplified cross-sectional view.

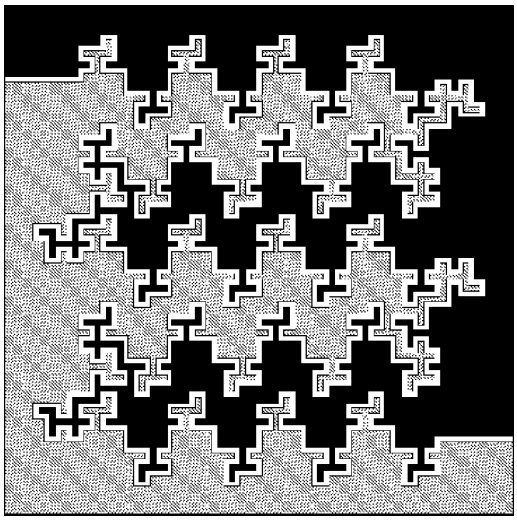

Figure 3: Layout generated by LGFC.

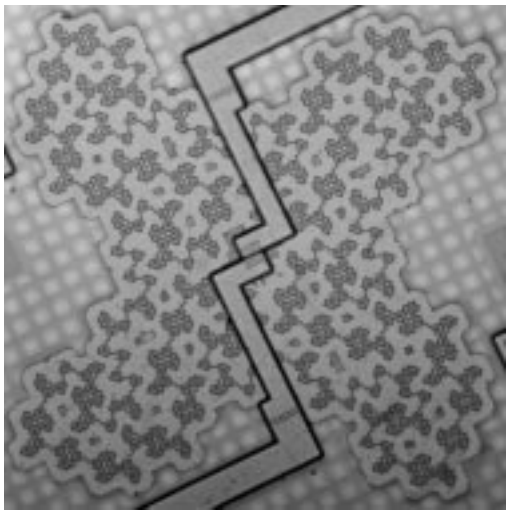

Figure 4: Die photo of the fractal capacitor.

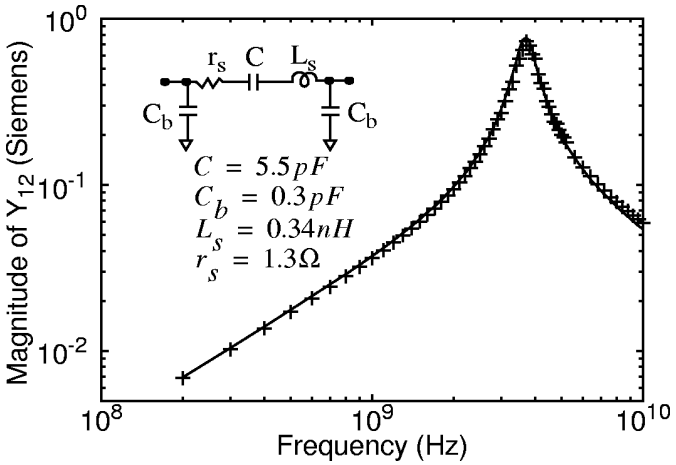

Figure 5: Two-port measurements.

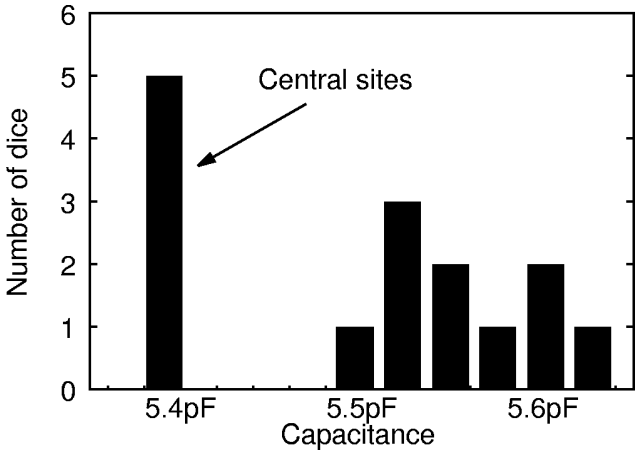

Figure 6: Capacitance distribution across the wafer.