

FA 8.1: A 115mW CMOS GPS Receiver

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The Global Positioning System (GPS) provides accurate positioning and timing information that is useful in many applications. In particular, portable consumer GPS applications require cheap compact low-power receivers. This 115mW receiver, implemented in an analog $0.5\mu\text{m}$ CMOS technology, comprises the entire radio frequency (RF) and analog sections in addition to the local oscillator (LO) frequency synthesizer and a pair of oversampled A/D converters.

The GPS L_1 band is a 20MHz allocation centered at 1.57542GHz. This band contains two direct-sequence spread spectrum signals: the C/A code (or coarse acquisition code) and the P code (or precision code). The C/A code is intended for civilian use, and its main lobe occupies 2MHz at the center of the band. The main lobe of the P code occupies the full 20MHz and is intended for military use. The receiver translates the L_1 band to a low intermediate frequency of 2MHz and uses a 3MHz lowpass filter to eliminate any out-of-band interference while passing the desired C/A code main lobe. As illustrated in Figure 1, if the only concern is with the main lobe of the C/A code, the channel has, in essence, a built-in guard band extending for 5MHz above the main lobe, implying a relatively low order channel filter. I and Q channels enable subsequent rejection of the image signal, that consists primarily of noise and thus requires only modest rejection.

A block diagram of the receiver is shown in Figure 2. The signal path is fully differential and includes a low-noise amplifier (LNA), passive double-balanced mixers, IF amplifiers, active filters and 1-bit oversampled A/D converters. The receiver also incorporates a phase locked loop (PLL) to generate the LO, as well as the necessary drivers to operate the mixers. The LNA and mixer employ previously-reported architectures [1]. In this implementation, the LNA possesses a 2.4dB noise figure on 15mW of power consumption, including biasing.

The on-chip G_m - C channel filter is a 5th-order elliptical filter, based on an L - C ladder prototype. Due to well-known dynamic range limitations of active filters, the gyrator transconductor must be power-efficient and linear. A suitable solution is shown in Figure 3, consisting of a pair of square-law, class-AB half-transconductors. A voltage buffer formed by M2 and M5-M6 places the input voltage across device M1. To the extent that M1 is a square-law device, the I-V characteristic of the transconductor is *linear* due to cancellation of even-order distortion products in the differential output. Two effects limit the quality of this approximation: velocity saturation due to high lateral fields, and vertical field mobility degradation. The first is mitigated through the use of longer channel lengths. The second is counteracted by using a small amount of positive feedback, via M10, to increase the curvature of the I-V characteristic of the half-transconductor, causing it to approximate a square-law curve more closely. This technique is power efficient because it linearizes the transconductor without the need for increased power consumption. The filter requires eight such transconductors and consumes 9.7mW. For

simplicity, a replica bias circuit tunes the filter. The resulting variation in cutoff frequency is accommodated by oversampling in the subsequent A/D converter.

As shown in Figure 2, the receiver also incorporates a PLL for LO synthesis. One of the largest power consuming blocks in a PLL is typically the divide-by- N prescaler. The present PLL architecture eliminates this block by using an aperture phase detector (APD) that measures the LO phase during a window positioned around a low-to-high transition of the reference clock. This architecture potentially consumes less power because the APD switches only at the reference rate rather than the higher LO rate. With a single APD, the loop can lock to any harmonic of the reference input that falls within the VCO tuning range. This undesirable behavior is eliminated by two mutually-prime references ($N*f_0$ and $M*f_0$, where N and M are mutually-prime numbers), forcing the loop to lock at a harmonic of *both* references ($N*M*f_0$).

A schematic of the APD is shown in Figure 4. The reference input is used as the precharge clock for the two precharged inverters, with a delayed version serving as the PLL reference. As a result, the precharge clock is de-asserted slightly before the delayed reference edge arrives, thus defining the beginning of the aperture. To reduce the aperture uncertainty, fast falling edge (FFE) circuits drive the precharge transistors. The LO input is AC-coupled to the signal input of the top inverter, which is biased just above threshold for more accurate sensing of the first LO falling edge after the start of the aperture. The resulting up and down signals drive the charge pump directly, making this a proportional phase detector.

Proper chip layout can mitigate potential sources of interference in the receiver. Strict differential symmetry in the signal path rejects common-mode noise, and patterned ground shields beneath all sixteen spiral inductors reduce substrate coupling and improve inductor Q [2]. Additionally, a separate local supply is used for the PLL, and about 1.2nF of on-chip supply decoupling is added. Finally, careful floor planning enables the maximum physical separation between the sensitive LNA input and frequency reference inputs. Figure 6 shows a photograph of the resulting chip. The signal path frequency response is shown in Figure 5, and the measured receiver performance is summarized in Table I.

Acknowledgments:

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References:

- [1] Arvin R. Shahani, Derek K. Shaeffer, and Thomas H. Lee, "A 12mW wide dynamic range CMOS front-end for a portable GPS receiver," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 12, Dec. 1997.
- [2] C. Patrick Yue and S. Simon Wong, "On-chip spiral inductors with patterned ground shields for Si-based RF IC's," in *1997 Symposium on VLSI Circuits Digest of Technical Papers*, 1997, pp. 85-86.

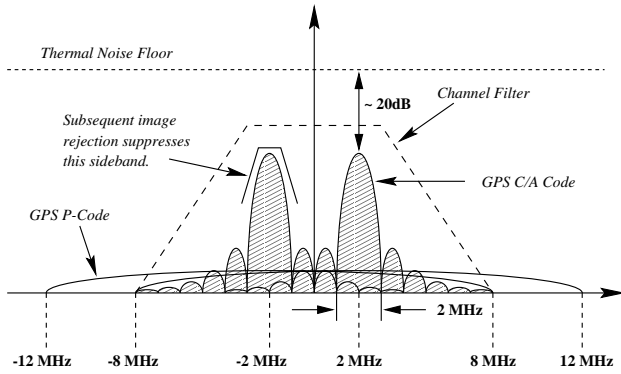


Fig. 1. Intermediate frequency signal structure.

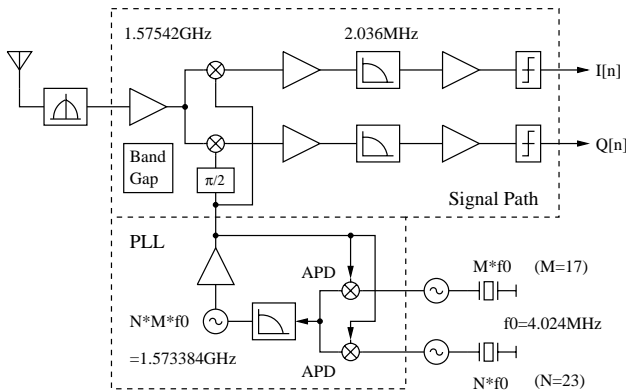


Fig. 2. Block diagram of the GPS receiver.

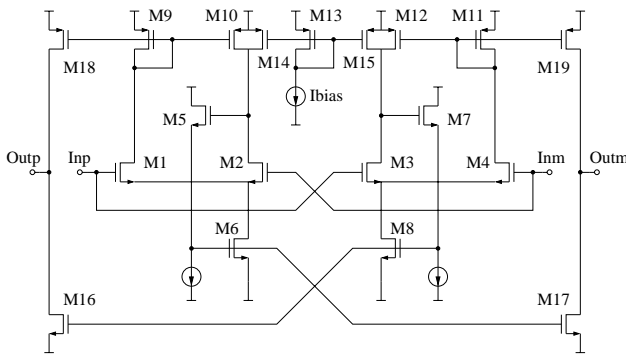


Fig. 3. Simplified gyrator transconductor circuit schematic.

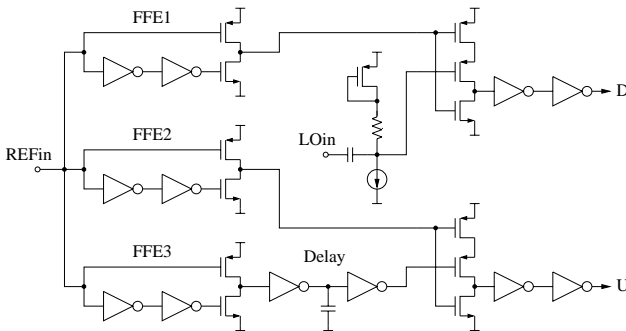


Fig. 4. Aperture phase detector (APD) schematic.

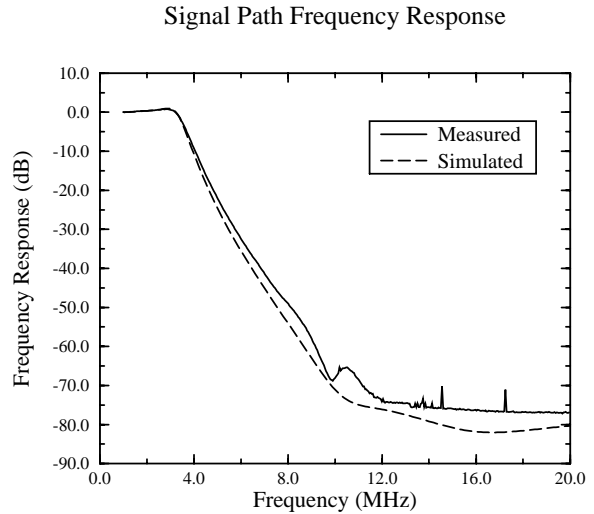


Fig. 5. Measured signal path frequency response.

TABLE I
MEASURED GPS RECEIVER PERFORMANCE.

Signal Path Performance	
LNA Noise Figure	2.4dB
LNA S11	$\leq -15\text{dB}$
Receiver Noise Figure ^a	5.4dB
IIP3 (Filter-limited)	-16dBm @ -43dBm P_s
Peak SFDR	57dB
Filter Cutoff Frequency	3.5MHz
Filter Pass-Band Peaking	$\leq 1\text{dB}$
Filter Stop-Band Attenuation	$\geq 50\text{dB}$ @ 8MHz $\geq 66\text{dB}$ @ 10MHz
Pre-Filter Power Gain	19dB
Pre-Filter Voltage Gain	32dB
Total Power Gain ^b	$\approx 82\text{dB}$
Total Voltage Gain	$\approx 107\text{dB}$
PLL Performance	
Loop Bandwidth	5MHz
Spurious Tones ^c	$f_0 \pm f_{ref} \leq -43\text{dBc}$ $f_0 \pm (f_{ref1} - f_{ref2}) \leq -53\text{dBc}$
VCO Tuning Range	240MHz ($\pm 7.6\%$)
VCO Gain Constant	240MHz/V
LO Leakage @ LNA Input	$\approx -53\text{dBm}$
Power Dissipation	
Signal Path	79mW
PLL / VCO	36mW
Supply Voltage	2.5V
Implementation	
Die Area	11.2mm ²
Technology	0.5 μm CMOS

^aIncludes balun loss of 0.5dB.

^bLimiting amplifier limits on system thermal noise.

^cDue to supply noise from the frequency references.

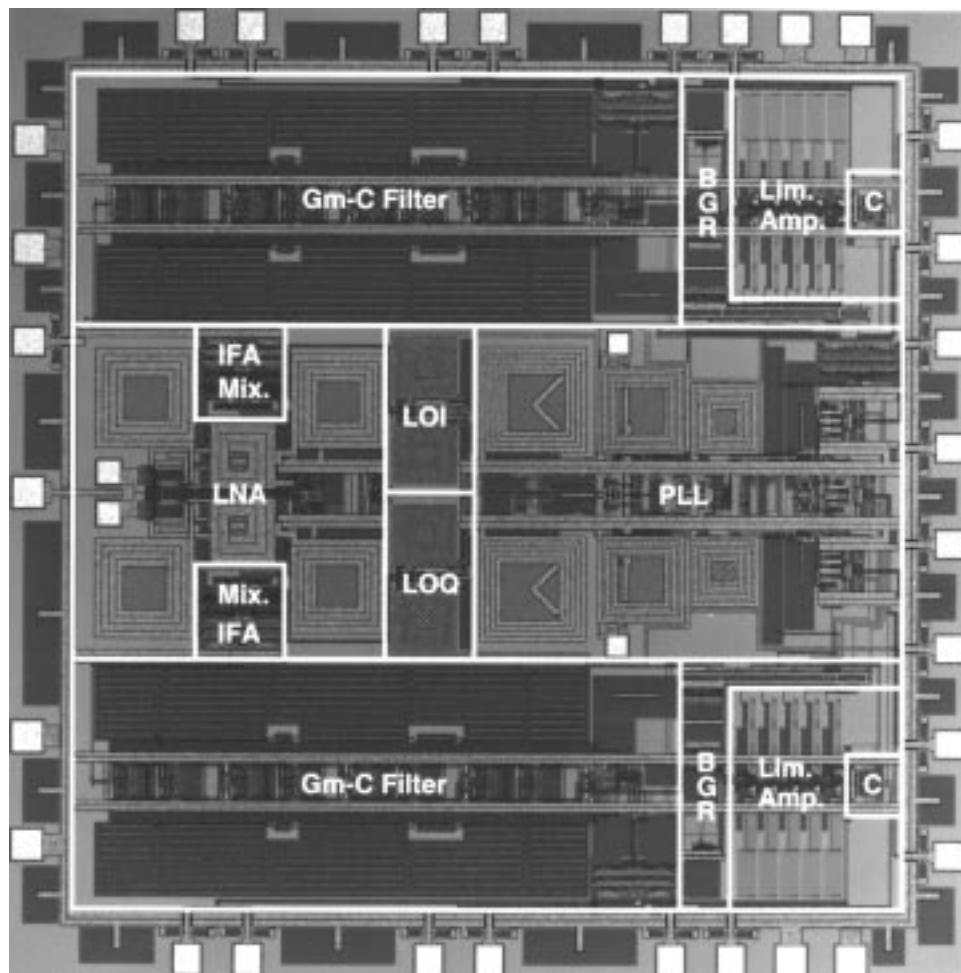


Fig. 6. Die photograph.