Fractal Capacitors

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Outline

● Motivation
● Fractal capacitors
● CAD tool
● Measurements
● Conclusions
Motivation

- Demand for linear capacitors
- Area efficiency
- Improvement with process scaling
- Reduction of bottom-plate capacitance
Traditional Capacitors

- **Gate Capacitance:**
  - High capacitance per unit area
  - Nonlinear
  - Requires DC bias voltage
  - Low breakdown voltage
  - Medium Q

- **Junction Capacitance:**
  - Highly nonlinear
  - Requires DC bias voltage
  - Sensitive to process variations
  - Low Q
  - Large temperature variation

- **Metal to Metal / Poly Capacitance:**
  - Linear
  - High Q
  - Small temperature variation
  - Low capacitance per unit area
Vertical vs. Lateral Flux

- Lateral flux increases the total amount of capacitance.
Fractal Geometries

- Some fractals have finite area but infinite perimeter.
Fractal Capacitor

- Quasi fractal geometries can be utilized to increase capacitance per unit area.
Layout Issues

- Cross connection
- Fractal dimension
Reduction of the Bottom-Plate Capacitance

- Area is smaller.
- Some of the field lines terminate on the adjacent plate instead of the substrate.
Scaling

Unlike conventional parallel-plate structures, the capacitance per unit area increases as the process technologies scale.
Other Advantages

- Lateral flux capacitors shift the burden of matching away from oxide thickness to lithography.

- The effect of systematic lithography offset is reduced due to pseudo-random nature of the structure.

- Capacitance density can be traded for lower series resistance.
LGFC
Layout Generator for Fractal Capacitors

CAD Tool

Tech. File → LGFC
Fractal Lib. → LGFC
User Input → LGFC
Layout → Field Solver
Report → Field Solver

C, L_s, & r_s
Fractal Construction: An Example

- Choose an “initiator.”
- Replace each segment of the initiator by a “generator.”
- Continue recursively.

An Initiator

\[ M = 4 \]

A Generator

\[ N = 8, \quad r = \frac{1}{4}, \quad D = \frac{\log(N)}{\log(1/r)} = 1.5 \]
Die Micrograph

Horizontal spacing=0.6 μm
Vertical spacing=0.8μm
Area=24,000 μm²
Capacitance Estimation

\[ C_{\text{lateral}} = K \frac{(\sqrt{A})^D}{(w + s)^{D-1}} \times t \]

- \( w \): Minimum width of the metal.
- \( s \): Minimum spacing between two adjacent strips.
- \( A \): Area of the fractal capacitance.
- \( t \): Thickness of the metal layers.
- \( K \): Proportionality factor that depends on the family of fractals being used.
- \( D \): Fractal dimension.
Boost Factor vs. Lateral Spacing

- D=1.8
- D=1.6

Area=24000 $\mu$m$^2$
Vertical metal spacing=0.8 $\mu$m
Metal thickness=0.8 $\mu$m
Measurements

$\text{Magnitude of } Y_{12} \text{ (siemens)}$

$\text{Frequency (Hz)}$

$\text{High-frequency two-port measurements}$

$f_{\text{res}} = 3.7 \text{ GHz}$

+ Measurements

- Best-Fit RLC Model
Measurements

\[ C = 5.5\,\text{pF} \]
\[ C_b = 0.3\,\text{pF} \]
\[ L_s = 0.34\,\text{nH} \]
\[ r_s = 1.3\,\Omega \]

Best-Fit Parameters
Measurements

Central Sites

Measurement Sites

22mm

8”
Capacitance distribution across the wafer

- Capacitance: 5.4pF, 5.5pF, 5.6pF
- Number of dice: 0, 1, 2, 3, 4, 5
- Central sites
  - $m = 5.5\text{pF}$
  - $\sigma_{\text{central}} = 9.4\text{fF} \ (0.2\%)$

Measurements:
- $\sigma = 83\text{fF}$
Measurements

• There is a good agreement between the measurements (5.5pF mean) and the simulations (5.4pF).

• 90% of the measured series inductance is due to connecting stubs.

• About 80% of the series resistance can be attributed to vias and connecting stubs.

• Both series resistance and inductance are dominated by non fundamental mechanisms.

• The overall improvement over a standard parallel plate capacitor is a factor of 2.3.
Conclusions

- Fractal capacitors use chip area more efficiently.
- Fractal capacitors are linear.
- The capacitance density improves with the scaling of process technologies.
- Bottom-plate parasitic capacitance is reduced.
- A CAD tool to automatically generate custom fractal layouts has been developed.