

MP 4.3 Monolithic CMOS Distributed Amplifier and Oscillator

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CMOS implementations for RF applications often employ technology modifications to reduce the silicon substrate loss at high frequencies. The most common techniques include the use of a high-resistivity substrate ($\rho > 10\Omega\text{-cm}$) or silicon-on-insulator (SOI) substrate and precise bondwire inductors [1, 2]. However, these techniques are incompatible with low-cost CMOS manufacture. This design demonstrates use of CMOS with a conventional low-resistivity epi-substrate and on-chip inductors for applications above 10GHz.

A three-segment distributed amplifier is illustrated in Figure 4.3.1. An oscillator is realized by connecting the output of the amplifier back to the input. The oscillation that builds up experiences the transmission line delay plus the average of one gate delay around the loop. This is different from a previous approach that uses both the reverse and forward traveling waves of the distributed amplifier to achieve wide tuning range [3]. The 50 Ω matched impedance enables fast rise and fall times which are essential to reducing noise sensitivity [4]. A high oscillation frequency is achieved by using n-FETs only.

The distributed amplifier and oscillator are implemented in a 0.18 μm CMOS technology with four Al-Cu metal layers. Coplanar striplines (CPS) were used as inductive elements [5]. To achieve a 50 Ω matched line when device loading is included, the CPS characteristic impedance must be larger than 50 Ω (Figure 4.3.1). A cross-section of the CPS is shown in Figure 4.3.2. The impedance increases with increasing spacing, S , but so does the coupling to the substrate and therefore the loss [5]. The dimensions chosen for this interconnect technology (4.4 μm T_{ox} between metal 4 and the substrate) are $W = 10\mu\text{m}$ and $S = 10\mu\text{m}$, which yield 70 Ω impedance. Interdigitated n-wells and substrate taps are placed underneath the CPS in order to avoid a continuous lossy low-inductance return path.

The loop length of the CPS for the oscillator is 2.5mm. Although the electric field spreads through the passivation and air above the lines as well as through the SiO_2 and Si below the lines, they are mostly confined in the SiO_2 . If an effective permittivity of $\epsilon_r = 4$ is assumed, the unloaded line delay is estimated to be 17ps. The parasitic gate and drain capacitances increase estimated loaded line delay to about 20ps (8ps/mm). The estimated gate delay is 5ps, and the simulated oscillation frequency is 20GHz with $V_{\text{pp}} = 1\text{V}$ (4dBm). SPICE simulations with fast Fourier transform predict -25dBc second harmonic and -20dBc third harmonic.

The S -parameters of the distributed amplifier are measured with an HP8510C network analyzer, cascade ground-signal (GS) coplanar probes, and external 50 Ω terminations (Z_{bias} and Z_{load}). The low-frequency gain is 5dB, and the unity gain cutoff frequency is 23GHz (Figure 4.3.3). The return loss is less than -13dB up to 18GHz. When the pads are included, the unity gain cutoff frequency is reduced to 13GHz. This is due to the large coupling from the input/output pads to the lossy substrate. During testing of the oscillator, the bias terminal is connected to a bias-T and the output is connected to an HP8565E spectrum analyzer. The measured operating frequency is 16.6 GHz (Figure 4.3.4), slightly lower than expected. The 2x30ps cycle time indicates that the loaded transmission line delay is 10ps/mm. This is verified by S -parameter characterization of the loaded

CPS under zero bias and small swing. The longer delay is due to additional layout parasitic capacitance and increased coupling through the high- ϵ_r silicon substrate. There are no spurs in the 0.1 to 50GHz range, and the second and third harmonics are clearly observable. The fundamental (-3.5dBm, $V_{\text{pp}} = 0.4\text{V}$) and harmonics are lower than simulation predictions due to the higher-than-expected pad loss. The third harmonic is also close to the 60GHz Bragg cutoff frequency determined by the CPS segment lengths.

A process split with thicker top level metal (2 μm instead of 1.1 μm) reduces the loss of the CPS. Thicker metal 4 results in slightly smaller line loss (from 0.7dB/ μm to 0.65dB/ μm at 17GHz) and smaller substrate coupling, which lead to a slightly higher center frequency (16.8GHz) and a higher signal power (-2.5dBm). The minor improvement for a 45% reduction in DC resistance (and 20% reduction in AC resistance due to skin effect) confirms that the transmission is determined by the line LC time-of-flight and not by the line RC delay. Although the n-wells underneath the CPS are not intended for tuning, changing the n-well bias could vary the line capacitance and provide a slight degree of tuning. The spectra when the n-well bias is scanned over a voltage range are shown in Figure 4.3.5. The slightly smaller tuning range for the 2 μm top-level metal is due to smaller substrate coupling.

The phase noise is measured with the setup shown in the inset of Figure 4.3.6. The reduced power dissipation, achieved by not terminating the bias-pad, improves the phase noise 6dB while reducing the oscillation frequency only 3%. Connecting only one probe also reduces the coupling to external components, thereby reducing the measurement uncertainty. The phase noise is -110dBc/Hz at 1MHz offset. The noise floor of the spectrum analyzer is also shown to verify validity of the measurements.

A die photo of the 0.3x1.5mm² distributed amplifier is shown in Figure 4.3.7. The CPS lines can be routed close to each other, resulting in a compact 0.3x1.5mm² layout.

Acknowledgments:

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- [4] Hajimiri, A., et al., "A General Theory of Phase Noise in Electrical Oscillators" IEEE Journal of Solid-State Circuits, Feb. 1998, vol.33, no. 2, pp. 179.
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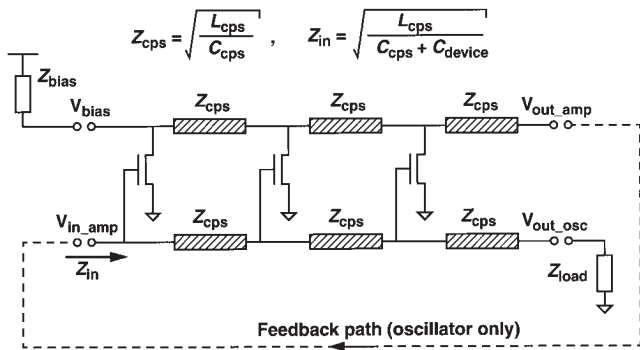


Figure 4.3.1: Amplifier and oscillator schematic.

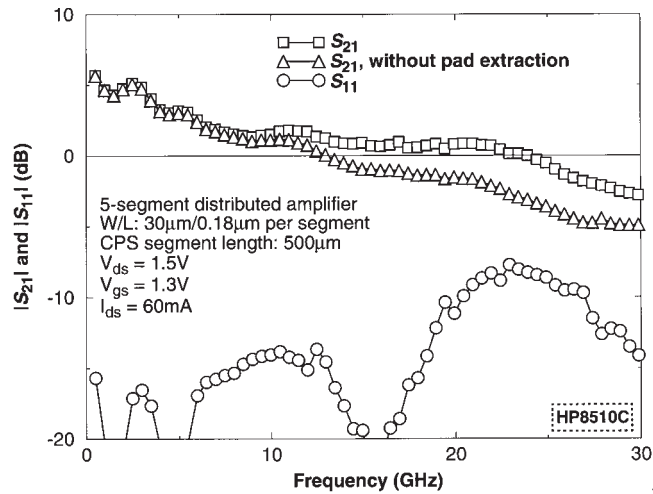


Figure 4.3.3: Distributed amplifier S-parameters.

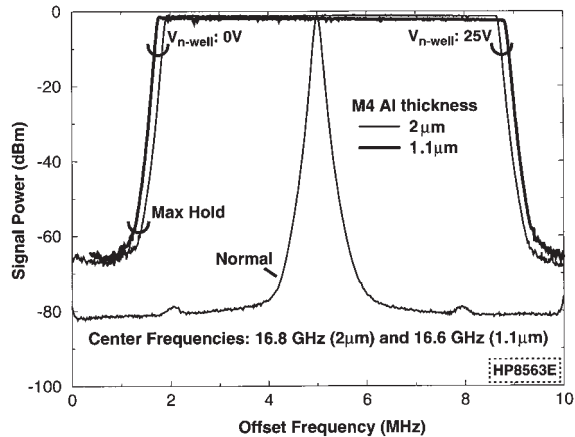


Figure 4.3.5: Expanded view of first harmonic.

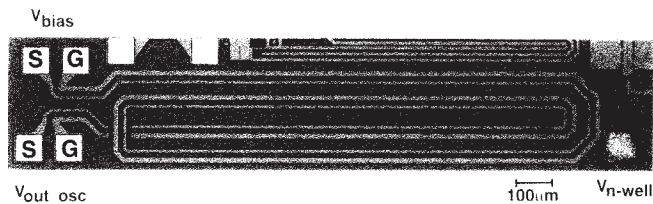


Figure 4.3.7: Distributed oscillator die micrograph.

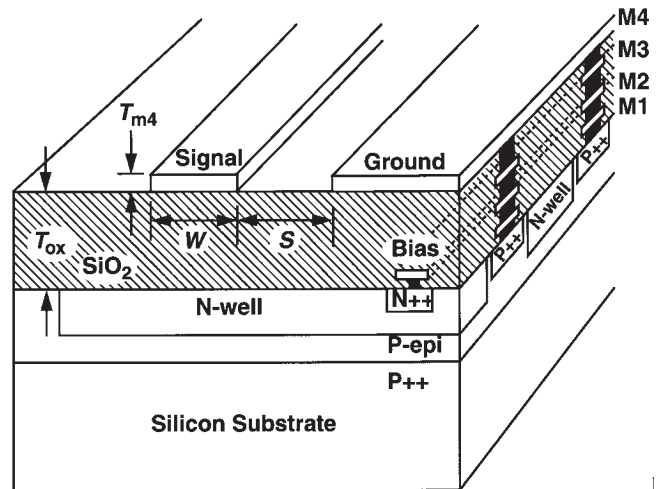


Figure 4.3.2: CPS and n-well bias cross-section.

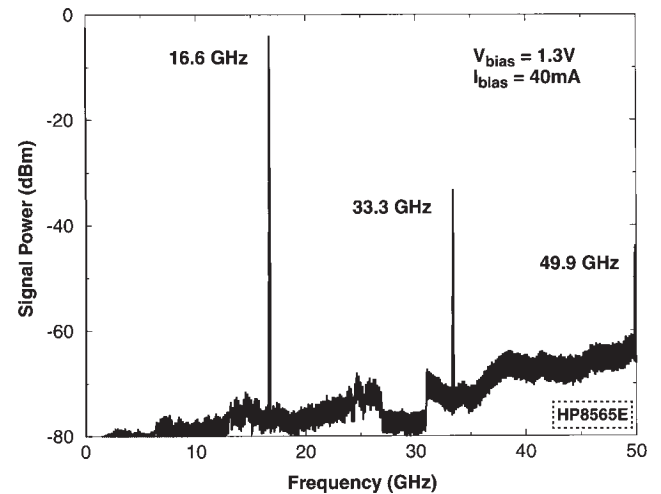


Figure 4.3.4: Oscillator power spectrum.

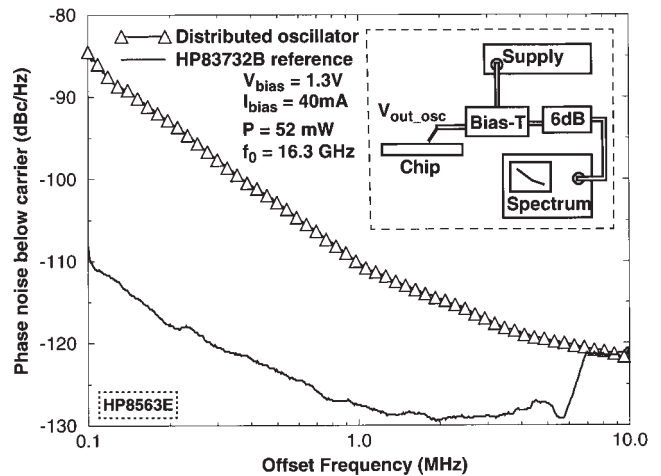


Figure 4.3.6: Oscillator phase noise spectrum.

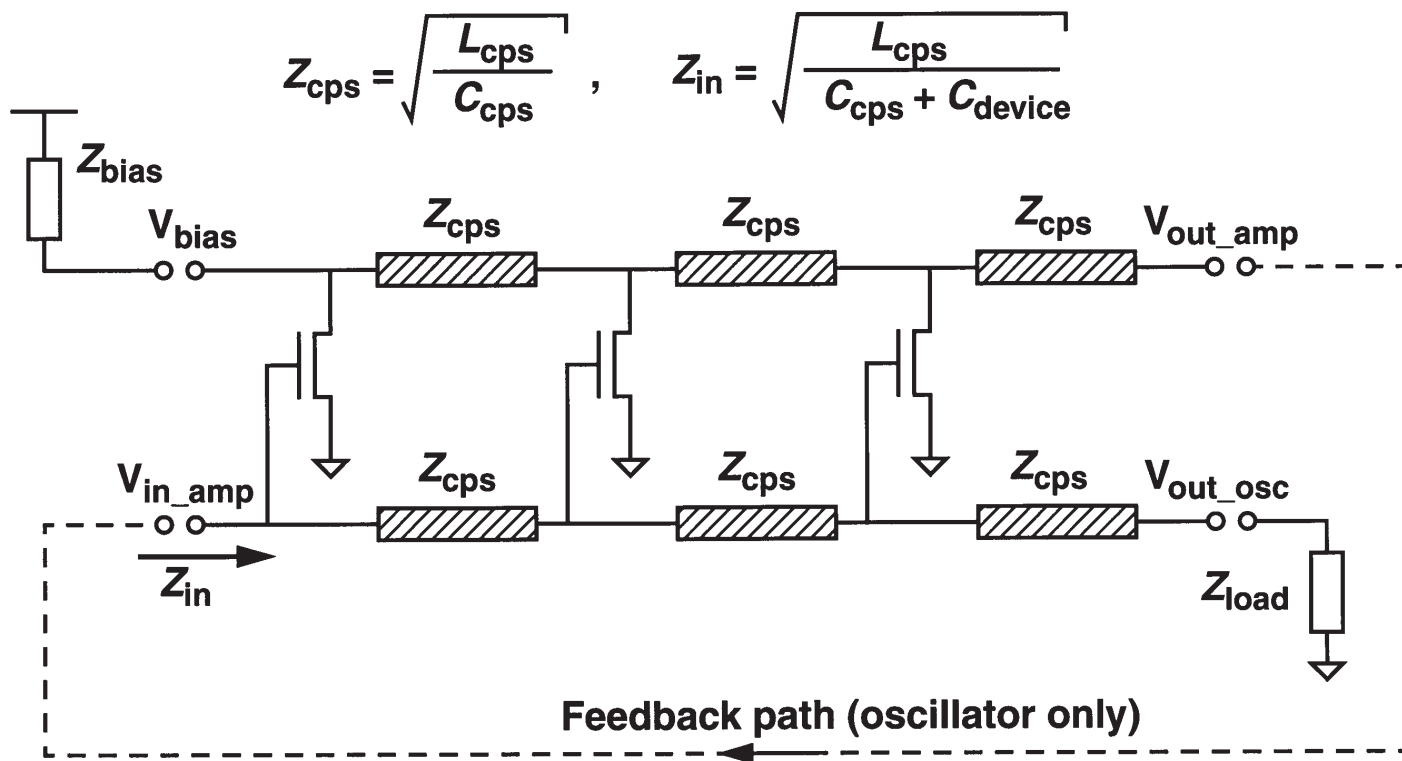


Figure 4.3.1: Amplifier and oscillator schematic.

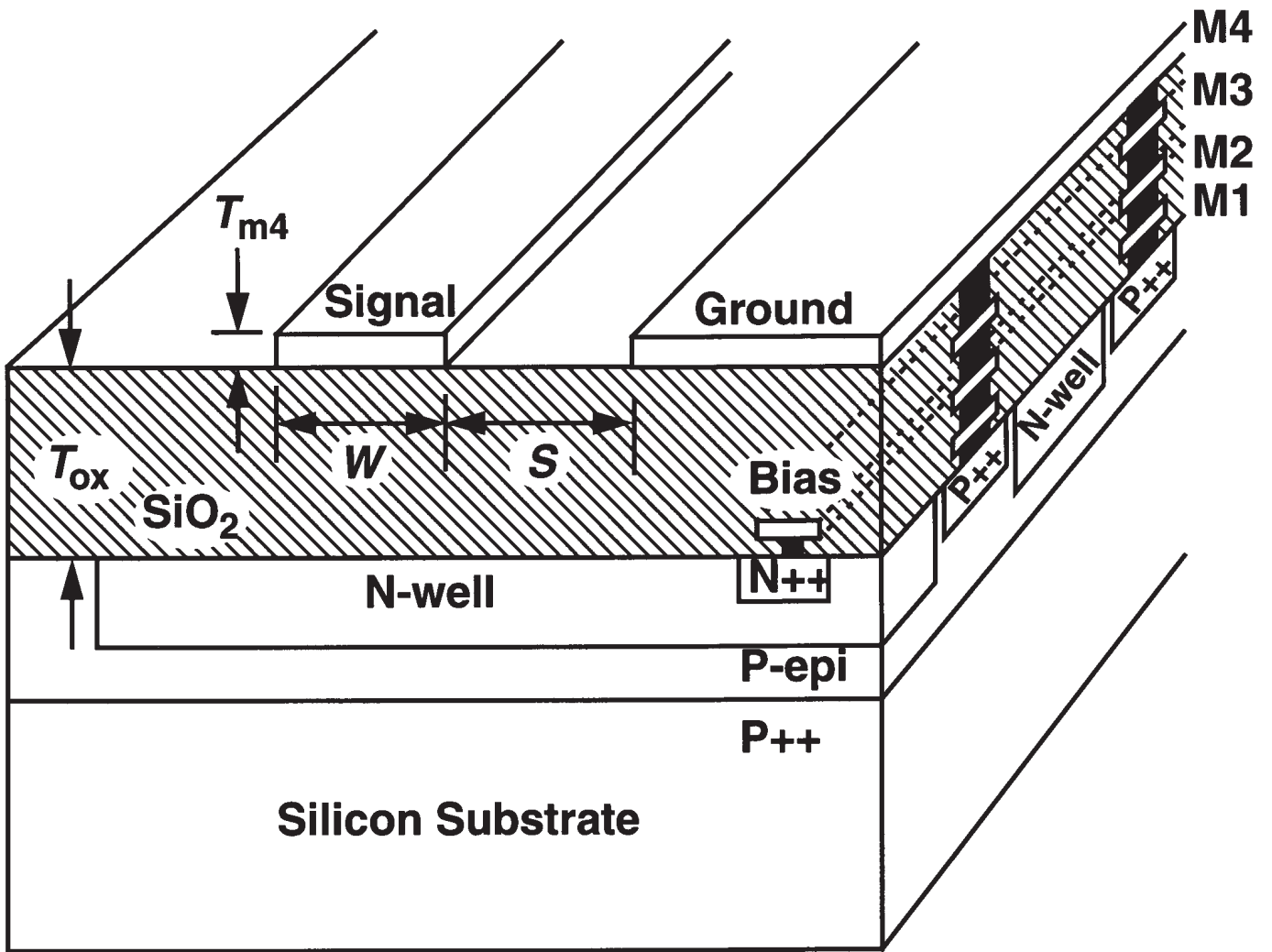


Figure 4.3.2: CPS and n-well bias cross-section.

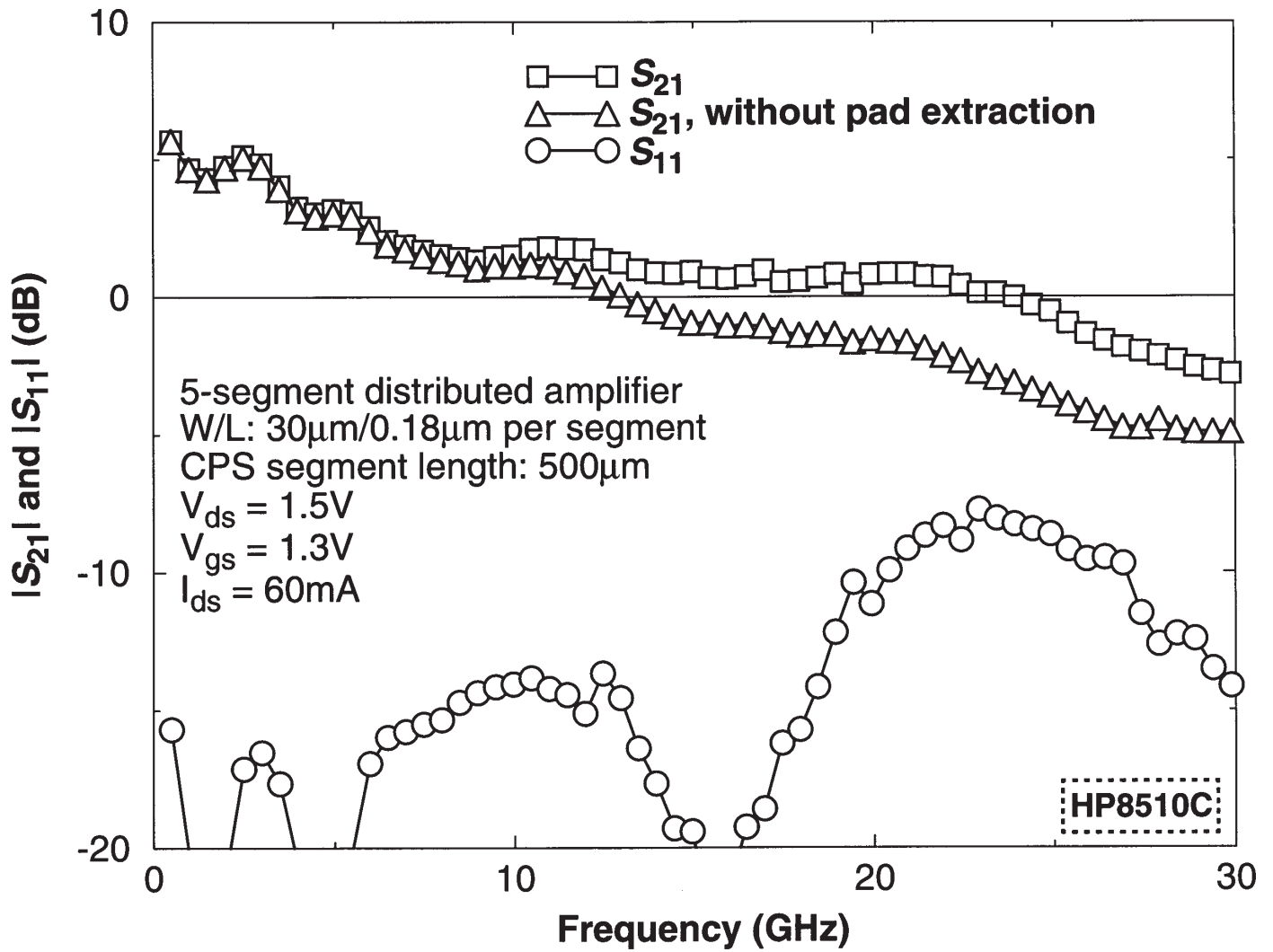


Figure 4.3.3: Distributed amplifier S-parameters.

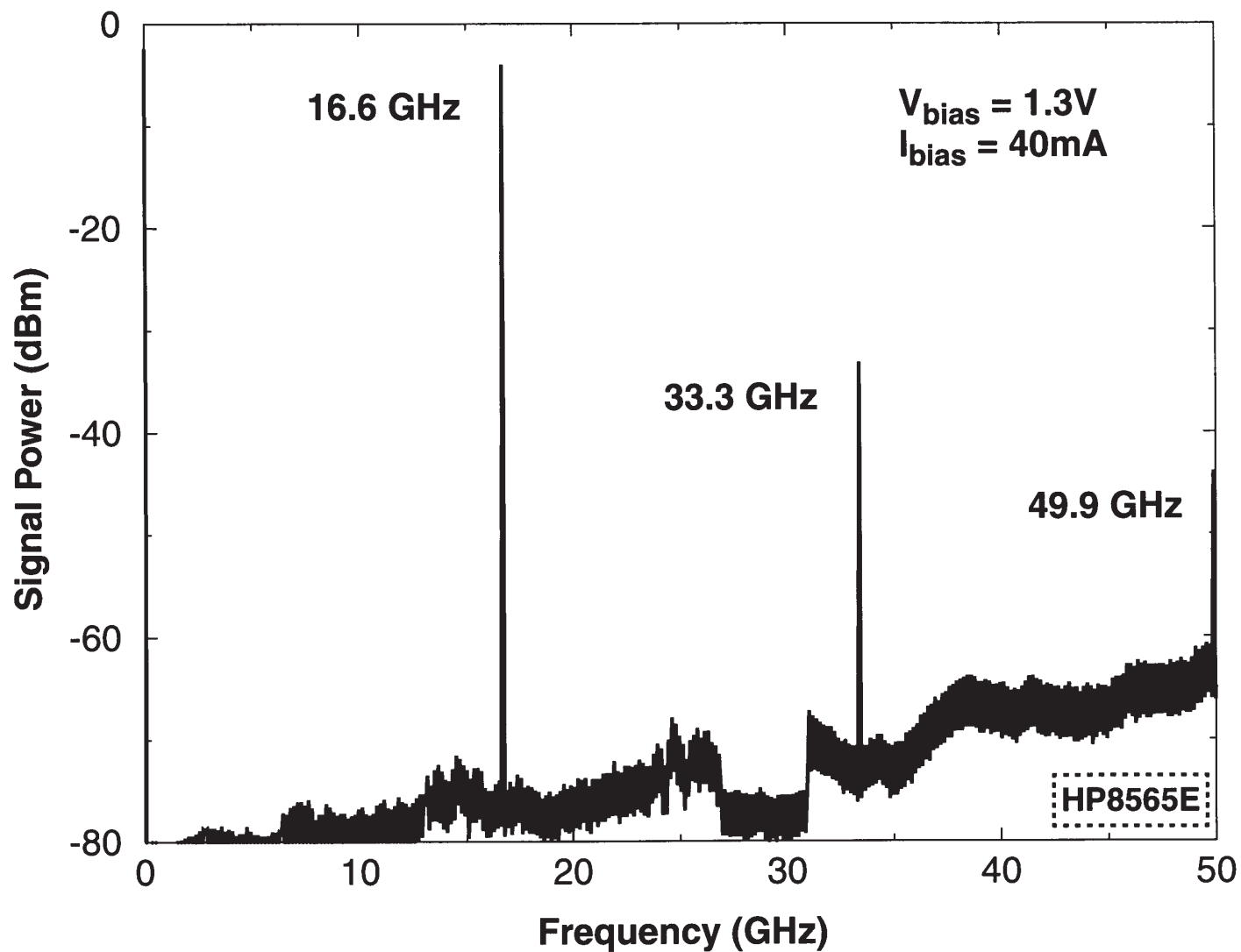


Figure 4.3.4: Oscillator power spectrum.

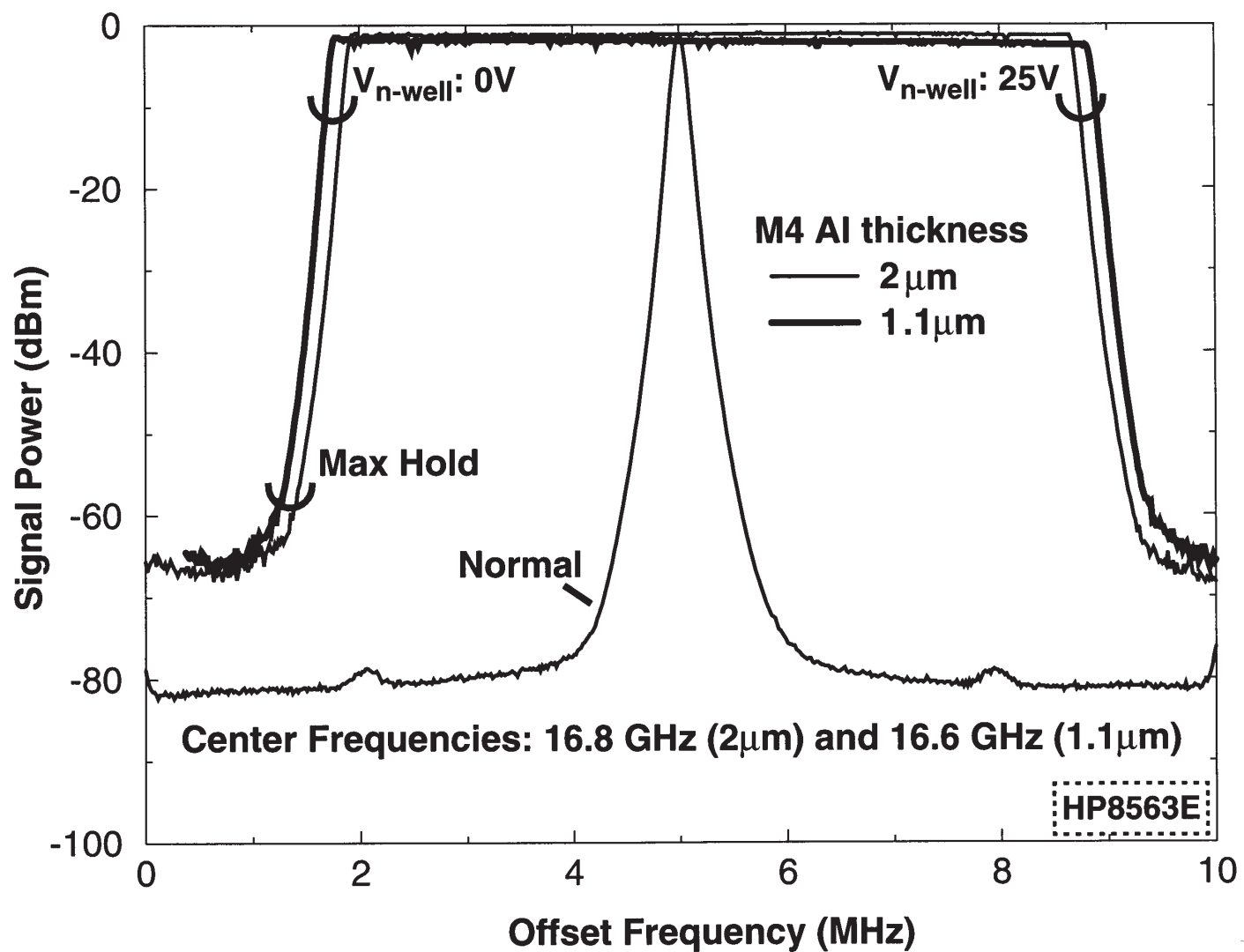


Figure 4.3.5: Expanded view of first harmonic.

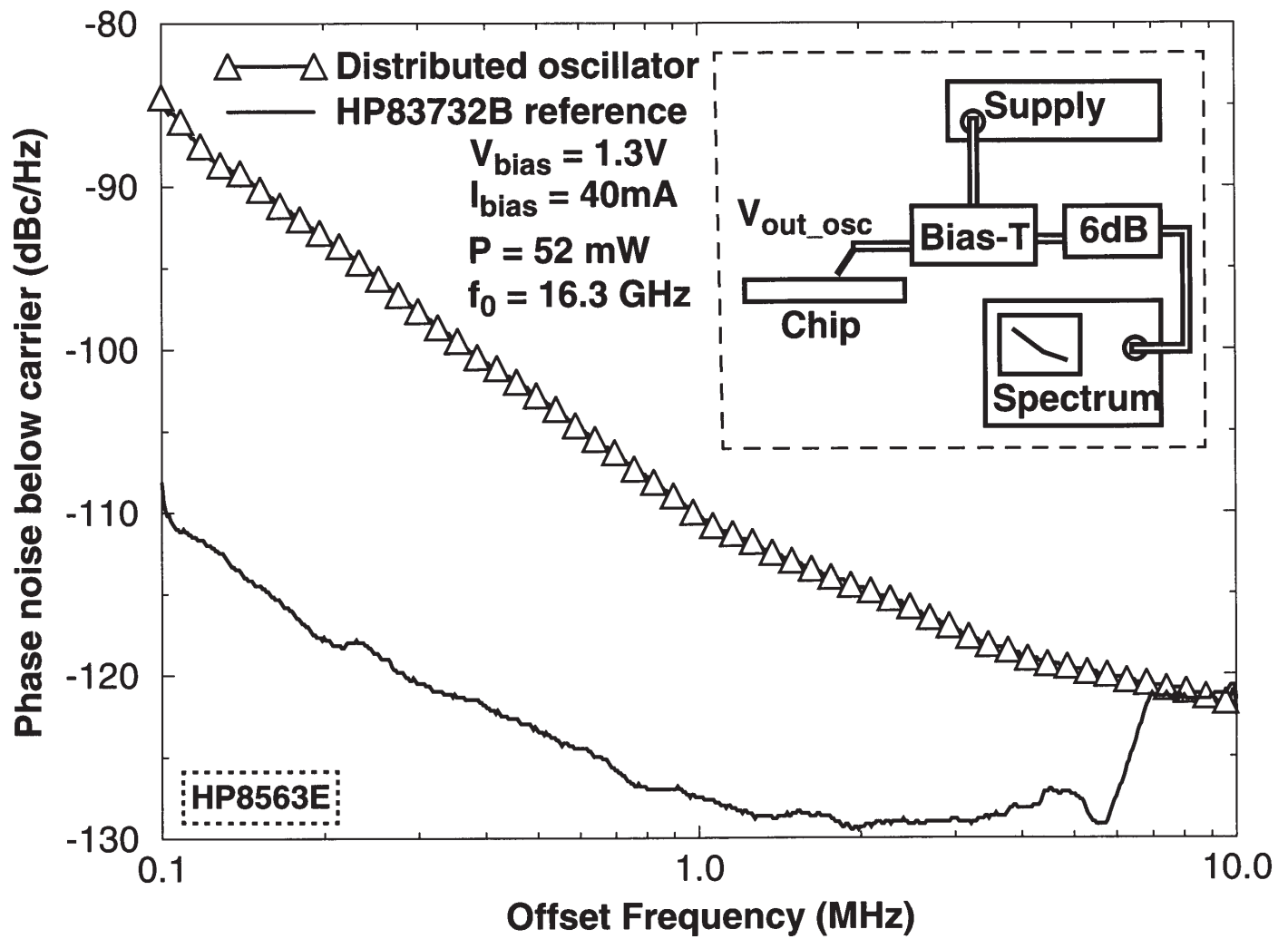


Figure 4.3.6: Oscillator phase noise spectrum.

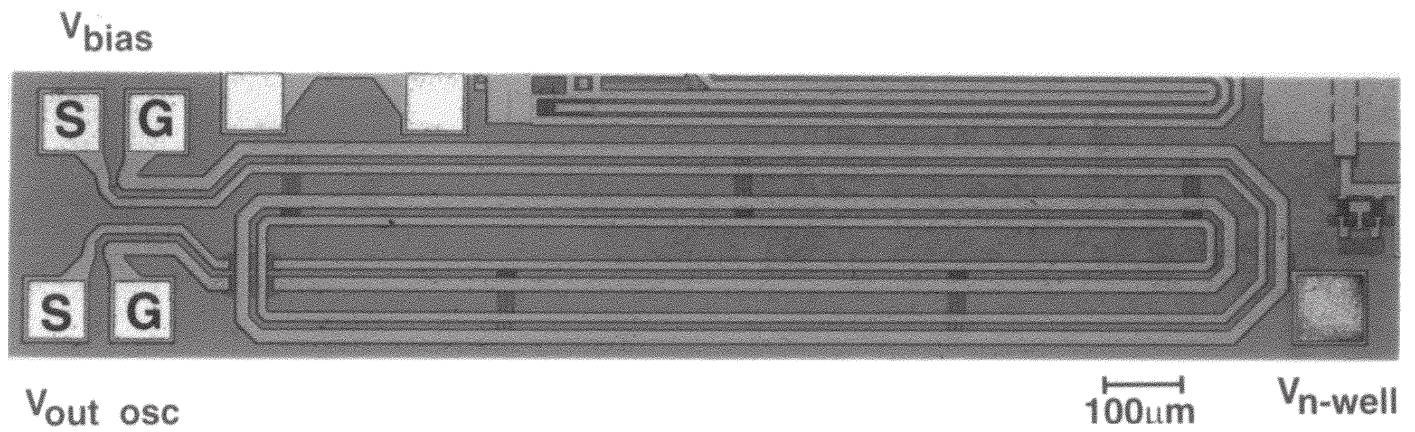


Figure 4.3.7: Distributed oscillator die micrograph.