LOW PHASE NOISE CMOS RING OSCILLATOR VCOs FOR FREQUENCY SYNTHESIS

Rafael J. Betancourt-Zamora and Thomas H. Lee
Stanford University, 420 Via Palou Mall, CIS-26, Stanford, CA 94305-4070, betasoft@smirc.stanford.edu

Abstract

We propose a methodology that uses a new phase noise model to trade-off phase noise and power dissipation in the design of ring oscillators suitable for frequency synthesis. We compare the theoretical phase noise performance of three buffer stages using clamped, symmetric and cross-coupled loads, respectively. We propose a cross-coupled buffer topology that achieves lower phase noise by exploiting symmetry. This achieved a 95% reduction in the $1/f^3$ corner frequency of the phase noise characteristic.

Introduction

The explosive growth in portable mobile communications have driven the need for integrated, low power frequency synthesizers. Frequency synthesizers provide the precise reference frequencies for modulation and demodulation of RF signals. Traditionally, frequency synthesizers have been implemented using phase-locked loops (PLL). The major sources of power dissipation in a PLL are the VCO and the frequency divider. An alternative frequency-locked loop (FLL) synthesizer architecture has been proposed [1], that eliminates the need for a frequency divider.

All practical frequency sources have undesirable phase fluctuations due to intrinsic device noise. Phase noise is particularly important in RF systems as it can lead to (1) increased bit error rates (BERs) in digital communication systems, (2) contamination of adjacent frequency channels and (3) receiver desensitization due to reciprocal mixing where out-of-band signals are translated into the IF [2].

In a typical digital communication system, phase noise in the local oscillator can cause the signal constellation to rotate in a random fashion, thereby degrading the BER performance. As an example, Figure 1 shows the effects of noise on the constellation for a QPSK modulated signal, where (a) shows the effect of additive white gaussian noise (AWGN), while (b) adds the effect of phase noise at the carrier frequency. The noise have been exaggerated for illustration purposes. It shows how phase noise increases the probability of error in the detection of the signal by skewing the constellation thus reducing the effective distance between the symbols.

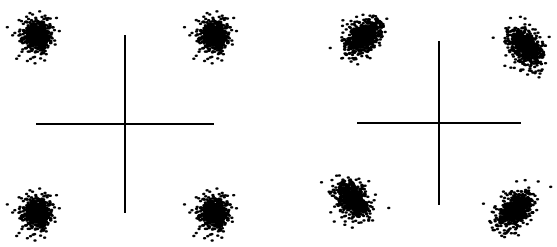

Figure 1. QPKS constellation: (a) with AWGN, (b) with AWGN and oscillator phase noise

A PLL tracks the phase noise of the reference signal within its loop bandwidth, relaxing the close-in phase noise requirements of the VCO (provided that the reference has better phase noise than the VCO). This is why VCO phase noise is usually specified at frequency offsets beyond the suppression range of the PLL. However, a FLL tracks frequency, not phase. This makes the specification of close-in phase noise of a VCO for a FLL more critical.

The VCO's power dissipation is determined by the frequency of operation and the phase noise performance required. Power dissipation at a given frequency cannot be made arbitrarily small, as it is constrained by the choice of technology, and by the system's phase noise requirements.

This paper presents a design methodology for differential ring oscillators suitable for FLL frequency synthesis, that trades off power dissipation with phase noise. These oscillators are intended for a biotelemetry application in the 174-216MHz VHF band.

VCO Design

Power vs. Frequency Trade-off

For a differential ring oscillator, the total power dissipation is given by

$$P = NI_{dd}V_{dd} \quad \textbf{(1)}$$

where N is the number of stages, I_{dd} is the tail current of the differential pair, and V_{dd} is the supply voltage. The frequency of oscillation can be approximated by

$$f \approx \frac{I_{dd}}{2NC_L V_S} \quad \textbf{(2)}$$

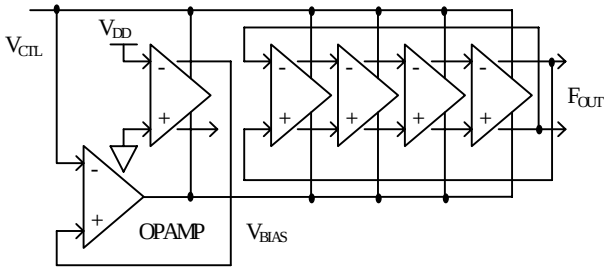

Figure 2. Differential ring oscillator VCO with replica bias

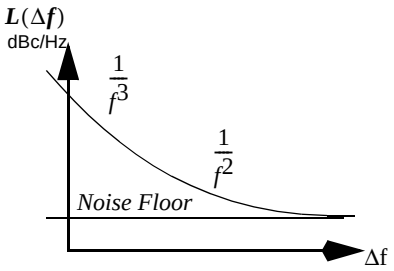

Figure 3. Oscillator close-in phase noise due to upconversion of thermal and *1/f* device noise

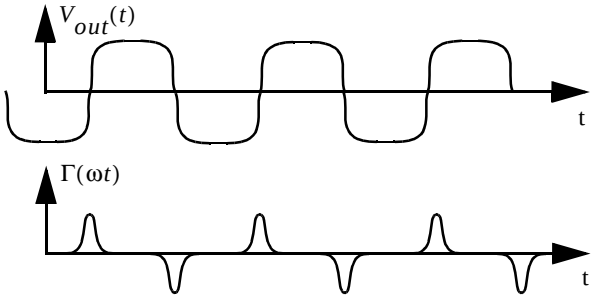

Figure 4. Ring oscillator waveforms: (a) single-ended output, $V_{out}(t)$, (b) impulse sensitivity function $\Gamma(\omega t)$

where C_L is the total load capacitance and V_s is the maximum single-ended voltage swing at the output of each stage.

The VCO consists of a 4-stage ring oscillator (Figure 2) that uses buffer delay stages with replica-feedback biasing [3]. The buffers are NMOS differential pairs with linear PMOS loads. The replica bias feedback ensures that the loads are always in their linear region by forcing the swing V_s to be the same as $(V_{dd}-V_{ctl})$. Frequency control is achieved by varying V_{ctl} which also changes the bias I_{dd} of the buffer stages. The layout of the ring oscillator is symmetrical and load balanced to avoid any skewing between the phases.

Power vs. Phase Noise Trade-off

The Hajimiri phase noise model [4-6] predicts the upconversion of thermal and *1/f* device noise into close-in phase noise. Phase noise in the $1/f^2$ region is due to white device thermal noise (Figure 3). For a differential ring oscillator using short-channel devices, one may derive the following lower bound on the single-sideband phase noise in the $1/f^2$ region:

$$L\{\Delta f\} \geq \frac{18kTV_{dd}}{\pi^2 P} \cdot \left(\frac{2.5}{E_C L_{eff}} + 1\right) \cdot \left(\frac{f_o}{\Delta f}\right)^2 \cdot N \qquad \textbf{(3)}$$

where P is the power dissipation given by (1), E_C is the critical field in silicon, and L_{eff} is the gate length of the differential-pair devices. Observe that phase noise is a strong function of the number of stages, which justifies

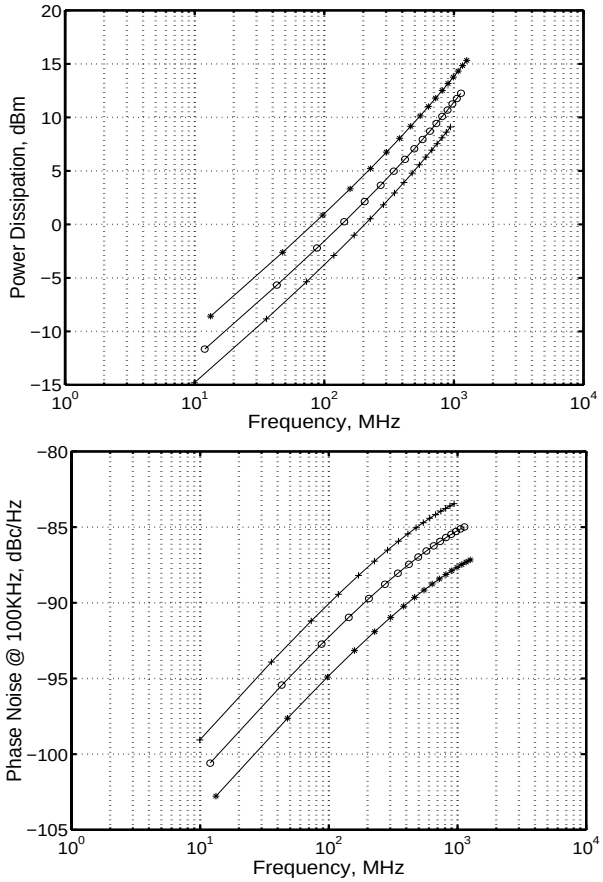

Figure 5. Power dissipation and phase noise for differential ring oscillator using PMOS linear loads and replica-feedback biasing: (+)W_n=3μm, (o)W_n=6μm, (*)W_n=12μm

the selection of a 4-stage oscillator.

Phase noise in the $1/f^3$ region is due to device $1/f$ noise. It is usually assumed that the $1/f^3$ corner frequency is the same as the $1/f$ corner of device noise. This is not true, as the $1/f^3$ corner is actually given by:

$$f_{1/f^3} = f_{1/f} \cdot \frac{\Gamma_{dc}^2}{\Gamma_{rms}^2} \qquad \textbf{(4)}$$

where Γ_{dc} is the DC value and Γ_{rms} is the RMS value of $\Gamma(x)$, the impulse sensitivity function (ISF). The ISF is a function of the output waveform and it accounts for the time-variant sensitivity of the oscillator to its noise sources. Figure 4 shows the ISF corresponding to a typical ring oscillator waveform. We can observe a high sensitivity to noise at the transitions of the output waveform.

The upconversion of device $1/f$ noise occurs through Γ_{dc}. However, the DC value of the ISF is governed by the symmetry properties of the single-ended output waveform. This model thus predicts the upconversion of $1/f$ device noise into close-in phase noise as a function

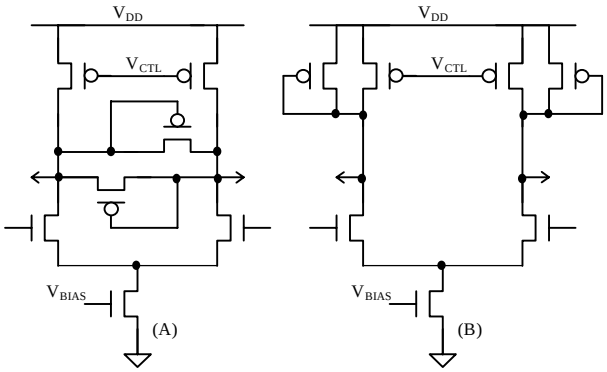

Figure 6. Differential delay buffer cells: (a) VCO_1, clamped-load; (b) VCO_2, symmetric load

of the symmetry of the output waveform.

To study the trade-off between phase noise and power dissipation we used (1) and (2) to plot the power dissipation vs. frequency (Figure 5) for differential pair devices of different widths W_n. The same figure also shows the corresponding $1/f^2$ phase noise bound given by (3) using a frequency offset from the carrier of 100KHz. We assumed a typical 0.5µm CMOS process (V_{dd}=3.3V, E_c=5.6x10^{6}V/m, $f_{1/f}$=3MHz), $W_{pmos}=2W_n$, all minimum length (L_{eff}=0.5µm) short-channel devices, and V_s= (V_{dd}-V_{ctl}).

We observe that V_s increases with frequency, which increases the power dissipation, and lowers the phase noise. Still, the net effect on phase noise is an increase with frequency as predicted by (3). For our design we selected the W_n=6µm curve for an oscillation frequency of 200MHz at a power level of 2.1dBm (1.6mW @ 3.3V) with L = -90dBc/Hz at 100KHz offset.

Differential Buffer Topology

Three ring oscillators were designed, each using a different PMOS load circuit for the delay buffer stage: VCO_1-clamped load, VCO_2-symmetric load, and VCO_3-cross-coupled load, respectively.

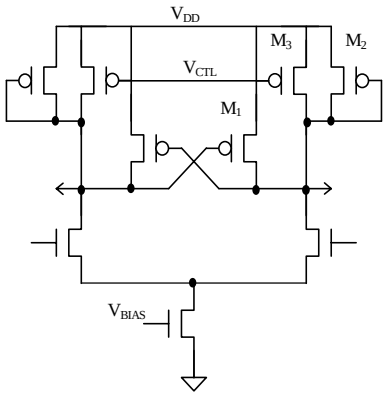

Figure 7. VCO_3, differential delay buffer cell with cross-coupled loads

The clamped-load differential buffer (Figure 6a) used in VCO_1 has excellent noise and PSR characteristics [7]. The cross-coupled diode loads clamp the output swing making the buffer delay insensitive to common-mode noise. Symmetric load buffers (Figure 6b), as used in VCO_2, also have very good supply noise rejection characteristics and have been used extensively in PLL and clock generator designs [8].

For the proposed cross-coupled load (Figure 7) design of VCO_3, we started with a symmetric load stage with no cross-coupling and swept the width of the cross-coupling devices while maintaining the total width ($W_1+W_2=W_3=6\mu m$) of the loads constant. The maximum symmetry of the output waveform was observed when the widths of M_1 and M_2 were equal to half the width of M_3.

Results

To compare the three topologies, a more detailed noise analysis was performed. The predicted noise for a 4-stage oscillator in the $1/f^2$ region is given by:

$$L\{\Delta f\} = \frac{\Gamma_{rms}^2}{(\pi V_s C_L \Delta f)^2} \cdot \frac{\overline{i_n^2}}{\Delta f} \qquad \textbf{(5)}$$

where is the total noise contribution from all sources at the output node. Figure 8 shows the predicted phase noise for VCO_1, VCO_2, and VCO_3. The $1/f^2$ regions are within 2.6dB of each other as it is to be expected for similarly sized noise sources. The model also predicts lower phase noise in the $1/f^3$ region for VCO_3 as it has better symmetry than the other two.

Table 1 shows the phase noise at 100KHz offset, and the $1/f^3$ corner frequency for all three oscillators running at 200MHz. Note that as expected due to the better symetry, the $1/f^3$ corner for VCO_3 is 95% lower than

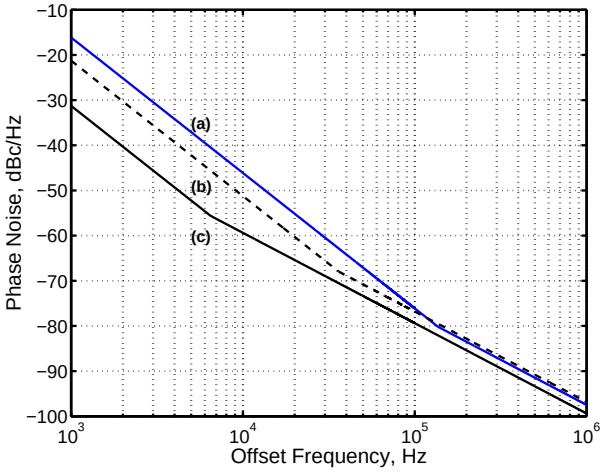

Figure 8. Predicted single-sideband phase noise: (a) VCO_1, (b) VCO_2, (c) VCO_3

Oscillator	$1/f^3$ corner, KHz	L{100KHz}, dBc/Hz
VCO_1	137	-75
VCO_2	36	-77
VCO_3	6.5	-80

Table 1: Theoretical phase noise and $1/f^3$ corner frequency for VCO_1, VCO_2, VCO_3

that of VCO_1. These theoretical phase noise and power vs. frequency characteristics are in good agreement with those reported previously [1] for VCO_1.

A test chip was fabricated through MOSIS using the HP 0.5µm CMOS process (Figure 9). Testing is underway using the HP-E5500 phase noise measurement system and results will be available at the conference.

Conclusion

To minimize power dissipation of the VCO, a design technique based on a new phase noise model was presented. We compared the phase noise performance of three differential buffer stages. We proposed a cross-coupled load buffer that achieves lower phase noise in the $1/f^3$ region by exploiting single-ended symmetry in the oscillator's waveform.

Acknowledgments

We wish to thank Ali Hajimiri, and Miguel Gabino-Perez for their assistance. This work was partially supported by NASA-Ames Research Center through a Training Grant No. NGT 2-52211.

References

[1] R.J. Betancourt-Zamora, A. Hajimiri, and T.H. Lee, *"A 1.5mW, 200MHz CMOS VCO for wireless biotelemetry,"* First International Workshop on Design of Mixed-Mode Integrated Circuits and Applications, Cancun, Mexico, pp. 72-74, July, 1997.

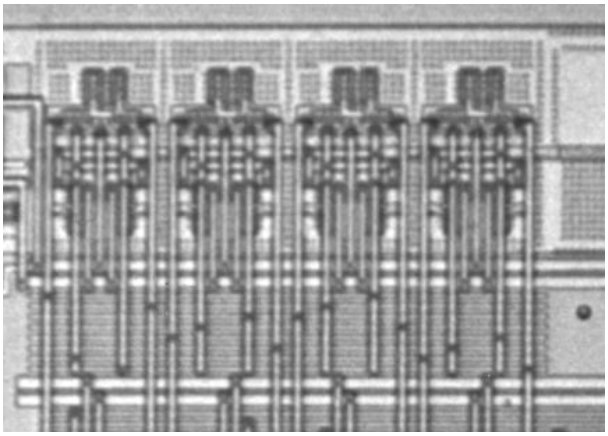

Figure 9. Microphotograph of VCO_3: differential delay buffer cell with cross-coupled loads

[2] J.A.Crawford, "Frequency Synthesizer Design Handbook", Artech House, Boston, 1994.

[3] J. Maneatis and M. Horowitz, *"Precise delay generation using coupled oscillators,"* IEEE Journal of Solid-State Circuits, vol. 28, pp. 1273-1282, December 1993.

[4] A. Hajimiri and T.H. Lee, *"A general theory of phase noise in electrical oscillators,"* IEEE Journal of Solid-State Circuits, vol. 33, pp. 179-194, February 1998.

[5] A. Hajimiri and T.H. Lee, *"Phase noise in multi-gigahertz CMOS ring oscillators,"* Custom Integrated Circuits Conference Digest, pp. 49-52, May 1998.

[6] A. Hajimiri and T.H. Lee, *Correction to "A general theory of phase noise in electrical oscillators,"* IEEE Journal of Solid-State Circuits, vol. 33, p. 928, June 1998.

[7] M. Horowitz, et al., *"PLL design for a 500MB/s interface,"* Int'l Solid-State Circuits Conference Digest, pp. 160-161, February 1993.

[8] J. Maneatis, *"Low-jitter and process-independent DLL and PLL based on self-biased techniques,"* Int'l Solid-State Circuits Conference Digest, pp. 130-131, 430, February 1996.