50-GHz Interconnect Design in Standard Silicon Technology

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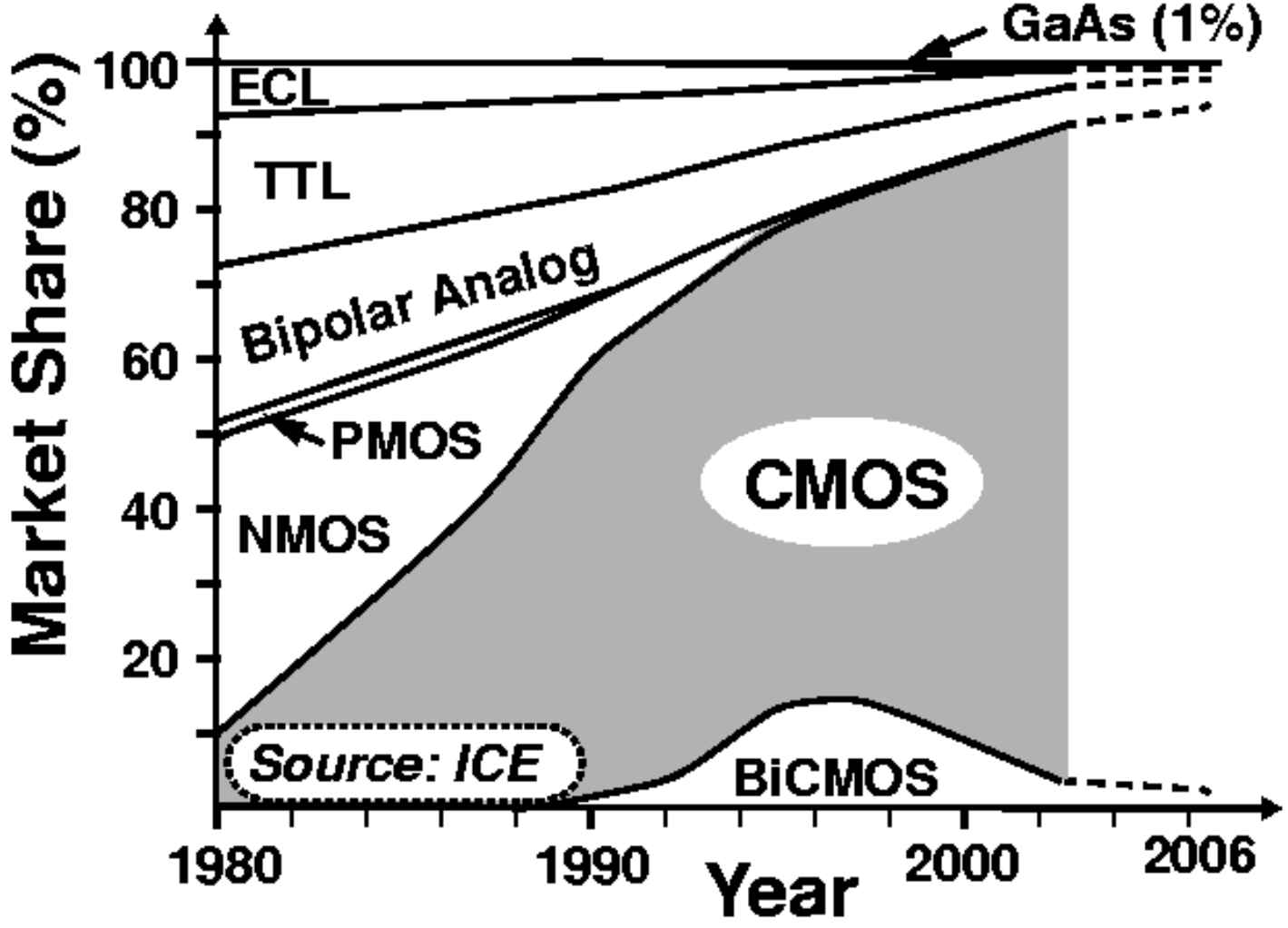
Outline

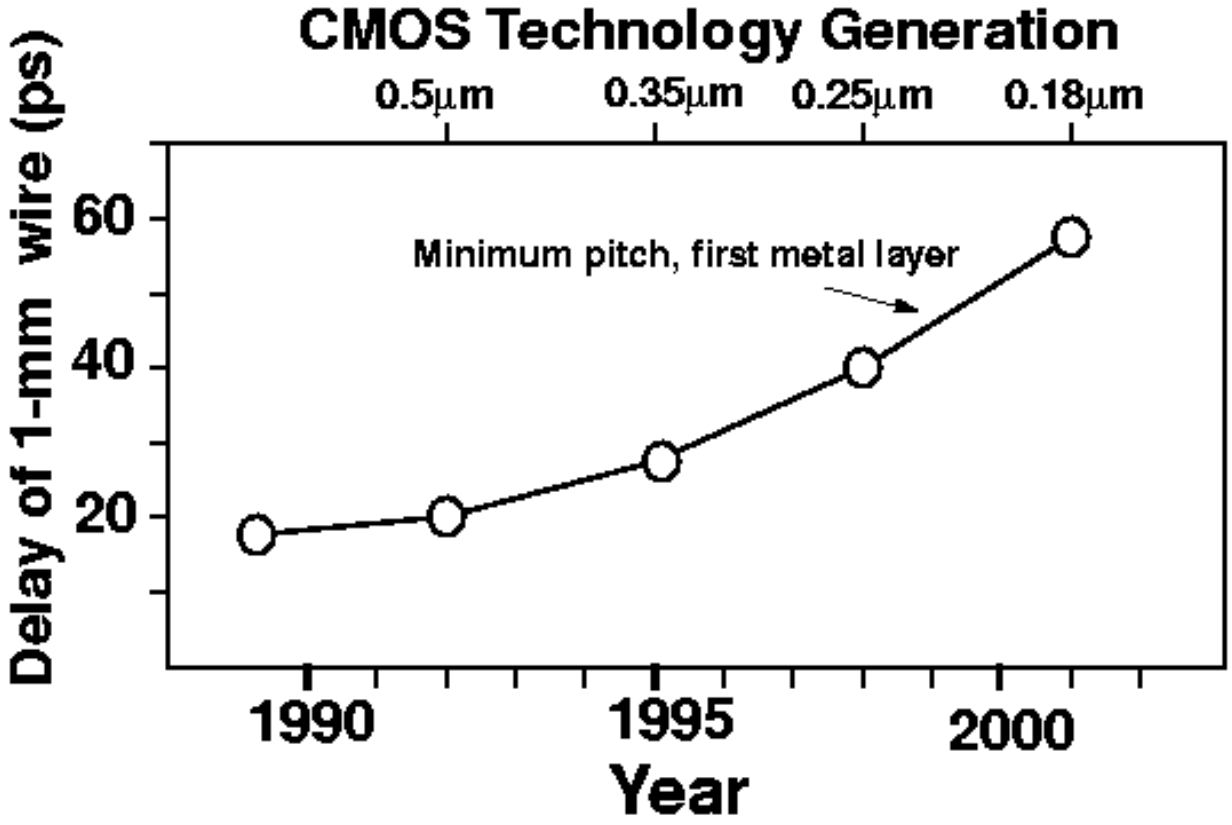
- Introduction, Logic Process Scaling
- Future Interconnect Process Emulation
- On-Chip Transmission Lines on Si
- Monolithic Resonator Design
- Conclusions

IC Technology Market Trend ($)



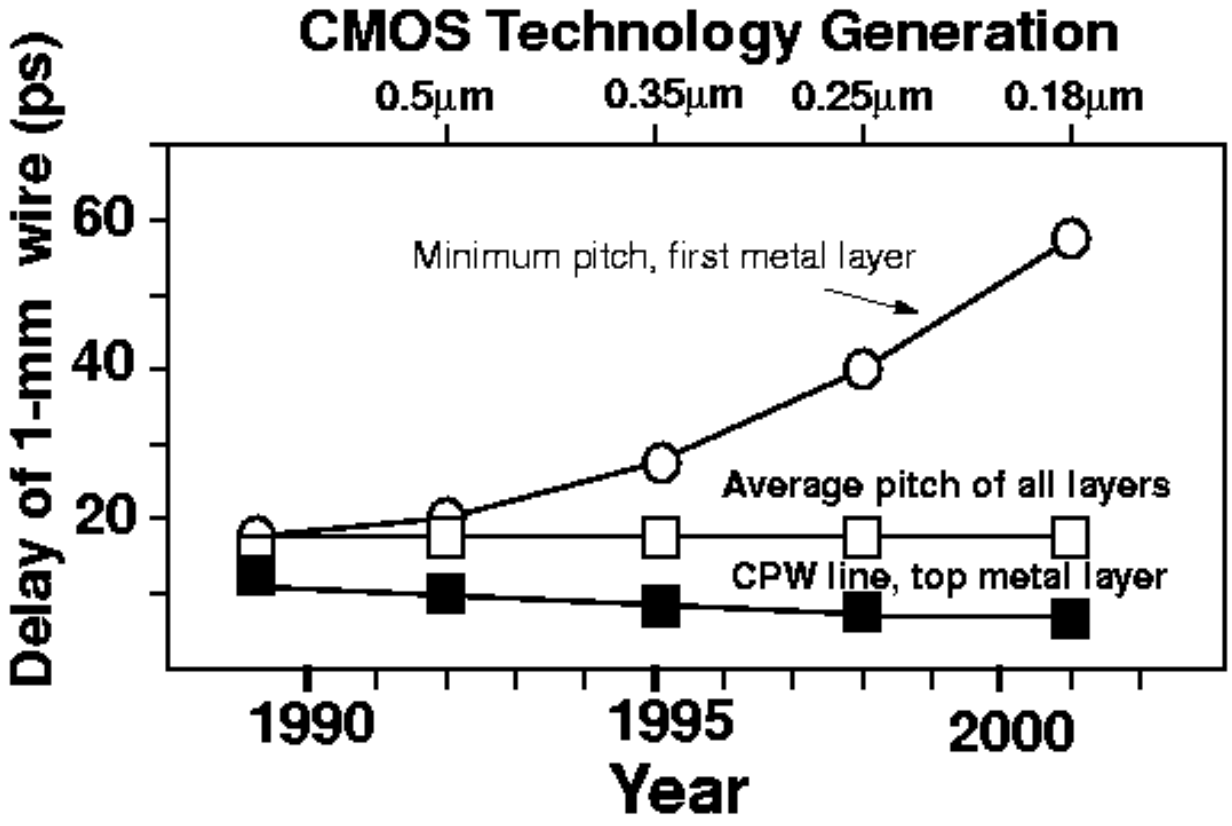
CMOS Logic Process Scaling Trends

- Dimensions and gate delay: 0.7x per generation
- Interconnect delay: ?



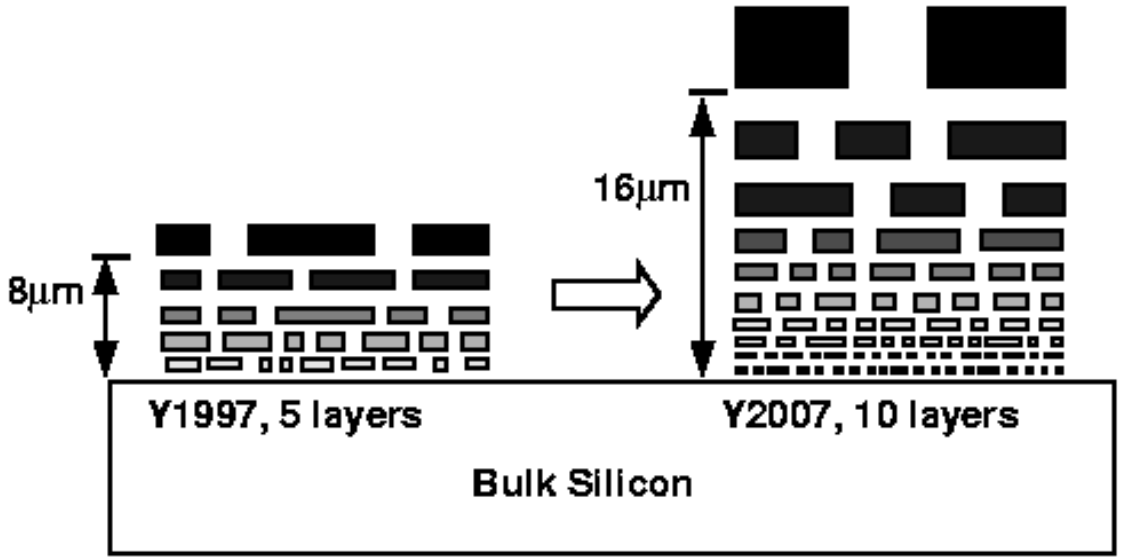
CMOS Logic Process Scaling Trends

- Interconnect delay: ***depends on the level***

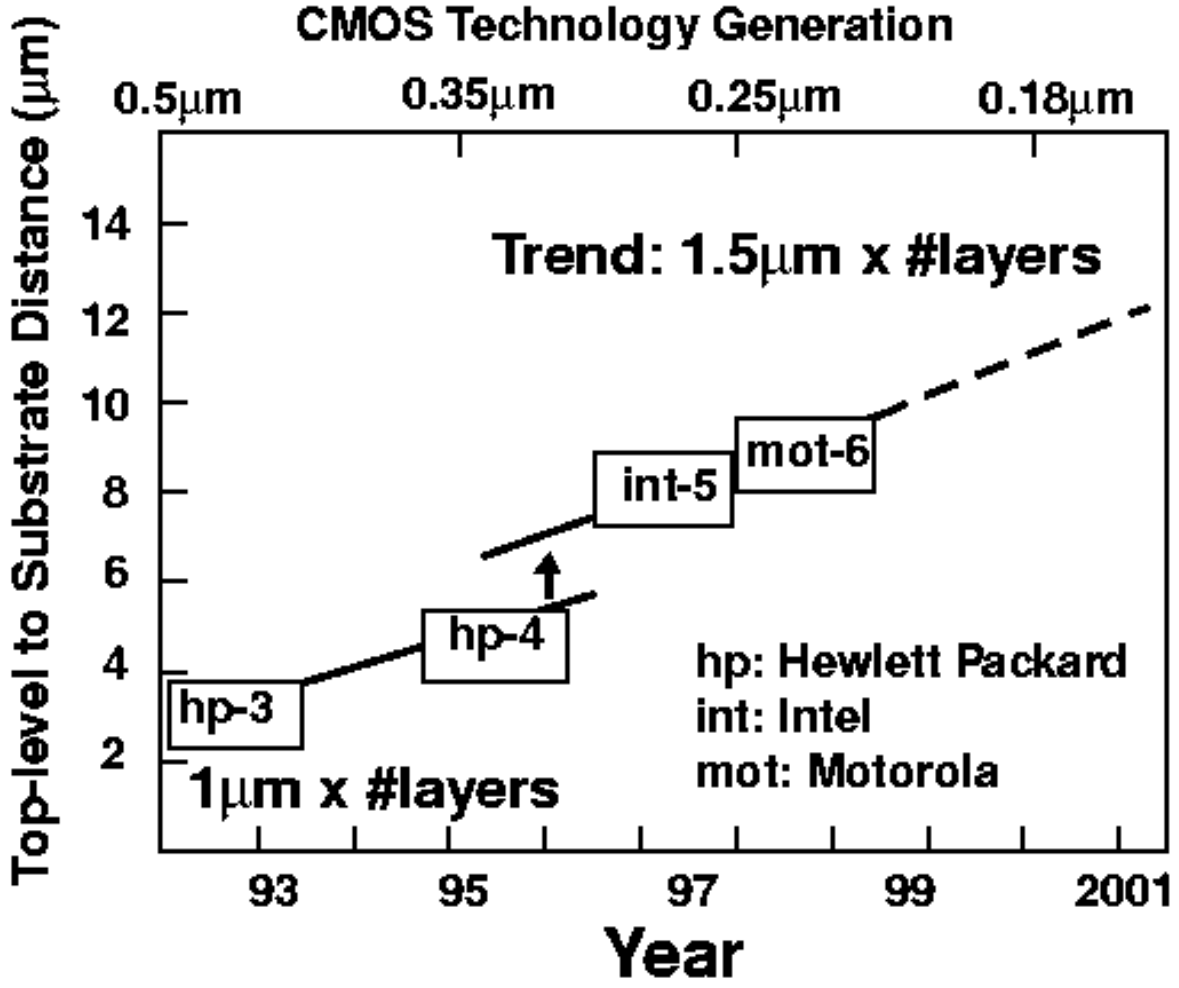


Reverse Scaling of Top-Layer Metals

- CMOS transistor density increases
- Supply current increases

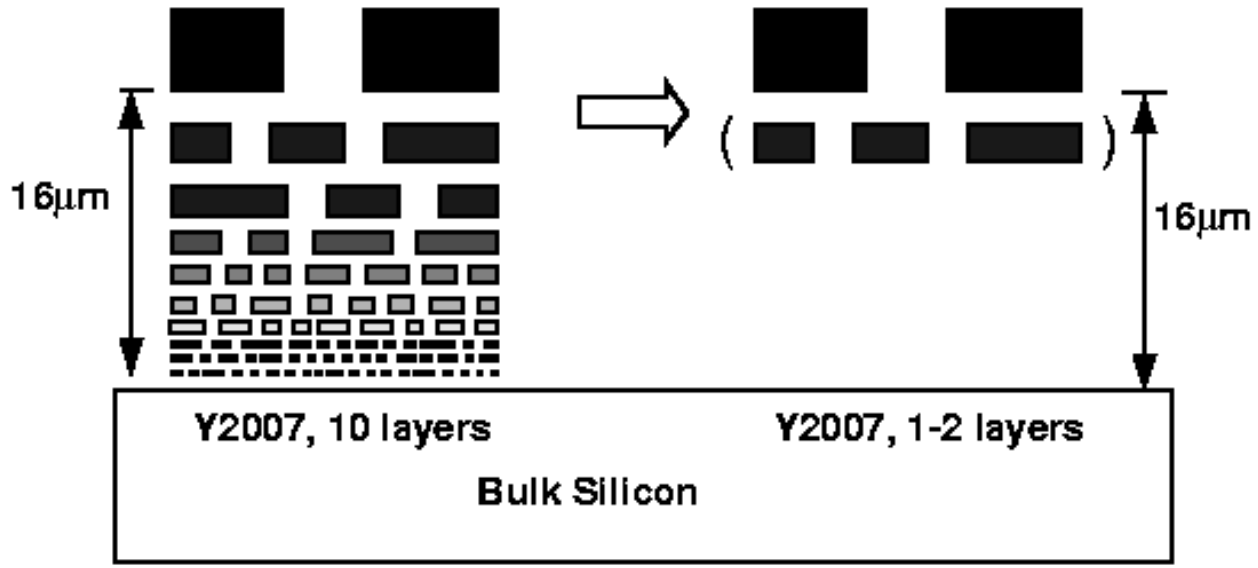


Top-Level Metal to Si Distance Trend

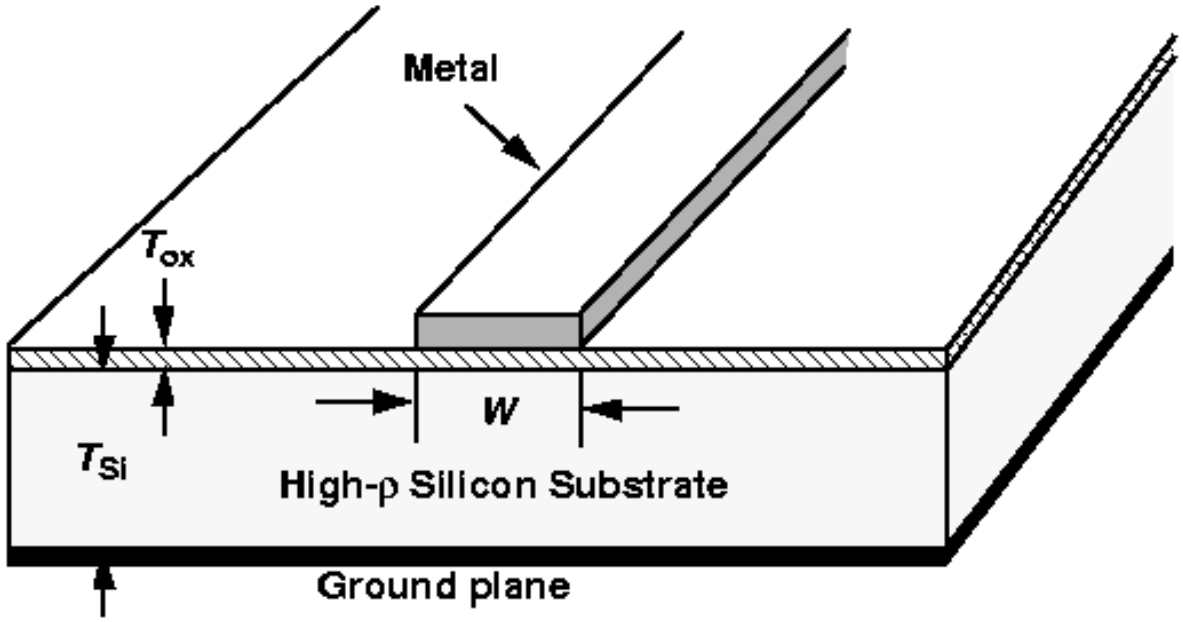


Future Interconnect Process Emulation

- Only emulate top metal layer(s)
- Deposit thick oxide underneath metal layers

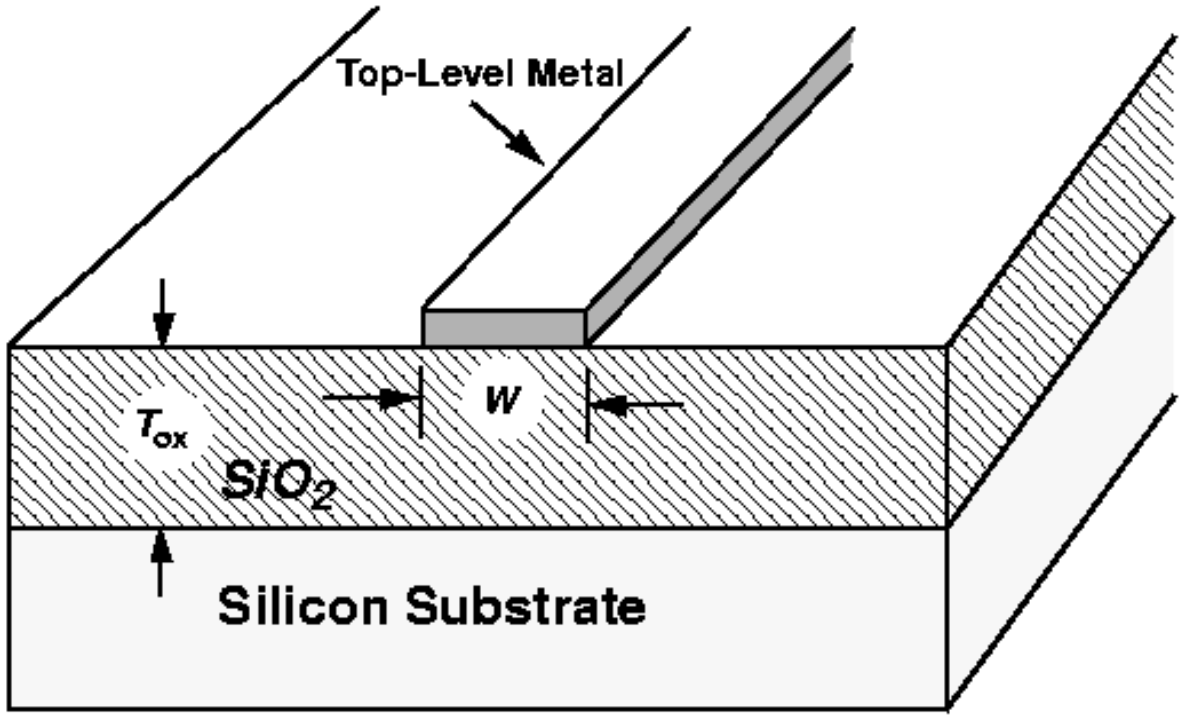


On-Chip Microstrip with High-ρ Si



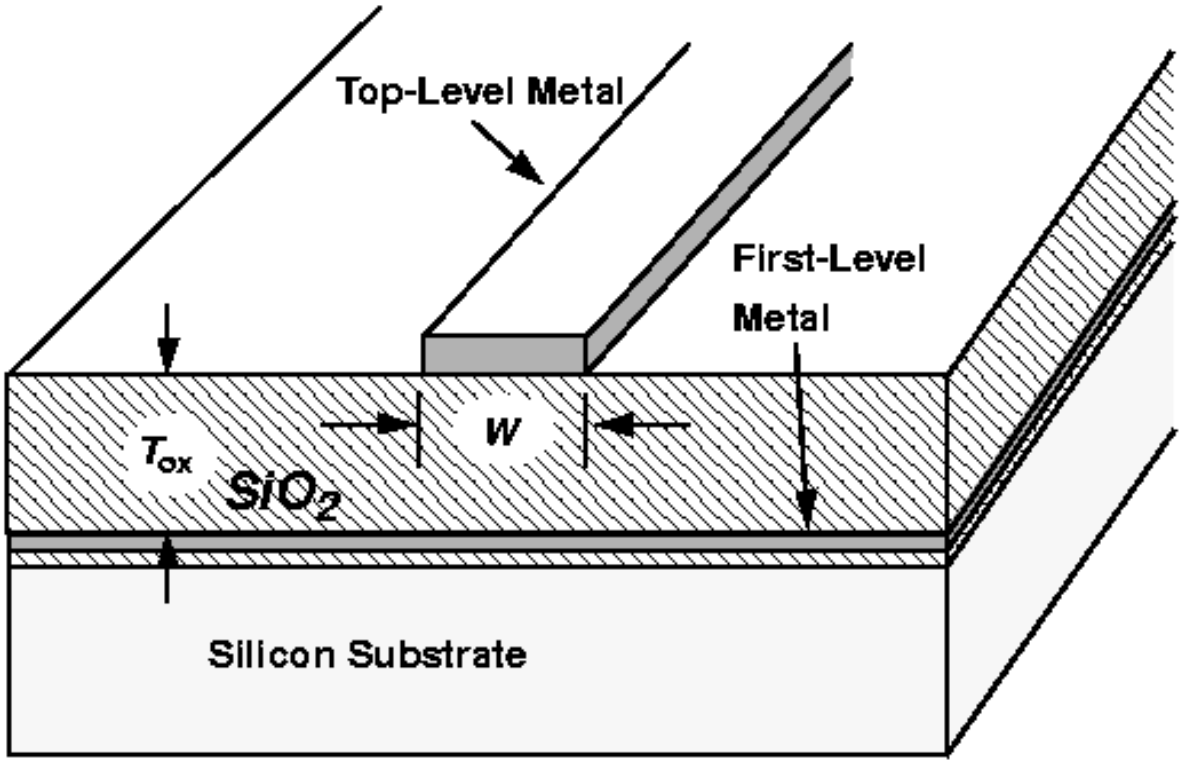
- High *dielectric* losses in substrate

On-chip Microstrip with Low-ρ Si



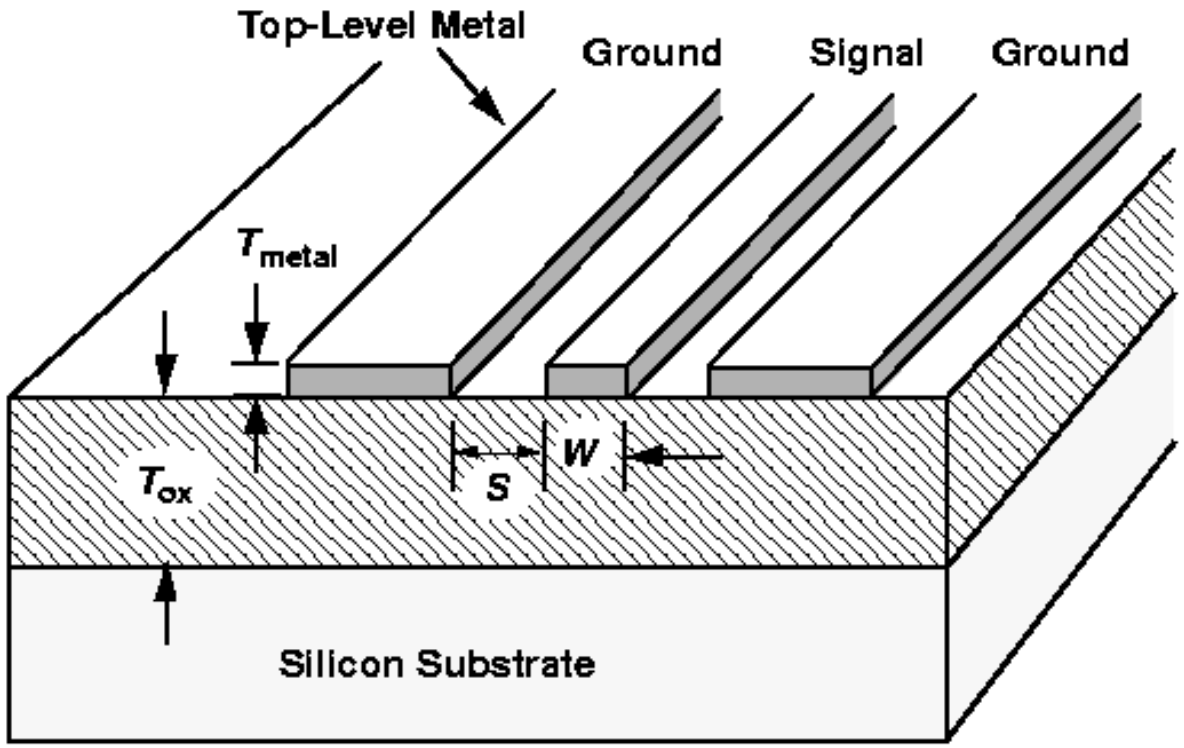
- High *resistive* losses in substrate

Microstrip with M1 Ground Return



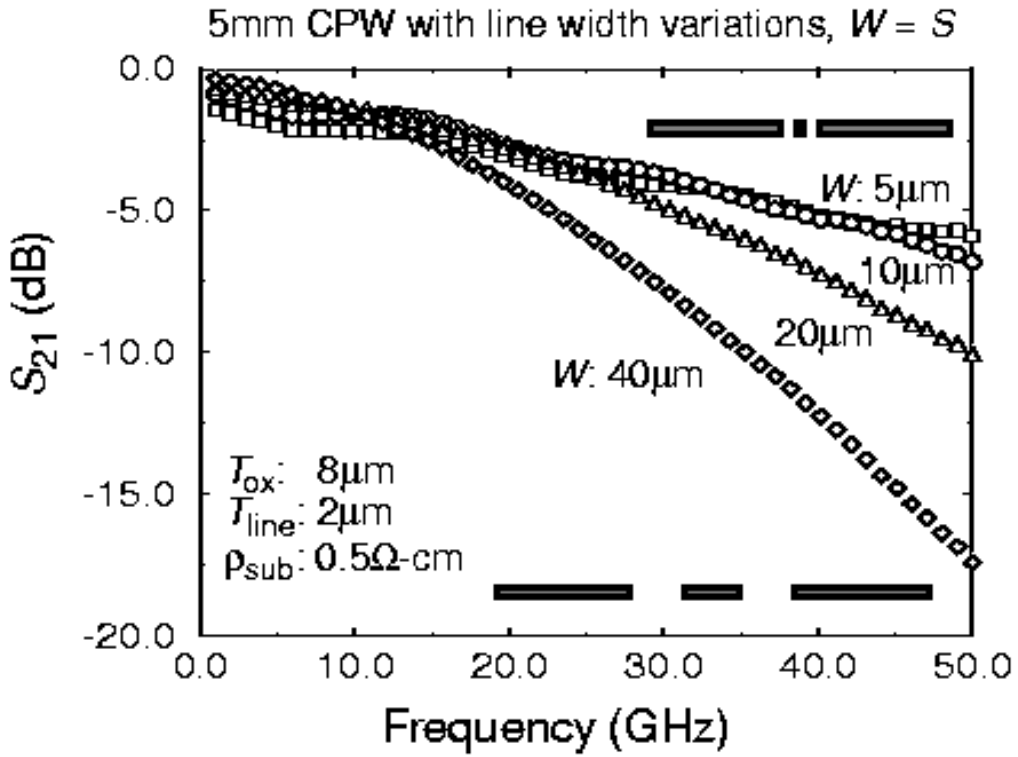
- Still high resistive losses in metal 1

Coplanar Waveguide Ground Return



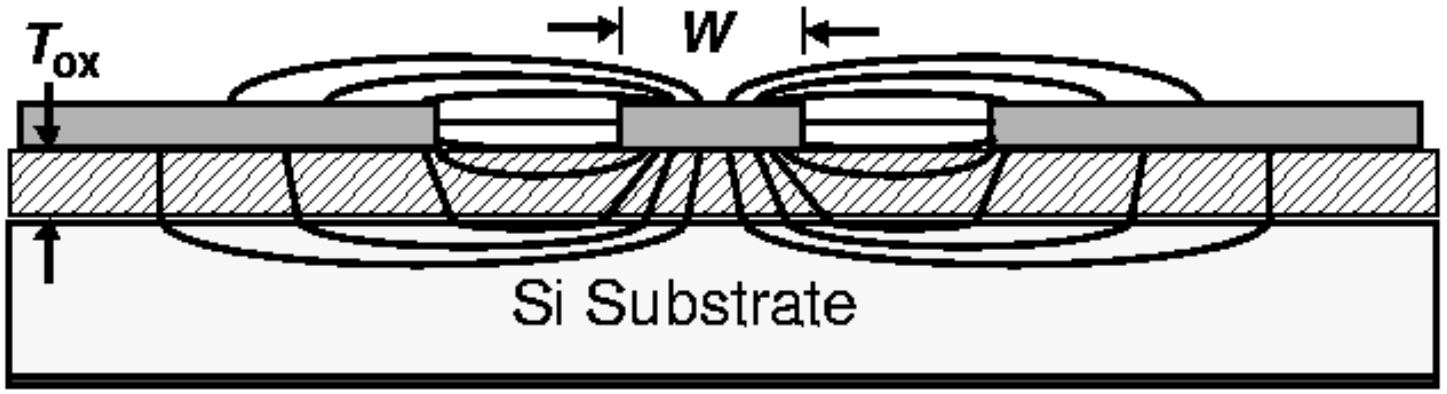
Take advantage of top level T_{metal} and T_{ox} scaling

S parameters for Various Line Widths

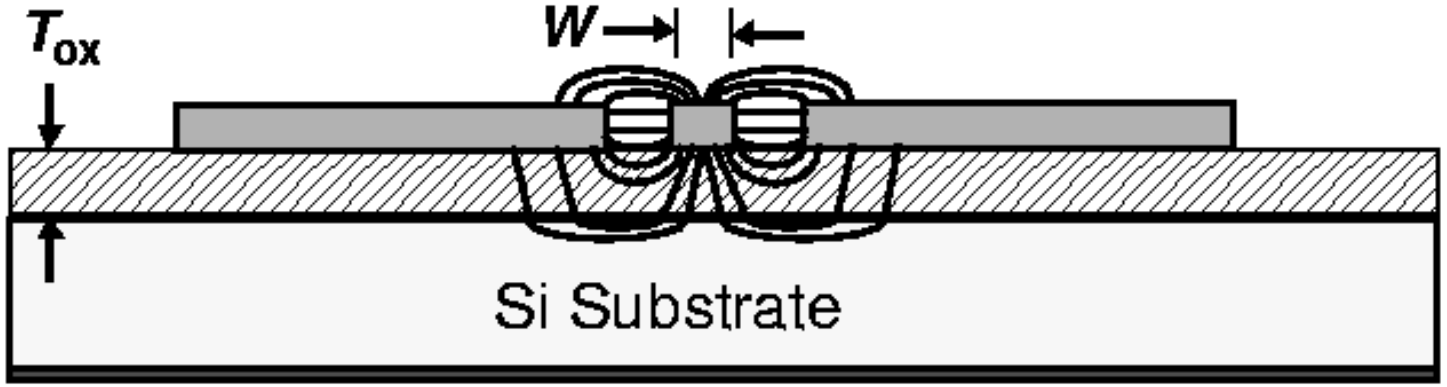


- Wide lines have high loss at high frequencies

Si Substrate Coupling vs. Line Width

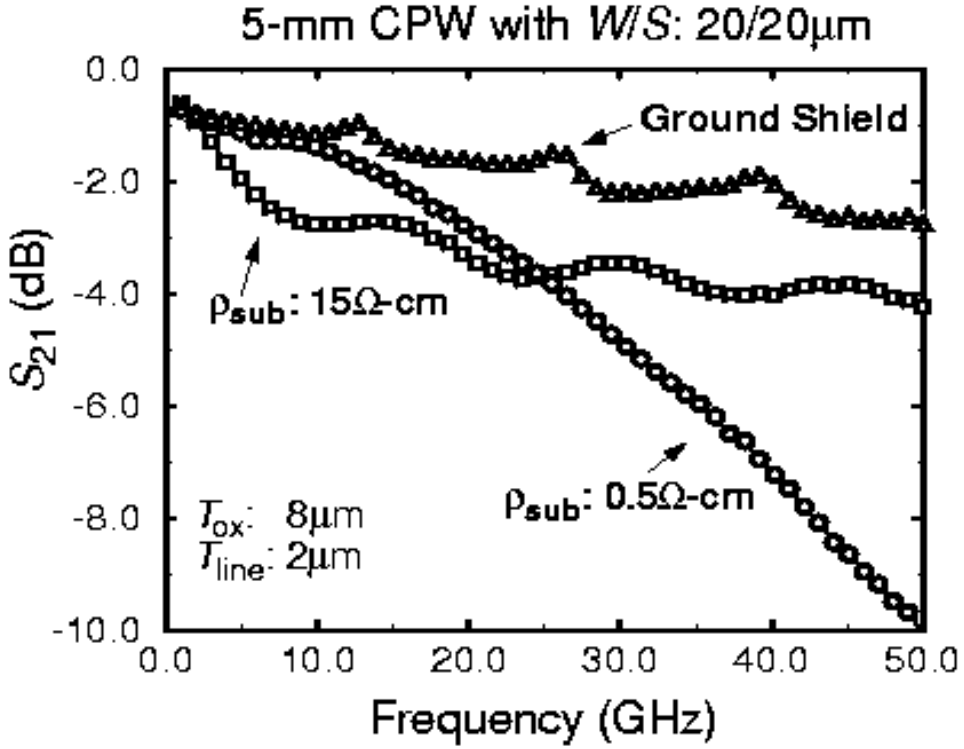


Large Width, Space → large coupling through substrate



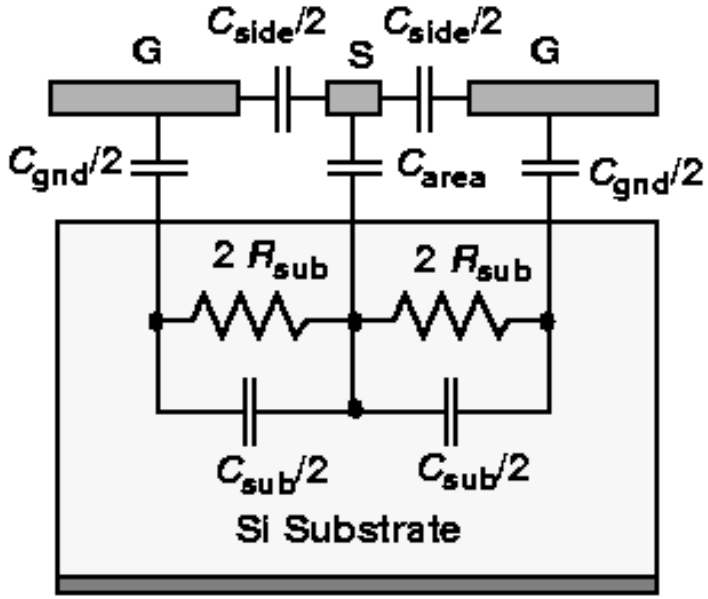
Small Width, Space → small coupling through substrate

S parameters for Different Substrates

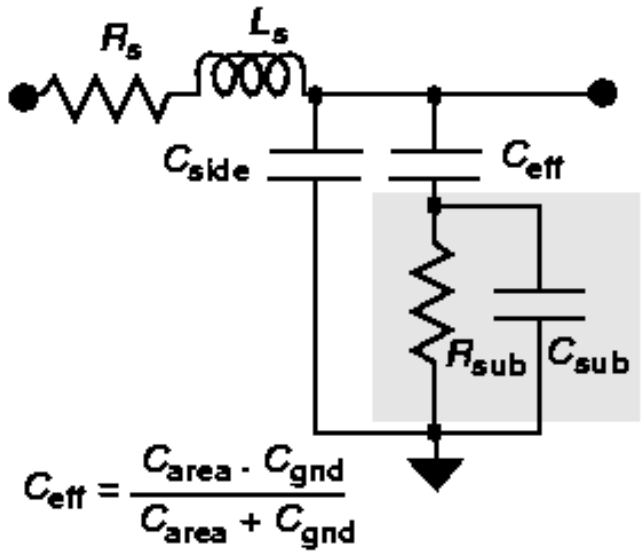


Low-ρ substrate yields lowest loss below 25 GHz

Model of Coplanar Waveguide

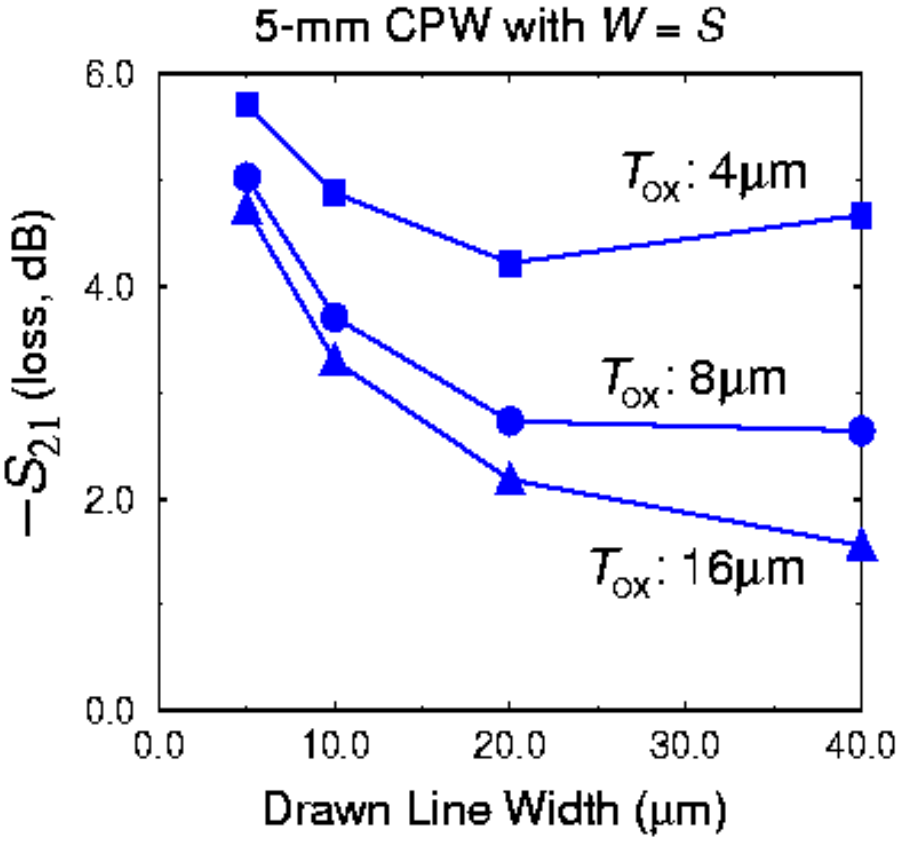


Cross-section of CPW



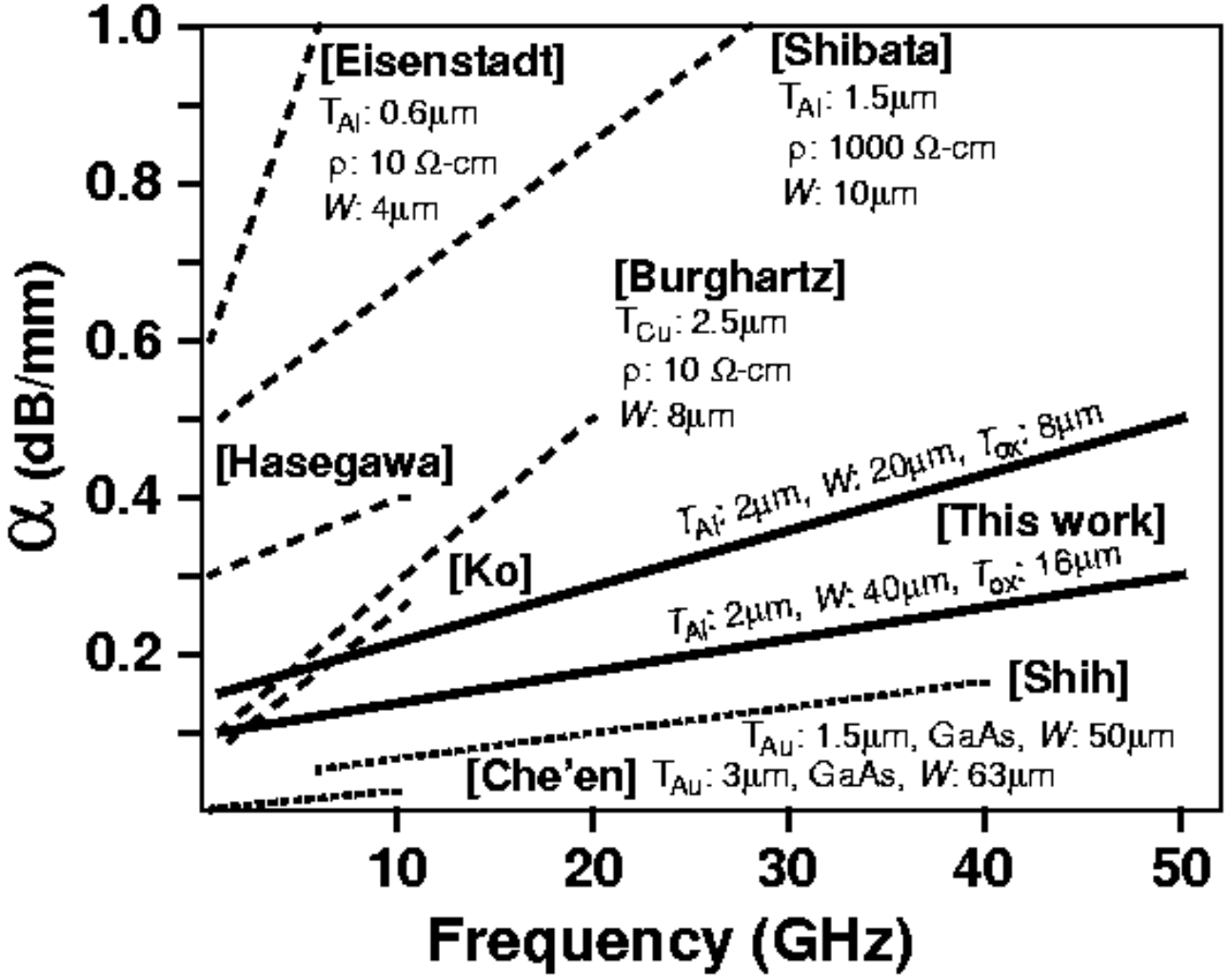
Segment line model

Ground Shield CPW Loss at 50 GHz



T_{ox} = 16 µm ⟶ 1.5 dB loss for a 5-mm line at 50 GHz

Transmission Line Loss Comparison



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Monolithic Resonator Design

Design Goals:

- Compatible with conventional CMOS technology
- Epi substrate with low resistivity (0.01–1 Ω-cm)
- Resonant frequency above 10 GHz

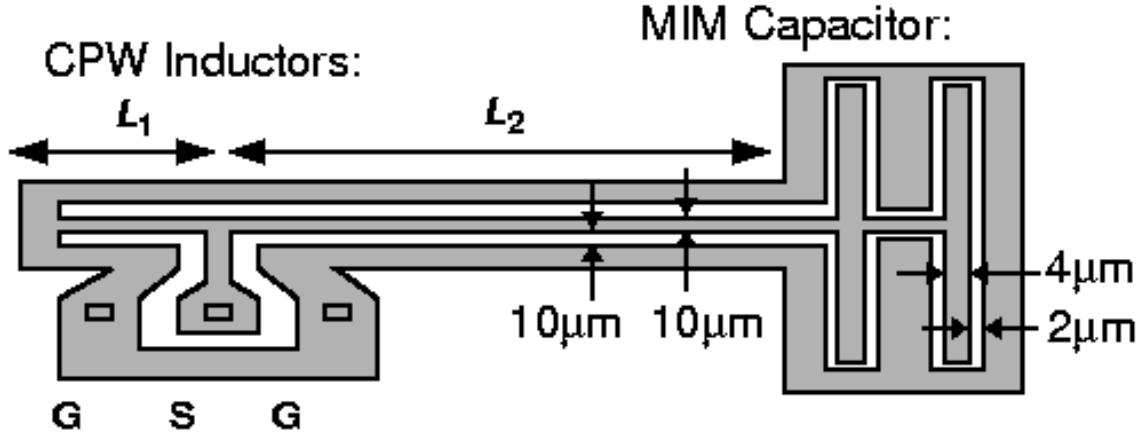
Process Assumptions (M. Bohr, IEDM-96):

- Top-layer aluminum thickness of 2μm
- T_{ox} = 8μm between top-layer metal and substrate

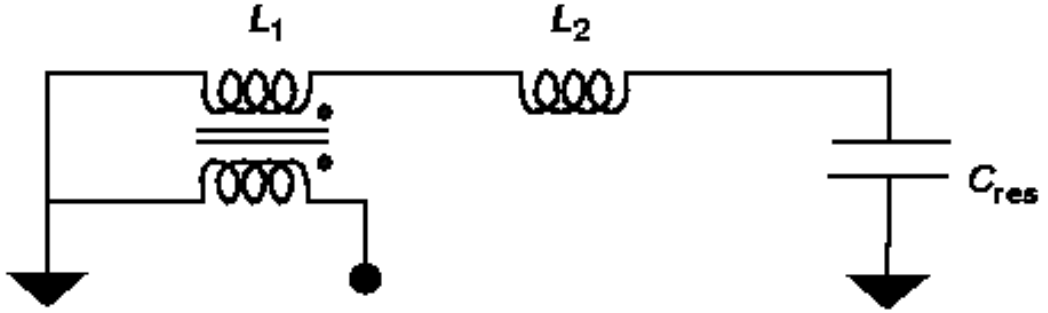
Coplanar Distributed Resonator Design

- Inductors made with 10/10μm line width and space
- Capacitor made with 4/2μm line width and space

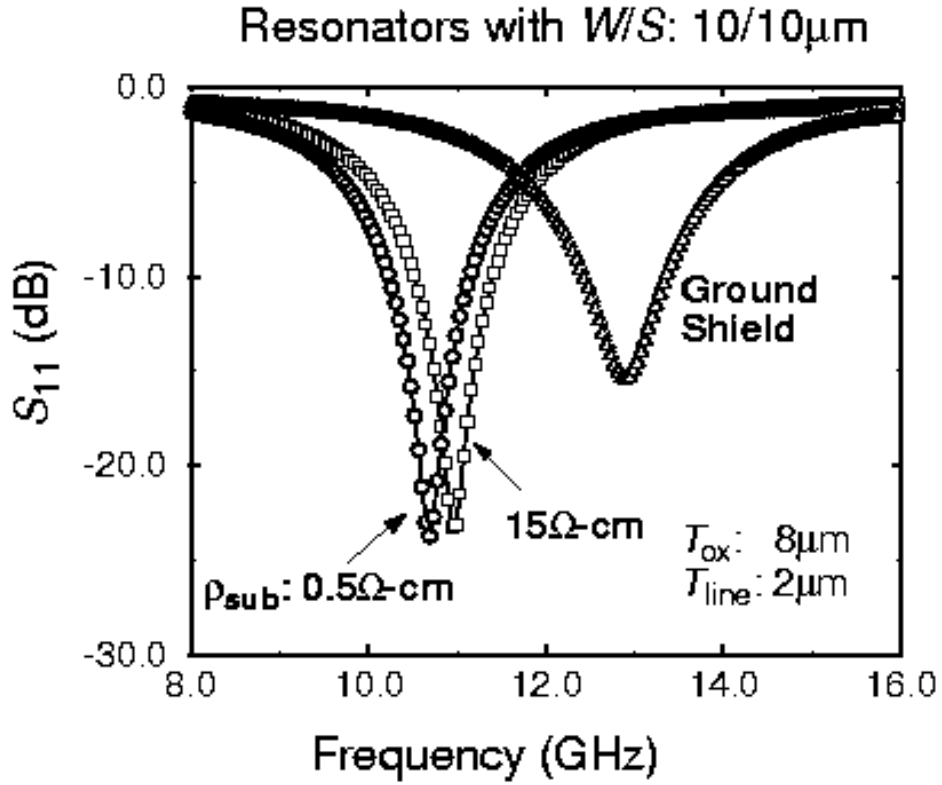
Top view:



Model:



One-Port Characteristics of Resonators



- Resonator Q of 7 is achieved at 11 and 13 GHz

Conclusions

- Exploit reverse technology scaling of the top metal layers
- No fundamental limit to CMOS interconnects at 50 GHz

Key Results:

- Low loss transmission lines (0.3dB/mm at 50 GHz)
- Compatibility with low-ρ CMOS epi-substrates
- Transmission line implementation of coupled inductors
- Resonators with $Q = 7$ above 10 GHz

Acknowledgments

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Discussions:

- Liam Madden, C. Patrick Yue, and Alvin L. S. Loke