50-GHz Interconnect Design in Standard Silicon Technology

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Outline

- Conclusions
- Monolithic Resonator Design
- On-Chip Transmission Lines on Si
- Future Interconnect Process Emulation
- Introduction, Logic Process Scaling
CMOS Logic Process Scaling Trends

- Dimensions and gate delay: 0.7x per generation
- Interconnect delay: ?

![CMOS Technology Generation Diagram](image)
CMOS Logic Process Scaling Trends

- Interconnect delay: depends on the level
Reverse Scaling of Top-Layer Metals

- CMOS transistor density increases
- Supply current increases
Top-Level Metal to Si Distance Trend

CMOS Technology Generation

Trend: 1.5μm x #layers

hp: Hewlett Packard
int: Intel
mot: Motorola

hp-3
hp-4
int-5
mot-6

1μm x #layers

Year

93
95
97
99
2001
Future Interconnect Process Emulation

- Only emulate top metal layer(s)
- Deposit thick oxide underneath metal layers
On-Chip Microstrip with High-$\rho$ Si

- High dielectric losses in substrate
On-chip Microstrip with Low-$\rho$ Si

- High *resistive* losses in substrate
Microstrip with M1 Ground Return

- Still high resistive losses in metal 1
Coplanar Waveguide Ground Return

Take advantage of top level $T_{\text{metal}}$ and $T_{\text{ox}}$ scaling
S parameters for Various Line Widths

- Wide lines have high loss at high frequencies
Si Substrate Coupling vs. Line Width

Large Width, Space $\rightarrow$ large coupling through substrate

Small Width, Space $\rightarrow$ small coupling through substrate
$S$ parameters for Different Substrates

5-mm CPW with $W/S$: 20/20µm

$S_{21}$ (dB)

- $\rho_{\text{sub}}$: 15Ω-cm
- $T_{\text{ox}}$: 8µm
- $T_{\text{line}}$: 2µm
- $\rho_{\text{sub}}$: 0.5Ω-cm

Frequency (GHz)

Low-$\rho$ substrate yields lowest loss below 25 GHz
Model of Coplanar Waveguide

Cross-section of CPW

Segment line model

\[ C_{\text{eff}} = \frac{C_{\text{area}} \cdot C_{\text{gnd}}}{C_{\text{area}} + C_{\text{gnd}}} \]
Ground Shield CPW Loss at 50 GHz

$T_{ox} = 16 \mu m \rightarrow 1.5$ dB loss for a 5-mm line at 50 GHz
Transmission Line Loss Comparison

[Eisenstadt]
- $T_{AI}$: 0.6$\mu$m
- $\rho$: 10 $\Omega$-cm
- $W$: 4$\mu$m

[Shibata]
- $T_{AI}$: 1.5$\mu$m
- $\rho$: 1000 $\Omega$-cm
- $W$: 10$\mu$m

[Burghartz]
- $T_{Cu}$: 2.5$\mu$m
- $\rho$: 10 $\Omega$-cm
- $W$: 8$\mu$m

[Hasegawa]
- $T_{AI}$: 2$\mu$m, $W$: 20$\mu$m, $T_{ox}$: 8$\mu$m

[Ko]
- $T_{AI}$: 2$\mu$m, $W$: 40$\mu$m, $T_{ox}$: 16$\mu$m

[This work]
- $T_{Au}$: 1.5$\mu$m, GaAs, $W$: 50$\mu$m
- $T_{Au}$: 3$\mu$m, GaAs, $W$: 63$\mu$m

[Che’en]
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Monolithic Resonator Design

Design Goals:
- Compatible with conventional CMOS technology
- Epi substrate with low resistivity (0.01–1 Ω-cm)
- Resonant frequency above 10 GHz

Process Assumptions (M. Bohr, IEDM-96):
- Top-layer aluminum thickness of 2µm
- $T_{ox} = 8µm$ between top-layer metal and substrate
Coplanar Distributed Resonator Design

- Inductors made with $10/10\mu m$ line width and space
- Capacitor made with $4/2\mu m$ line width and space

Top view:

CPW Inductors:

MIM Capacitor:

Model:

$C_{res}$
One-Port Characteristics of Resonators

- Resonator Q of 7 is achieved at 11 and 13 GHz

Resonators with W/S: 10/10 μm

- Ground Shield
- 15Ω-cm
- 8μm
- 0.5Ω-cm
- T_{ox}
- T_{line}-2μm

(BP)^{11}\ S

Frequency (GHz)
Conclusions

- Exploit reverse technology scaling of the top metal layers
- No fundamental limit to CMOS interconnects at 50 GHz

Key Results:
- Low loss transmission lines (0.3dB/mm at 50 GHz)
- Compatibility with low-\(\rho\) CMOS epi-substrates
- Transmission line implementation of coupled inductors
- Resonators with \(Q = 7\) above 10 GHz
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