Modeling and Characterization of On-Chip Transformers

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OUTLINE

- Motivation
- Background
- On-chip transformer realizations
- Models
- Experimental verification
- Summary
**Motivation for Transformer Modeling**

- Essential for Radio Frequency Integrated Circuits (RFICs)
- 3-D field solvers are **inconvenient**
  - Numerically expensive and cumbersome
  - Good for **verification** but not for **design**
- Scalable, analytical models
  - Design **guidelines** and explore **trade-offs**
  - Circuit **design** and **optimization**
SELF-INDUCTANCE

replacements $v_1$

$\begin{array}{|c|c|}
\hline
\text{Quantity} & \text{Units} \\
\hline
i_1 & A \\
v_1 & V \\
t & s \\
L_1 & H \\
\hline
\end{array}$

- $v_1 = L_1 \frac{\partial i_1}{\partial t}$
- nH typical in RF On-chip environment
Mutual Inductance

\[ v_2 = M \frac{\partial i_1}{\partial t} \]
\[
\begin{align*}
\text{Mutual coupling coefficient, } k &= \frac{M}{\sqrt{L_1 L_2}} \\
|k| &\leq 1
\end{align*}
\]
**Non-Ideal Transformer**

- $k = \frac{M}{\sqrt{L_1 L_2}} < 1$.
- Series resistance.
- Port-to-port & port-to-substrate capacitances.
 configurations

- Three or four terminal device
- Grounded terminals
TAPPED TRANSFORMER

- Low $k(\approx 0.3 - 0.5)$
- High $L_1, L_2$
- Top metal layer
- Asymmetric
- Low port-to-port capacitance
**Interleaved Transformer**

- Medium $k (\approx 0.7 - 0.8)$
- Low $L_1, L_2$
- Top metal layer
- Symmetric
- Medium port-to-port capacitance
Stacked Transformer

- High $k (\approx 0.9)$
- High $L_1, L_2$
- Multiple metal layers
- Area efficient
- High port-to-port & port-to-substrate capacitances
**STACKED TRANSFORMER VARIATIONS**

- Shift top and bottom spirals laterally or diagonally
- Trade-off lower $k$ for reduced port-to-port capacitance
## Comparison of Transformer Realizations

<table>
<thead>
<tr>
<th>Transformer type</th>
<th>Area</th>
<th>Coupling coefficient, $k$</th>
<th>Self-inductance</th>
<th>Self-resonant frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tapped</td>
<td>High</td>
<td>Low</td>
<td>Mid</td>
<td>High</td>
</tr>
<tr>
<td>Interleaved</td>
<td>High</td>
<td>Mid</td>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td>Stacked</td>
<td>Low</td>
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</table>

- Non-idealities result in trade-offs
- Optimal choice determined by circuit application
- Transformer models needed for comparison
**Self-Inductance Calculation**

A graph showing the percentage of inductors exceeding absolute error against the percentage of absolute error.

The modified Wheeler expression is given by:

\[ L = \frac{9.375 \mu_0 n^2 AD^2}{11 OD - 7 AD} \]

- Verified by measurements (75) and 3-D field solver simulations (17,000)
TAPPED TRANSFORMER MODEL

- Evaluate $C_{ov,o}$, $C_{ox,o}$, $C_{ox,i}$, $R_{s,o}$ & $R_{s,i}$ by extending previous work
- Use modified Wheeler expression for $L_{s,o}$, $L_{s,i}$
- Calculate $M$
Mutual Inductance Calculation

- Single inductor: $L_T$
- Interleaved transformer: $L_1$ (primary), $L_2$ (secondary)
- Tapped transformer: $L_1$ (inner), $L_2$ (outer)

$$L_T = L_1 + L_2 + 2M$$
$k$ FOR TAPPED AND INTERLEAVED TRANSFORMERS

1. Find $L_1$, $L_2$ and $L_T$

2. Determine $M$ from $M = 0.5(L_T - L_1 - L_2)$

3. Evaluate $k = \frac{M}{\sqrt{L_1 L_2}}$
STACKED TRANSFORMER MODEL

- Evaluate $C_{ov}, C_{ox,t}, C_{oxm}, C_{ox,b}, R_{s,t}$ & $R_{s,b}$ by extending previous work
- Use modified Wheeler expression for $L_{s,t}, L_{s,b}$
- Calculate $M$
Current Sheet Approach for $k$

- Reduce complexity by $4n^2$
- Use symmetry
- Derive simple expression using electromagnetic theory
\( k \) for Stacked Transformers

\[ k \approx (0.9 - d_{\text{norm}}) \]
(for \( k > 0.2 \))

\[ d_{\text{norm}} = \sqrt{\frac{x_s^2 + y_s^2}{AD}} = \frac{d_s}{AD} \]

- Metal and oxide thicknesses have only 2nd order effects on \( k \)
$M$ for Stacked Transformers

1. Find $L_1$ and $L_2$

2. Determine $k$

3. Evaluate $M = k \sqrt{L_1 L_2}$
ACCURACY OF MODELS

- Lumped model of distributed structure
- Substrate not modeled
- Patterned Ground Shield (PGS)
  - Eliminates resistive and capacitive coupling to substrate
  - Inductive coupling to substrate may degrade performance at high frequencies
**Experimental Set-up**

- **DUT**: Device Under Test
- **Coplanar GSG probes**: Coupling probes for measurement
- **50Ω environment**: Measurement environment for 50 ohm impedance

**Diagram**:
- **HP8720B network analyzer** connected to the DUT
- **S parameters** measured using the network analyzer
- **L₁, M, L₂**: Components of the circuit model
- **Port 1, Port 2, Port 3**: Connection points for measurement and analysis

**PSfrag replacements**:
- Port 1 replacements
- Port 2 replacements
- Port 3 replacements
Die Photo
**Experimental Verification: Tapped**

- **ODo = 290 \mu m**,  
  \( n_o = 2.5 \)
- **ODi = 190 \mu m**,  
  \( n_i = 4.25 \)
- **w = 13 \mu m**,  \( s = 7 \mu m \)

---

**Frequency (GHz)**

<table>
<thead>
<tr>
<th>Frequency (GHz)</th>
<th>0.8</th>
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**Experimental Verification: Stacked 1**

- Stacked transformer with top spiral overlapping bottom one
- \( OD = 180\mu m, n = 11.75, w = 3.2\mu m, s = 2.1\mu m \)
- \( x_s = 0\mu m, y_s = 0\mu m, d_s = 0\mu m \)

![PSfrag replacements](image1)

![PSfrag replacements](image2)

![PSfrag replacements](image3)

![PSfrag replacements](image4)
CONTRIBUTIONS

- On-chip transformer models

- Expressions for mutual inductance and mutual coupling coefficient

- Models verified by measurements

- Basis for design and optimization of transformer circuits
ACKNOWLEDGMENTS

IBM fellowship support

NSF contract MIP-9313701

Rockwell International
  Dr. Christopher Hull
  Dr. Paramjit Singh

Staff of the Stanford Nanofabrication Facility

Industrial Sponsors of the Center for Integrated Systems