Analysis and Optimization of Accumulation-Mode Varactor for RF ICs


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Outline

• Introduction
• Operation
• Characterization
• Optimization
• Conclusion
Phase Noise in VCOs

\[ \frac{1}{Q_{tot}} = \frac{1}{Q_L} + \frac{1}{Q_C} + \frac{1}{Q_{ext}} \]

\[ \mathcal{L}(\Delta \omega) \propto \frac{\omega_o^2}{P_{\text{diss}} Q_{tot}^2 (\Delta \omega)^n} \]

- \( Q_L \sim 4-8 \) for 1-10 nH spiral inductor.
- Need \( Q_C > 40-80 \) to minimize \( Q_{tot} \) degradation.
## Conventional IC Varactors

<table>
<thead>
<tr>
<th></th>
<th>PN junction</th>
<th>MOS capacitor</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Bias</strong></td>
<td>reverse</td>
<td>depletion-inversion</td>
</tr>
<tr>
<td><strong>C</strong></td>
<td>moderate (0.4 fF/μm²)</td>
<td>high (2-7 fF/μm²)</td>
</tr>
<tr>
<td><strong>Q</strong></td>
<td>low (5-7 for 1-10 pF)</td>
<td>moderate (14/GHz/pF)</td>
</tr>
<tr>
<td><strong>Tuning range</strong></td>
<td>small (33%)</td>
<td>moderate (parasitic S/D junction cap limited)</td>
</tr>
<tr>
<td><strong>f_{SR}</strong></td>
<td>4-13 GHz</td>
<td>8 GHz for 2 pF</td>
</tr>
<tr>
<td><strong>TC</strong></td>
<td>high (200-1000 ppm/C)</td>
<td>moderate (30 ppm/C)</td>
</tr>
</tbody>
</table>

* [Burghartz, et.al., TED '96]
Accumulation-Mode Varactor

- Standard CMOS process
- Reduce parasitic S/D junction capacitance
- High C per area (increases with technology scaling)
- High Q (increases with technology scaling)
- High tuning range (improves with technology scaling, 200% maximum limit)
- Moderate TC
Operating Regimes

Accumulation

$V_g > V_{FB}$

Depletion

$V_T < V_g < V_{FB}$

$N_D^+$
Physical Model

Accumulation

Depletion

G

S/D

n-well

n+

n+

Ls

Rg

Cox

CSi

Racc

Rd

Rw

Cw

Rd

Racc

C Si

Rd

C w

Rw

Rd

C d

C ox

C d

Rd

C w

R w

Rd

C Si

R w
## Physical Model Parameters

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Expression</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{ox}$</td>
<td>$\frac{NW}{L} \varepsilon_{ox} \frac{t_{ox}}{t_{ox}}$</td>
<td>oxide capacitance</td>
</tr>
<tr>
<td>$C_{Si}(u_s, u_b)$</td>
<td>$\frac{NW}{L} \varepsilon_{Si} \left( \frac{\sinh(u_s) - \sinh(u_b)}{F(u_s, u_b)} \right)$</td>
<td>semiconductor capacitance</td>
</tr>
<tr>
<td></td>
<td>$F(u_s, u_b) = \sqrt{2} \left[ \sinh(u_b(u_b - u_s) - \cosh(u_b) - \cosh(u_s) \right]^{1/2}$</td>
<td></td>
</tr>
<tr>
<td>$C_d$</td>
<td>$\frac{NW}{L} x_{ldd} C_{Si}(u_s, u_{ldd})$</td>
<td>channel-to-S/D depletion cap</td>
</tr>
<tr>
<td>$R_{acc}$</td>
<td>$\frac{L}{2NW L_{acc}^2 Q_{acc}}$</td>
<td>accumulation-layer resistance</td>
</tr>
<tr>
<td></td>
<td>$Q_{acc} = \varepsilon_{Si} \frac{kT}{q L_{di}} F(u_s, u_b)$</td>
<td></td>
</tr>
<tr>
<td>$R_g, R_w$</td>
<td>$\frac{R_{gsq}}{3NL}, \frac{R_{wsq} L_w}{2NW}$</td>
<td>gate and well resistance</td>
</tr>
<tr>
<td>$R_d$</td>
<td>$\frac{R_{lddsq} L_{ldd}}{NW} + R_{contact}$</td>
<td>LDD and contact resistance</td>
</tr>
</tbody>
</table>
Series Capacitance

\[ C_s = \frac{C_{ox}C_{Si}}{C_{ox} + C_{Si}} \]

Accumulation

- \( C_{Si} \) in accumulation is associated with accumulation-layer charge (e\(^-\)).

Depletion

\[ C_s = \frac{C_{ox}(C_{Si} + 2C_d)}{C_{ox}(C_{Si} + 2C_d)} \]

- \( C_{Si} \) in depletion is depletion capacitance associated with fixed donor charge (N_\text{D}^+).

\( C_s \) varies with bias voltage as \( C_{Si}, C_d \) are bias-dependent.
Series Resistance (Varactor Loss)

\[ R_s \approx \left( R_g + \left[ \frac{1}{2} (R_{acc} + R_d) \parallel R_w \right] \right) \]
\[ \approx \frac{R_{acc}}{2} \parallel R_w \]

\[ R_s \approx R_g + R_w \left( \frac{C_{Si}}{C_{Si} + 2C_d} \right)^2 \]

- \( R_s \) can be reduced by controlling device geometry.

\( R_s \) varies with bias voltage as \( R_{acc} \), \( C_{Si} \), and \( C_d \) are bias-dependent.
Quality Factor (Q)

\[ Q = \frac{1}{\omega R_s C_s} \]

- Frequency-dependent.
- Bias-dependent as \( R_s, C_s \) varies with bias.
Tuning Range

- Tuning range = $\frac{2C_{ox}}{C_{ox} + 2C_{Si, min}} \Rightarrow 200\% @$ maximum limit.

- As technology scales, tuning range increases towards the limit.

- When used with low-TC capacitor (eg. MIM capacitor) temperature stability can be improved by trading-off with tuning range.
Test Structure

W = 15.85 um
L = 1.95 um
N (no of gate fingers) = 14
Measurement Setup

Bias Generator

Probe Station

Device Under Test
• At $V_g \gg V_{FB}$, $C \approx C_{ox}$

• At $V_g < V_{FB}$, $C \approx \frac{C_{ox}C_{Si}}{C_{ox} + C_{Si}}$

• Exhibit frequency dependence associated with parasitic inductance $\Rightarrow C_{s, eff} = \frac{C_s}{1 - \omega^2 L_s C_s}$, $f_{SR} \geq 15\text{GHz}$
Measured Series Resistance

- In accumulation, $R_s$ increases as $V_g$ is swept from deep accumulation towards flatband due to extraction of accumulation-layer charges.
- In depletion, $R_s$ decreases beyond flatband due to the decrease of $C_{Si}$ which reduces the effect of $R_w$. 

![Graph showing Measured and Modeled Series Resistance vs. $V_g$](image)
• Q reaches minimum at flatband voltage where changes in capacitance is large.

\[\text{trade-off between Q and capacitance tuning.}\]
Optimization Formulation

Objective: maximize Q subject to following constraints

- $C =$ nominal desired capacitance (1 pF)
- Area < max allowed area
- Tuning range > min required tuning range (+/- 30%)
- $W >$ min allowed channel width (0.6 um)
- $L >$ min allowed channel length (0.4 um)
- $N >$ min no of gate finger (1)
- Biased in accumulation mode (to minimize substrate effect) ($V_g > V_{FB}$)

Optimization variables: $W, L, N, V_g$
Optimization Results (0.5 µm CMOS)

\( C_{\text{nom}} = 1 \text{ pF}, \quad Q @ 1 \text{ GHz} \)

\( Q_{\text{max}} = 200!! \)
Conclusions

- Standard CMOS implementation.
- Varactor model has been developed and used for device optimization.
- Substrate effect can be mitigated by operating in accumulation mode.
- Wide tuning range allows trade-off with temperature stability.
- Performance improves with technology scaling.