A 1.4-GHz 3-mW 0.5-µm CMOS LC Low Phase Noise VCO Using Tapped Bond Wire Inductors

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A 1.4-GHz 3-mW CMOS LC Low Phase Noise VCO using Tapped Bond Wires

Outline

• Goals
• Approach
• Circuit
• Results
Goals of Design

- GPS - 1.575 GHz, IF=200MHz
- Low Power
- Minimum Phase Noise
- Tunable
- Reasonable Area
A 1.4-GHz 3-mW CMOS LC Low Phase Noise VCO using Tapped Bond Wires

200 MHz IF Frequency for GPS

IF Amp

1.6 GHz

0.2 GHz

1.4 GHz

200 MHz
Ring Oscillator vs. LC Oscillator

Ring Oscillator: Dissipates all stored energy each cycle
→ High power dissipation
Large tuning range

LC Oscillator: Dissipates 1/Q of the energy in the resonant tank
→ Lower power dissipation

\[ Q = \frac{\text{Stored energy}}{\text{Dissipated energy}} \times 2\pi \]
Known As Clock Jitter.

Frequency Instability - Time Domain
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**Frequency Instability - Freq Domain**

Known As Phase Noise.

![Diagram of frequency instability]

- **Ideal**: A vertical peak at the center frequency $f_0$.
- **Actual**: A broad peak with a sideband spectrum analyzed by a spectrum analyzer.

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Units of Phase Noise

\[
S_v(\omega) \quad \Delta \omega \quad dB_c
\]

\[
L\{\Delta \omega\} \quad [dBc/Hz]
\]

\[
\frac{1}{f^3} \quad (-30dB/dec)
\]

\[
\frac{1}{f^2} \quad (-20dB/dec)
\]

\[
\log(\Delta \omega) = \log(\omega - \omega_0)
\]

*Measured in dB below carrier per unit bandwidth.*
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$1/f$ noise of CMOS vs BJT

Internal noise sources set a fundamental limit for phase noise.

Low frequency noise can be an important contributor to the system noise.
How To Achieve Low Phase Noise

• More Power

• Higher Q Resonant Tank
  (use of bond wires and tapping)

• Single-ended Symmetry
Basic LC Oscillator Configuration
Oscillator Block Diagram

LC Tank
A low frequency current induces a frequency change for the asymmetric waveform.
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Basic Design Configuration

\[ W_p = 2 \times W_n \]
Implementing the LC Tank

A

B

C

D
Implementing the LC Tank

\[ a \]

\[ b \]
Implementing the LC Tank

\[ -R \]

\[ -R \]

\[ a \]

\[ b \]

\[ c \]

package
die
Circuit Diagram
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Die Photo and Packaging

Bond Wire Inductor

die

package

1 mm
Output Spectrum of Oscillator

Frequency (100 kHz/div)
Center at 1.4 GHz

Magnitude (10 dB/div)
Phase Noise vs. Offset Frequency

-107 dBc/Hz @ 100 kHz
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Frequency vs. Control Voltage

Control Voltage (V)

Frequency (GHz)
## Results

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency</td>
<td>1.4 GHz</td>
</tr>
<tr>
<td>Power</td>
<td>3 mW at 3.0V supply</td>
</tr>
<tr>
<td>Phase Noise</td>
<td>-83 dBc/Hz @ 10kHz</td>
</tr>
<tr>
<td>for various offsets</td>
<td>-107 dBc/Hz @ 100kHz</td>
</tr>
<tr>
<td></td>
<td>-122 dBc/Hz @ 600kHz</td>
</tr>
<tr>
<td>Tuning Range</td>
<td>220 MHz (17%)</td>
</tr>
<tr>
<td>Process Technology</td>
<td>0.5-μm standard CMOS</td>
</tr>
</tbody>
</table>
### Figure of Merit- CMOS w/Bond Wires

<table>
<thead>
<tr>
<th>Method</th>
<th>Frequency</th>
<th>Power</th>
<th>Phase Noise (PN)</th>
<th>FOM</th>
</tr>
</thead>
<tbody>
<tr>
<td>This work</td>
<td>1.4 GHz</td>
<td>3 mW</td>
<td>-107 dBc/Hz</td>
<td>315 dBF</td>
</tr>
<tr>
<td>Tapping [3]</td>
<td>1.8 GHz</td>
<td>24 mW</td>
<td>-109 dBc/Hz</td>
<td>310 dBF</td>
</tr>
<tr>
<td>Single-sided Symmetry [2]</td>
<td>1.6 GHz</td>
<td>0.5 mW</td>
<td>-95 dBc/Hz</td>
<td>312 dBF</td>
</tr>
</tbody>
</table>

**Figure of Merit(dBF) = 20 log(freq) - PN - 10 log(power)**
A 1.4-GHz 3-mW CMOS LC Low Phase Noise VCO using Tapped Bond Wires

**Figure of Merit - Various Technologies**

<table>
<thead>
<tr>
<th>Technology</th>
<th>Freq</th>
<th>Power</th>
<th>@100kHz</th>
<th>FOM</th>
</tr>
</thead>
<tbody>
<tr>
<td>This work</td>
<td>1.4 GHz</td>
<td>3 mW</td>
<td>-107 dBc/Hz</td>
<td>315 dBF</td>
</tr>
<tr>
<td>CMOS [6]</td>
<td>1.8 GHz</td>
<td>6 mW</td>
<td>-105 dBc/Hz</td>
<td>312 dBF</td>
</tr>
<tr>
<td>BJT [4]</td>
<td>1.1 GHz</td>
<td>2 mW</td>
<td>-95 dBc/Hz</td>
<td>302 dBF</td>
</tr>
<tr>
<td>BiCMOS [5]</td>
<td>1.8 GHz</td>
<td>70 mW</td>
<td>-88 dBc/Hz</td>
<td>285 dBF</td>
</tr>
</tbody>
</table>

BJT oscillator

Figure of Merit (dBF) = 20 log(freq) - PN - 10 log(power)
### Figure of Merit - Ring vs. LC

<table>
<thead>
<tr>
<th>Design</th>
<th>Freq</th>
<th>Power</th>
<th>@100kHz</th>
<th>FOM</th>
</tr>
</thead>
<tbody>
<tr>
<td>This work</td>
<td>1.4 GHz</td>
<td>3 mW</td>
<td>-107 dBC/Hz</td>
<td>315 dBF</td>
</tr>
<tr>
<td>Ring Oscillator</td>
<td>1.8 GHz</td>
<td>10 mW</td>
<td>-75 dBC/Hz</td>
<td>280 dBF</td>
</tr>
<tr>
<td>Ring Oscillator</td>
<td>1.2 GHz</td>
<td>20 mW</td>
<td>-80 dBC/Hz</td>
<td>278 dBF</td>
</tr>
<tr>
<td>Ring Oscillator</td>
<td>5.4 GHz</td>
<td>80 mW</td>
<td>-79 dBC/Hz</td>
<td>284 dBF</td>
</tr>
</tbody>
</table>

Figure of Merit (dBF) = 20 log(freq) - PN - 10 log(power)
Conclusions

• Tapping allows a greater amount of energy in the resonant tank, thereby increasing the signal energy without increasing the noise.

• Independently, single-sided symmetry reduces the up-converted low frequency phase noise contribution from the active devices.

• CMOS is a growing and attractive solution for RF oscillators.
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