At submicron channel lengths, CMOS is an attractive alternative to silicon bipolar and GaAs MESFET technologies for use in wireless receivers. A 12mW global positioning system (GPS) receiver front-end, comprising a low noise amplifier (LNA) and mixer implemented in a standard 0.35\mu m digital CMOS process, demonstrates the aptitude of CMOS for portable wireless applications.

A block diagram of the receiver front-end test is shown in Figure 1. The system consists of a LNA, buffer (for testing purposes only), and associated bias circuitry. Note that the LNA output and mixer input are taken off-chip to facilitate testing of each block individually.

To achieve a wide dynamic range, the noise figure of the LNA and linearity of the mixer are of primary concern. Figure 2 shows the circuit schematic of the LNA. A differential architecture is chosen in anticipation of eventual integration of a complete GPS receiver. Its common-mode rejection eases the task of rejecting interference from other on-chip elements, such as a DSP core. This choice results in increased amplifier noise for a given power dissipation compared to a single-ended implementation. This increase is mitigated by the high \( \omega_0 \) of the process, that permits acceptable noise performance despite a differential implementation.

The output signal from \( M_{1,2} \) flows through cascoding devices \( M_{3,4} \), bypassing the gates of the output stage to swing above the supply, which is advantageous for low-voltage operation. Note that resistors \( R_7,8 \) afford the on-chip environment improves linearity by reducing the signal currents in the MOS switches. Additionally, a large capacitive IF termination of both the RF and IF ports. A capacitive IF termination offers the advantage that it contributes no noise to the mixing process. At the RF port, a reactive tank is used to filter broadband noise from the source resistance and parasitic tank resistance, as well as the switches. Bond wires are used to achieve a good Q in addition to an innovative capacitor layout described in the next paragraph. A further improvement is the addition of inductors in series with the input source resistance to form an L-match together with part of the tank capacitance. This boosts the signal voltage and enhances filtering by increasing the effective source resistance.

Area-efficient linear capacitors are generally unavailable in standard digital process technologies (such as the one used here). However, deep submicron processes do allow small spacing between metal lines on any given interconnect layer, leading to high parallel plate capacitance. At submicron channel lengths, the switch capacitance is so small that it is normally considered undesirable, it is exploited in this design to augment the ordinary parallel plate capacitance. By operating the transistors in the linear region, good mixer linearity is achieved. The high impedance at the mixer IF port afforded by the on-chip environment improves linearity by reducing the signal currents in the MOS switches. Additionally, a large tank capacitors dominates the transistor non-linear parasitic capacitances.

The results of a two-tone IP3 measurement on the mixer are shown in Figure 5. Note that the impedance level at the mixer output is not 50\( \Omega \). Indeed, the impedance is complex, so in the mixer output quantities are expressed in dBm rather than dBm. The mixer has a -3.6dB voltage conversion gain, with an input-referred IP3 of -10dBm and an input 1dB compression point of -5dBm. Measured mixer SSB noise figure is 10dB. For these measurements, the LO drive amplitude is equivalent to the voltage swing associated with -5dBm into 100\( \Omega \). However, the LO port presents a nearly capacitive reactance, and hence actually dissipates little power.

The results of experimental measurements are summarized in Table 1. The LNA-mixer combination exhibits the best performance achieved to date of any CMOS implementation in this frequency range at this power level.

Acknowledgments:
The authors thank D. Dobberpuhl and Digital Equipment Corporation for supporting this work, and Vitesse Semiconductor for providing high-frequency packaging.

References:
22-3-1: Block diagram of the GPS front-end test setup.
22-3-2: LNA circuit schematic.
22-3-3: LNA forward gain (S21) and noise figure.
22-3-4: Schematic of mixer circuit with test buffer.
Mixer Third-Order Intercept (IP3)

Two-Tone Test, f1=1.575GHz, f2=1.585GHz

Output Amplitude (dBV)

Source Power (dBm)

22-3-5: Mixer two-tone IP3 measurement.
22-3-6: Chip micrograph.
**Low-noise amplifier**
- Frequency: 1.575GHz
- Noise figure: 3.8dB
- $S_{21}$: 17.7dB
- $S_{12}$: $\leq$ -52dB
- IP3 (input): -6dBm
- 1dB compression (input): -20dBm
- Power dissipation: 12mW

**Mixer**
- LO frequency: 1.4GHz
- LO amplitude: 300mV ($\approx$ 3.5dBm in 100$\Omega$)
- Voltage conversion gain: -3.6dB
- IP3 (input): 10dBm
- 1dB compression (input): -5dBm
- Noise figure (SSB): 10dB
- Supply voltage: 1.5V
- Technology: 0.35µm CMOS
- Die area: 0.84mm$^2$

**22-3-Table 1:** GPS front-end performance summary.